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2.4GHz RF transmitter with embedded 8051 compatible microcontroller and 9 input, 10 bit ADC

nRF24E2

FEATURES

- 2.4GHz RF transmitter
- 8051 compatible microcontroller
- compatible with nRF24E1
- 9 input 10 bit ADC 100kSPS
- Single 1.9V to 3.6V supply
- Internal voltage regulators
- 2 µA standby with wakeup on timer or external pin
- Internal VDD monitoring
- Supplied in 36 pin QFN (6x6mm) package
- 0.18µm CMOS technology
- Low Bill- of Material
- Ease of design

APPLICATIONS

- Wireless gamepads
- Wireless headsets
- Wireless keyboards
- Wireless mouse
- Wireless toys
- Intelligent sports equipment
- Industrial sensors
- PC peripherals
- Phone peripherals
- Tags
- Alarms
- Remote control

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1 GENERAL DESCRIPTION

The nRF24E2 is the transmitter part of the nRF2401 2.4GHz radio transceiver plus an embedded 8051 compatible microcontroller plus a 10-bit 9 input 100 kSPS AD converter. The circuit is supplied by only one voltage in range 1.9V to 3.6V. The nRF24E2 supports the proprietary and innovative modes of the nRF2401 such as ShockBurst™.

nRF24E2 is also a subset of the nRF24E1 chip, which means that it contains all functions of nRF24E1 except the radio receive functions, and it also means that it is fully program compatible with nRF24E1.

1.1 Quick Reference Data

Parameter	Value	Unit
Minimum supply voltage	1.9	V
Temperature range	-40 to +85	° C
Maximum RF output power	0	dBm
Maximum RF burst data rate	1000	kbps
Supply current for microcontroller @ 16MHz @3V	3	mA
Supply current for ADC @100 kSPS	0.9	mA
Supply current for RF transmit @ -5dBm output power	10.5	mA
Supply current in Power Down mode	2	µA
max CPU clock frequency	20	MHz
max AD conversion rate	100	kSPS
ADC Differential nonlinearity (DNL)	±0.5	LSB
ADC Integral nonlinearity (INL)	±0.75	LSB
ADC Spurious free dynamic range (SFDR)	65	dB
Package	36 pin QFN 6x6	

Table 1-1 : nRF24E2 quick reference data

Type Number	Description	Version
NRF24E2G	36 pin QFN 6x6, RoHS & SS-00259 compliant	B

Table 1-2 : nRF24E2 ordering information

1.2 Block Diagram

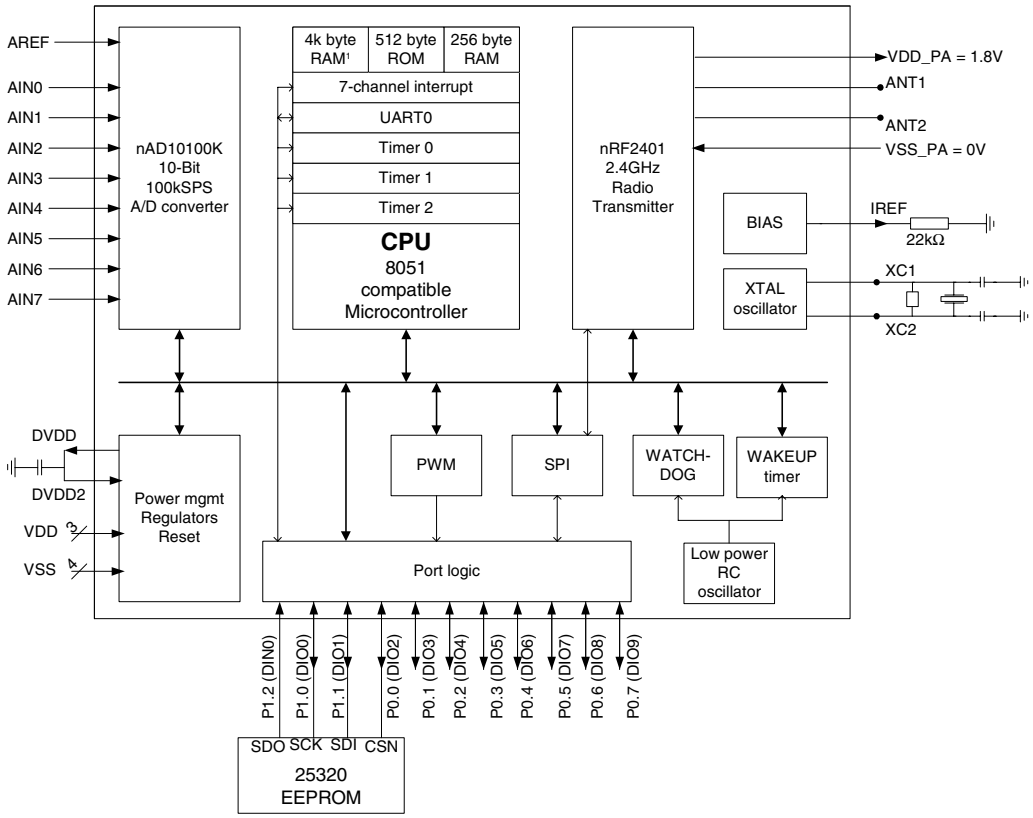
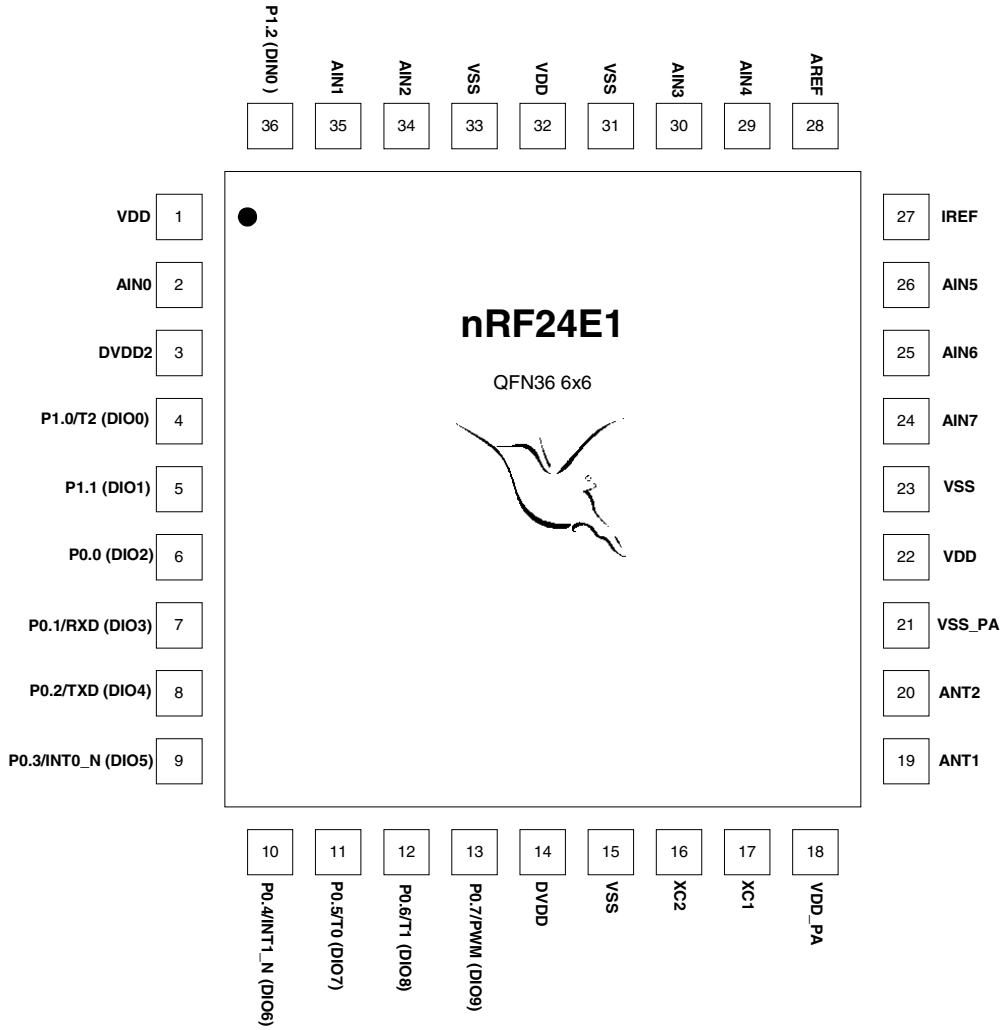


Figure 1-1 nRF24E2 block diagram plus external components

1.3 Pin Diagram



Pin	Name	Pin function	Description
1	VDD	Power	Power Supply (1.9-3.6 V DC)
2	AIN0	Analog input	ADC input 0
3	DVDD2	Regulated power	Digital Power Supply , must be connected to regulator output DVDD
4	P1.0/T2	Digital I/O	Port 1, bit 0 or T2 timer input or SPI clock or DIO0
5	P1.1	Digital I/O	Port 1, bit 1 or SPI dataout or DIO1
6	P0.0	Digital I/O	Port 0, bit 0 or EEPROM.CSN or DIO2
7	P0.1/RXD	Digital I/O	Port 0, bit 1 or UART.RXD or DIO3
8	P0.2/TXD	Digital I/O	Port 0, bit 2 or UART.TXD or DIO4
9	P0.3/INT0_N	Digital I/O	Port 0, bit 3 or INT0_N interrupt or DIO5

10	P0.4/INT1_N	Digital I/O	Port 0, bit 4 or INT1_N interrupt or DIO6
11	P0.5/T0	Digital I/O	Port 0, bit 5 or T0 timer input or DIO7
12	P0.6/T1	Digital I/O	Port 0, bit 6 or T1 timer input or DIO8
13	P0.7/PWM	Digital I/O	Port 0, bit 7 or PWM output or DIO9
14	DVDD	Regulator output	Digital voltage regulator output for de-coupling and feed to DVVD2
15	VSS	Power	Ground (0V)
16	XC2	Analog output	Crystal Pin 2
17	XC1	Analog input	Crystal Pin 1
18	VDD_PA	Regulator output	DC supply (+1.8V) to RF Power Amplifier (ANT1,ANT2) only
19	ANT1	RF	Antenna interface 1
20	ANT2	RF	Antenna interface 2
21	VSS_PA	Power	Ground (0V)
22	VDD	Power	Power Supply (1.9-3.6 V DC)
23	VSS	Power	Ground (0V)
24	AIN7	Analog input	ADC input 7
25	AIN6	Analog input	ADC input 6
26	AIN5	Analog input	ADC input 5
27	IREF	Analog input	Connection to external Bias reference resistor
28	AREF	Analog input	ADC reference voltage
29	AIN4	Analog input	ADC input 4
30	AIN3	Analog input	ADC input 3
31	VSS	Power	Ground (0V)
32	VDD	Power	Power Supply (1.9-3.6 V DC)
33	VSS	Power	Ground (0V)
34	AIN2	Analog input	ADC input 2
35	AIN1	Analog input	ADC input 1
36	P1.2	Digital input	Port 1, bit 2 or SPI datain or DIN0

Table 1-3 : nRF24E2 pin function

1.4 Glossary of Terms

Term	Description
ADC	Analog to Digital Converter
CLK	Clock
CRC	Cyclic Redundancy Check
CS	Chip Select
CE	Chip Enable
DR	Data Ready
FS	Full Scale
GFSK	Gaussian Frequency Shift Keying
GPIO	General Purpose In Out
ISM	Industrial-Scientific-Medical
kSPS	kilo Samples per Second
MCU	Microcontroller Unit
OD	Overdrive
P0 (or P1)	(8051) In / Out Port 0 (or Port 1)
PWM	Pulse Width Modulation
PWR_DWN	Power Down
PWR_UP	Power Up
RTC	Real Time Clock
RX	Receive
SFR	(8051) Special Function Register
SPI	Serial Peripheral Interface
SPS	Samples per Second
ST_BY	Standby
TX	Transmit
XTAL	Crystal (oscillator)

2 ARCHITECTURAL OVERVIEW

This section will give a brief overview of each of the blocks in the block diagram in Figure 1-1.

2.1 Microcontroller

The nRF24E2 microcontroller is instruction set compatible with the industry standard 8051. Instruction timing is slightly different from the industry standard, typically each instruction will use from 4 to 20 clock cycles, compared with 12 to 48 for the "standard". The interrupt controller is extended to support 3 additional interrupt sources; ADC, SPI, and wakeup timer. There are also 3 timers which are 8052 compatible, plus some extensions, in the microcontroller core. An 8051 compatible UART that can use timer1 or timer2 for baud rate generation in the traditional asynchronous modes is included. The CPU is equipped with 2 data pointers to facilitate easier moving of data in the XRAM area, which is a common 8051 extension. The microcontroller clock is derived directly from the crystal oscillator.

2.1.1 Memory configuration

The microcontroller has a 256 byte data ram (8052 compatible, with the upper half only addressable by register indirect addressing). A small ROM of 512 bytes, contains a bootstrap loader that is executed automatically after power on reset or if initiated by software later. The user program is normally loaded into a 4k byte RAM[1] from an external serial EEPROM by the bootstrap loader. The 4k byte RAM may also (partially) be used for data storage in some applications.

2.1.2 Boot EEPROM/FLASH

If the mask ROM option is not used, the program code for the device must be loaded from an external non-volatile memory. The default boot loader expects this to be a "generic 25320" EEPROM with SPI interface. These memories are available from several vendors with supply ranges down to 1.8V. The SPI interface uses the pins P1.2/DIN0 (EEPROM SDO), P1.0/DIO0 (EEPROM SCK), P1.1/DIO1 (EEPROM SDI) and P0.0/DIO2 (EEPROM CSN). When the boot is completed, the P1.2/DIN0, P1.0/DIO0 and P1.1/DIO1 pins may be used for other purposes such as other SPI devices or GPIO.

2.1.3 Register map

The SFR (Special Function Registers) control several of the features of the nRF24E2. Most of the nRF24E2 SFRs are identical to the standard 8051 SFRs. However, there are additional SFRs that control features that are not available in the standard 8051. The SFR map is shown in the table below. The registers with grey background are registers with industry standard 8051 behavior. Note that the function of P0 and P1 are somewhat different from the "standard" even if the conventional addresses (0x80 and 0x90) are used

[1] Optionally this 4k block of memory can be configured as 2k mask ROM and 2k RAM or 4 k mask ROM

	X000	X001	X010	X011	X100	X101	X110	X111
F8	EIP							
F0	B							
E8	EIE							
E0	ACC							
D8	EICON							
D0	PSW							
C8	T2CON		RCAP2L	RCAP2H	TL2	TH2		
C0								
B8	IP				T1_1V2	T2_1V2	DEV_ OFFSET	
B0		RSTREAS	SPI _DATA	SPI _CTRL	SPI CLK	TICK_ DV	CK_ CTRL	TEST_ MODE
A8	IE	PWM CON	PWM DUTY	REGX _MSB	REGX _LSB	REGX _CTRL		
A0	RADIO (P2)	ADCCON	ADC DATAH	ADC DATAL	ADC STATIC			
98	SCON	SBUF						
90	P1	EXIF	MPAGE		P0_DIR	P0_ALT	P1_DIR	P1_ALT
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	SPC_FNC
80	P0	SP	DPL	DPH	DPL1	DPH1	DPS	PCON

Table 2-1 : SFR Register map

2.2 PWM

The nRF24E2 has one programmable PWM output, which is the alternate function of PO.7 at pin DIO9.
The resolution of the PWM is software programmable to 6, 7 or 8 bits.
The frequency of the PWM signal is programmable via a 6 bit prescaler from the XTAL oscillator.
The duty cycle is programmable between 0% and 100% via one 8-bit register.

2.3 SPI

nRF24E2 features a simple single buffered SPI master. The 3 lines of the SPI bus (SDI, SCK and SDO) are multiplexed (by writing to register SPI_CTRL) between the GPIO pins (P1.2/DIN0, P1.0/DIO0 and P1.1/DIO1) and the RF transmitter. The SPI hardware does not generate any chip select signal. The programmer will typically use GPIO bits (from port P0) to act as chip selects for one or more external SPI devices. When the SPI interfaces the RF transmitter, the chip selects are available in an internal GPIO port, P2.

2.4 Port Logic

The device has 1 general purpose input and 10 general purpose bi-directional pins. These are by default configured as GPIO pins controlled by the ports P0 (DIO2 to DIO9) and P1 (DIO0, DIO1, DIN0) of the microcontroller.

Most of the GPIO pins can be used for multiple purposes under program control. The alternate functions include two external interrupts, UART RXD and TXD, a SPI master port, three enable/count signals for the timers and the PWM output.

2.5 Power Management

The nRF24E2 can be set into a low power down mode under program control, and also the ADC and RF subsystems can be turned on or off under program control. The CPU will stop, but all RAM's and registers maintain their values. The low power RC oscillator is running, and so are the watchdog and the RTC wakeup timer (if enabled by software). The current consumption in this mode is typically 2µA.
The device can exit the power down mode by an external pin (INT0_N or INT1_N) if enabled, by the wakeup timer if enabled or by a watchdog reset.

2.6 RTC Wakeup Timer, Watchdog and RC Oscillator

The nRF24E2 contains a low power RC oscillator which can not be disabled, so it will run continuously as long as VDD ≥ 1.8V.

RTC Wakeup Timer and Watchdog are two 16 bit programmable timers that run on the RC oscillator LP_OSC clock. The resolution of the watchdog and wakeup timer is programmable from approximately 300µs to approximately 80ms. By default the resolution is 10ms. The wakeup timer can be started and stopped by user software. The watchdog is disabled after a reset, but if activated it can not be disabled again, except by another reset

2.7 XTAL Oscillator

Both the microcontroller, ADC and RF front end run on a crystal oscillator generated clock. A range of crystals frequencies from 4 to 20 MHz may be utilised, but 16 MHz is recommended since it gives best over all performance. For details, please see Crystal Specification on page 88. The oscillator may be started and stopped as requested by software.

2.8 AD Converter

The nRF24E2 AD converter has 10 bit dynamic range and linearity with a conversion time of 48 CPU instruction cycles per 10-bit result.
The reference for the AD converter is software selectable between the AREF input and an internal 1.22V bandgap reference.

The converter has 9 inputs selectable by software. Selecting one of the inputs 0 to 7 will convert the voltage on the respective AIN0 to AIN7 pin.
Input 8 enables software to monitor the nRF24E2 supply voltage by converting an internal input that is VDD/3 with the 1.22V internal reference selected.
The AD converter is typically used in a start/stop mode. The sampling time is then under software control.
The converter is by default configured as 10 bits. For special requirements, the AD converter can be configured by software to perform 6, 8 or 12 bit conversions. The converter may also be used in differential mode with AIN0 used as inverting input and one of the other 7 external inputs used as noninverting input. In that case the conversion time can be reduced to approximately 2 µs.

2.9 Radio Transmitter

The transmitter part of the circuit has identical functionality to the transmitter part of the nRF2401 single chip RF transceiver. It is accessed through an internal parallel port and / or an internal SPI. nRF24E2 contains no receiver functions.
nRF2401 is a radio transceiver for the world wide 2.4 - 2.5 GHz ISM band. The transmitter consists of a fully integrated frequency synthesizer, a power amplifier and a modulator. Output power and frequency channels and other RF parameters are easily programmable by use of the RADIO register, SFR 0xA0. RF current consumption is only 10.5 mA in TX mode (output power -5dBm). For power saving the transmitter can be turned on / off under software control. Further information about the nRF2401 chip can be found at our website http://www.nordicsemi.no.

3 I/O PORTS

The nRF24E2 have two IO ports located at the default locations for P0 and P1 in standard 8051, but the ports are fully bi-directional CMOS and the direction of each pin is controlled by a _DIR and an _ALT bit for each bit as shown in the table below.

Pin	Default function	Alternate=1	SPI_CTRL=01
DIN0	P1.2		SPI_DI
DIO0	P1.0	T2 (timer2 input)	SPI_SCK
DIO1	P1.1		SPI_DO
DIO2	P0.0[2]	EEPROM_CSN	
DIO3	P0.1	RXD (UART)	
DIO4	P0.2	TXD (UART)	
DIO5	P0.3	INT0_N (interrupt)	
DIO6	P0.4	INT1_N (interrupt)	
DIO7	P0.5	T0 (timer0 input)	
DIO8	P0.6	T1 (timer1 input)	
DIO9	P0.7	PWM	

Table 3-1 : Port functions

3.1 I/O port behavior during RESET

During the period the internal reset is active (regardless of whether or not the clock is running), all the port pins are configured as inputs. When program execution starts, the DIO ports are still configured as inputs and the program will need to set the _ALT and/or the _DIR register for the pins that should be used as outputs.

3.2 Port 0 (P0)

P0_ALT and P0_DIR control the P0 port function in that order of priority. If the alternate function for port p0.n is set (by P0_ALT.n = 1) the pin will be input or output as required by the alternate function (UART, external interrupt, timer inputs or PWM output), except that the UART RXD direction will still depend on P0_DIR.1.

To use INT0_N or INT1_N, the corresponding alternate function must be activated, P0_ALT.3 / P0_ALT.4

When the P0_ALT.n is not set, bit ‘n’ of the port is a GPIO function with the direction controlled by P0_DIR.n.

P0.0 is always a GPIO. It will be activated by the default boot loader after reset and should be connected to the CSN of the boot flash.

[2] Reserved for use as EEPROM_CSN, works as GPIO P0.0 independent of the “Alternate setting”

Pin	Data in P0_ALT.n,P0_DIR.n							
	10		11		00		01	
P0.0 (DIO2)	P0.0	Out	P0.0	In	P0.0	Out	P0.0	In
P0.1 (DIO3)	RXD	Out	RXD	In	P0.1	Out	P0.1	In
P0.2 (DIO4)	TXD	Out	TXD	Out	P0.2	Out	P0.2	In
P0.3 (DIO5)	INT0_N	In	INT0_N	In	P0.3	Out	P0.3	In
P0.4 (DIO6)	INT1_N	In	INT1_N	In	P0.4	Out	P0.4	In
P0.5 (DIO7)	T0	In	T0	In	P0.5	Out	P0.5	In
P0.6 (DIO8)	T1	In	T1	In	P0.6	Out	P0.6	In
P0.7 (DIO9)	PWM	Out	PWM	Out	P0.7	Out	P0.7	In

Table 3-2 : Port 0 (P0) functions

Port 0 is controlled by SFR-registers 0x80, 0x94 and 0x95 listed in the table below.

Addr SFR (hex)	R/W	#bit	Init value (hex)	Name	Function
80	R/W	8	FF	P0	Port 0, pins DIO9 to DIO2
94	R/W	8	FF	P0_DIR	Direction for each bit of Port 0 0: Output, 1: Input Direction is overridden if alternate function is selected for a pin.
95	R/W	8	00	P0_ALT	Select alternate functions for each pin of P0, if corresponding bit in P0_ALT is set, as listed in Table 3-2 : Port 0 (P0) functions, P0.0 has no alternate function,as it is intended as CS for external boot flash memory. It will function as a GPIO bit regardless of P0_ALT.0

Table 3-3 : Port 0 control and data SFR-registers

3.3 Port 1 (P1 or SPI port)

The P1 port consists of only 3 pins, one of which is an hardwired input. The function is controlled by SPI_CTRL.

When SPI_CTRL is 01, the port is used as a SPI master port. The GPIO bits in port P0 may be used as chip select(s). For timing diagram, please see Figure 3-1 : SPI interface timing.

When not used as SPI port, P0_ALT.0 will force P1.0 to be the timer T2 input, P1.1 is now a GPIO. When P0_ALT.0 is 0, also P1.0 is a GPIO.

P1.2 (DIN0) is always an input.

Pin	**SPI_CTRL = 01**		**SPI_CTRL != 01**					
			P1_ALT.n = 1		**P1_ALT.n = 0**			
					P1_DIR.n = 0		**P1_DIR.n = 1**	
P1.0 (DIO0)	SCK	Out	T2	In	P1.0	In	P1.0	Out
P1.1 (DIO1)	SDO	Out	P1.1	In[3]	P1.1	In	P1.1	Out
P1.2 (DIN0)	SDI	In	P1.2	In	P1.2	In	P1.2	In

Table 3-4 : Port 1 (P1) functions

Port 1 is controlled by SFR-registers 0x90, 0x96 and 0x97, and only the 3 lower bits of the registers are used.

Addr SFR (hex)	**R/W**	**#bit**	**Init value (hex)**	**Name**	**Function**
90	R/W	3	FF	P1	Port 1, pins DIN0, DIO1 and DIO0
96	R/W	3	FF	P1_DIR	Direction for each bit of Port 1 0: Output, 1: Input Direction is overridden if alternate function is selected for a pin, or if SPI_CTRL=01. bit0, DIN0 is always input.
97	R/W	3	00	P1_ALT	Select alternate functions for each pin of P1 if corresponding bit in P1_ALT is set, as listed in Table 3-4 : Port 1 (P1) functions If SPI_CTRL is '01', the P1 port is used as SPI master data and clock : 2 -> SDI – input to nRF24E2 from slave 1 -> SDO – output from nRF24E2 to slave 0 -> SCK – output from nRF24E2 to slave

Table 3-5 : Port 1 control and data SFR-registers

[3] P1.1 is actually under control of P1_DIR.1 even when P1_ALT.1 is 1, since there is no alternate function for this pin.

P1 may also be configured as a SPI master port , and is then controlled by the 3 SFR registers 0xB2, 0xB3, 0xB4 as shown in the table below.

Addr SFR (hex)	R/ W	#bit	Init (hex)	Name	Function
B2	R/W	8	0	SPI_DATA	SPI data input/output
B3	R/W	2	0	SPI_CTRL	00 -> SPI not used no clock generated 01 -> SPI connected to port P1 (as for booting) another GPIO must be used as chip select (see also Table 3-4 : Port 1 (P1) functions) 10 -> SPI connected to RADIO transmitter for TX or for configuration (see Table 4-2 : RADIO register) 11 -> reserved, do not use
B4	R/W	2	0	SPICLK	Divider factor from CPU clock to SPI clock 00: 1/8 of CPU clock frequency 01: 1/16 of CPU clock frequency 10: 1/32 of CPU clock frequency 11: 1/64 of CPU clock frequency The CPU clock is the oscillator generated clock described in Crystal Specification page 88

Table 3-6 : SPI control and data SFR-registers

3.3.1 SPI interface operation

Whenever SPI_DATA register is written to, a sequence of 8 pulses is started on SCK, and the 8 bits of SPI_DATA register are clocked out on SDO with msb first. Simultaneously 8 bits from SDI are clocked into SPI_DATA register. Ouput data is shifted on negedge SCK, and input data is read on posedge SCK. This is illustrated in Figure 3-1 : SPI interface timing. When the 8 bits are done, SPI_READY interrupt (EXIF.5) goes active, and the 8 bits from SDI may be read from SPI_DATA register. The EXIF.5 bit must be cleared before starting another SPI transaction by writing to SPI_DATA register again.
SCK, SDO and SDI may be external pins or internal signals, as defined in SPI_CTRL register.

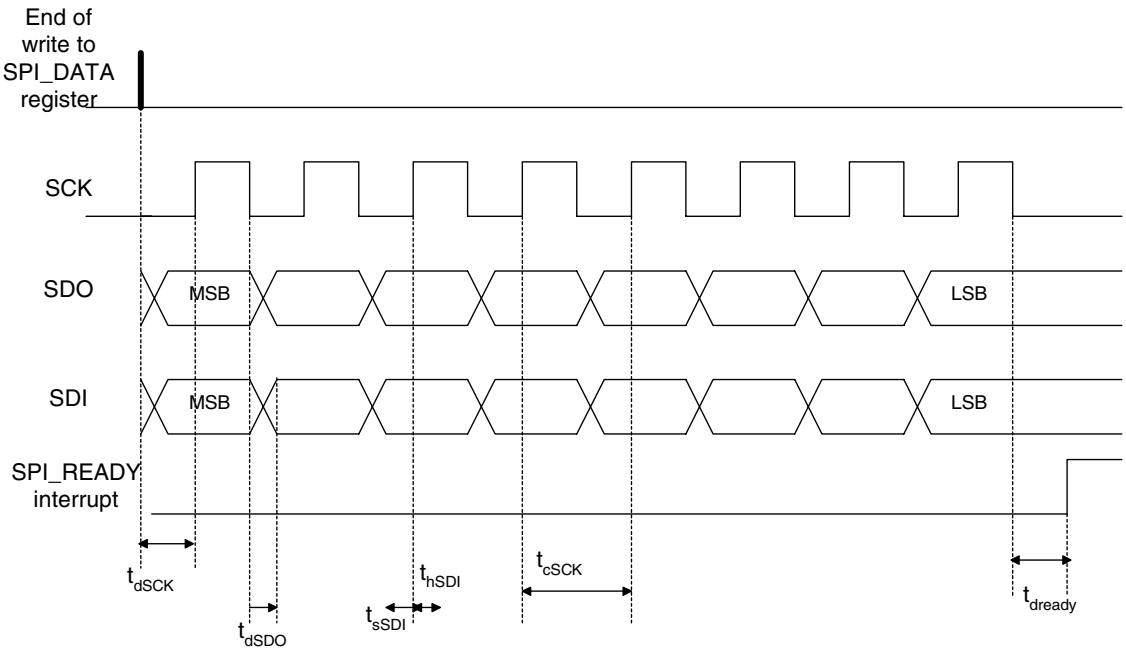


Figure 3-1 : SPI interface timing

t_{cSCK} : SCK cycle time, as defined by SPICLK register.

t_{dSCK} : time from writing to SPI_DATA register to first SCK pulse,

$t_{dSCK} = t_{cSCK} / 2$

t_{dSDO} : delay from negedge SCK to new SDO output data, may vary from -40ns to 40ns

t_{sSDI} : SDI setup time to posedge SCK, $t_{sSDI} > 45$ns.

t_{hSDI} : SDI hold time to posedge SCK, $t_{hSDI} > 0$ns.

t_{dready} : time from last SCK pulse to SPI_READY interrupt goes active

$t_{dready} = 7$ CPU clock cycles

Note that the above delay, setup and hold time numbers only apply for SPI connected to Port 1; as when SPI is connected to the Radio, SCK,SDO,SDI are all internal signals, not visible to the user.

Minimum time between two consecutive SPI transactions will be :

$8.5\ t_{cSCK} + t_{dready} + t_{SW}$

where t_{SW} is the time taken by the software to process SPI_READY interrupt, and write to SPI_DATA register.

4 nRF2401 2.4GHz TRANSMITTER SUBSYSTEM

4.1 RADIO port (Port 2)

The transmitter is controlled by the RADIO port. The RADIO port uses the address normally used by port P2 in standard 8051. However since the radio transmitter is on chip, the port is not bi-directional. The power on default values in the port "latch" also differs from traditional 8051 to match the requirements of the radio transmitter subsystem.
Operation of the transmitter is controlled by SFR registers RADIO and SPI_CTRL:

Addr SFR (hex)	**R/W**	**#bit**	**Init value (hex)**	**Name**	**Function**
A0	R/W	8	80	RADIO	General purpose IO for interface to nRF2401 radio transmitter subsystem
B3	R/W	2	0	SPI_CTRL	00 -> SPI not used 01 -> SPI connected to port P1 (boot) 10 -> SPI connected to nRF2401 TX 11 -> reserved, do not use

Table 4-1 : nRF2401 2.4GHz transmitter subsystem control registers - SFR 0xA0 and 0xB3

The bits of the RADIO register correspond to similar pins of the nRF2401 single chip, as shown in Table 4-2 : RADIO register . In the documentation the pin names are used, so please note that setting or reading any of these nRF2401 pins, means to write or read the RADIO SFR register accordingly. Please also note that in the transmitter documentation the notation MCU means the onchip 8051 compatible microcontroller.

RADIO register bit	corresponding pin name on single chip nRF2401 2.4GHz Transceiver
Read : This is a write only register, if read, all bits will be undefined	
Write :	
7: PWR_UP, power on radio	PWR_UP
6: CE, Activate TX mode	CE
5: Not used	CLK2
4: Not used	
3: CS, Chip select configuration mode	CS
2: Not used	
1: CLK1, clock for data input	CLK1
0: DATA, configuration or TX data input	DATA

Table 4-2 : RADIO register - SFR 0xA0, default initial data value is 0x80.

Note : Some of the pins are overridden when SPI_CTRL=1x, see Table 4-3 : Transmitter SPI interface.

4.1.1 Controlling the transmitter via SPI interface.

It is more convenient to use the built-in SPI interface to do the most common transmitter operations as RF configuration and ShockBurst™ TX. Please see Table 3-6 : SPI control and data SFR-registers for use of SPI interface. The radio port will be connected in different ways to the SPI hardware when SPI_CTRL is '1x'. When SPI_CTRL is '0x', all radio pins are connected directly to their respective port pins.

SPI signal	SPI_CTRL=10 (binary)
CS (active high)	RADIO_wr.6 (CE) for ShockBurst™ RADIO_wr.3 (CS) for Configuration
SCK	nRF2401/CLK1
SDI	not used
SDO	nRF2401/DATA

Table 4-3 : Transmitter SPI interface.

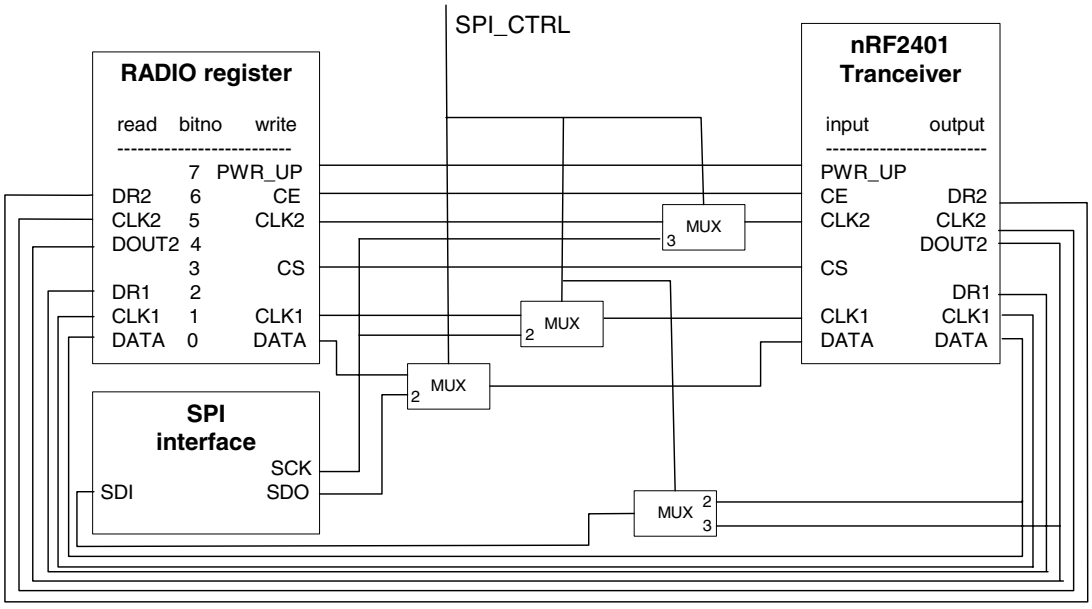


Figure 4-1 : Transmitter interface

4.1.2 RADIO port behavior during RESET

During the period the internal reset is active (regardless of whether or not the clock is running), the RADIO outputs that control the nRF2401 transmitter subsystem are forced to their respective default values (RADIO.3=0 (CS), RADIO.6=0 (CE)

RADIO.7=1 (PWR_UP)). When program execution starts, these ports will remain at those default levels until the programmer actively changes them by writing to the RADIO register.

4.2 Modes of operation

4.2.1 Overview

The transmitter subsystem can be set in the following main modes depending on three control pins:

Mode	PWR_UP	CE	CS
Active (TX)	1	1	0
Configuration	1	0	1
Stand by	1	0	0
Power down	0	X	X

Table 4-4 transmitter subsystem main modes

4.2.2 Active modes

The transmitter subsystem has two active (TX) modes:

- ShockBurst™
- Direct Mode (not supported by nRF24E2)

The device functionality in these modes is decided by the content of a configuration word. This configuration word is presented in the configuration section. Please note that Direct mode is not supported, as this will require a more powerful CPU than 8051.

4.2.3 ShockBurst™

The ShockBurst™ technology uses on-chip FIFO to clock in data at a low data rate and transmit at a very high rate thus enabling extremely power reduction.
When operating the transmitter subsystem in ShockBurst™, you gain access to the high data rates (1 Mbps) offered by the 2.4 GHz band without the need of a costly, high-speed microcontroller (MCU) for data processing.
By putting all high speed signal processing related to RF protocol on-chip, the nRF24E2 offers the following benefits:

- Highly reduced current consumption
- Lower system cost (facilitates use of less expensive microcontroller)
- Greatly reduced risk of ‘on-air’ collisions due to short transmission time

The transmitter subsystem can be programmed using a simple 3-wire interface where the data rate is decided by the speed of the CPU.

By allowing the digital part of the application to run at low speed while maximizing the data rate on the RF link, the ShockBurst™ mode reduces the average current consumption in applications considerably.

4.2.3.1 ShockBurst™ principle

When the transmitter subsystem is configured in ShockBurst™, TX operation is conducted in the following way (10 kbps for the example only).

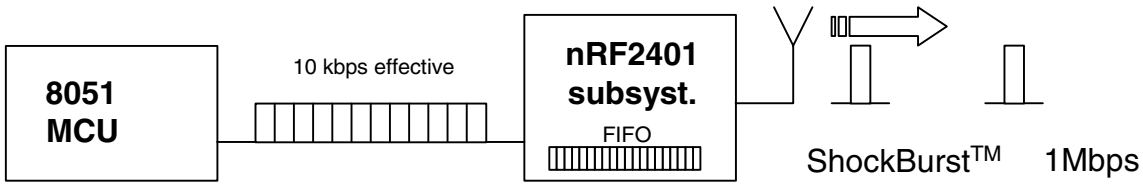


Figure 4-2Clocking in data with CPU and sending with ShockBurst™ technology

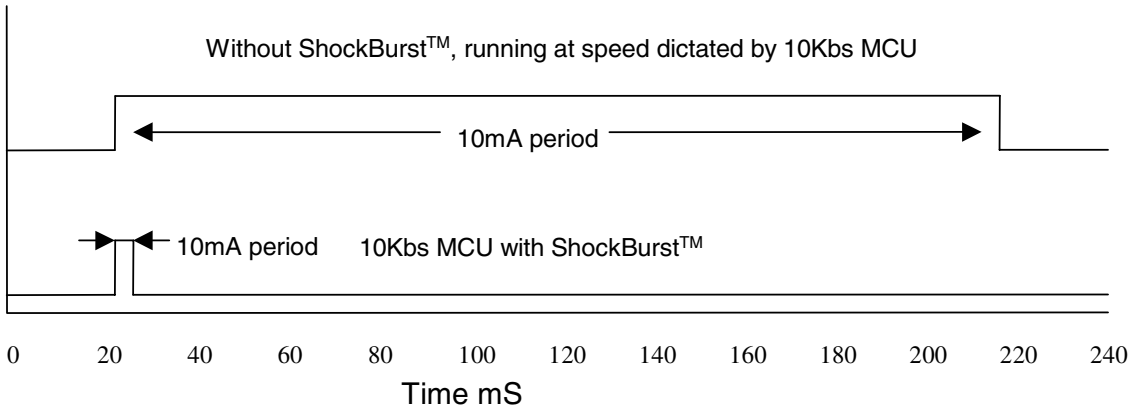


Figure 4-3 RF Current consumption with & without ShockBurst™ technology

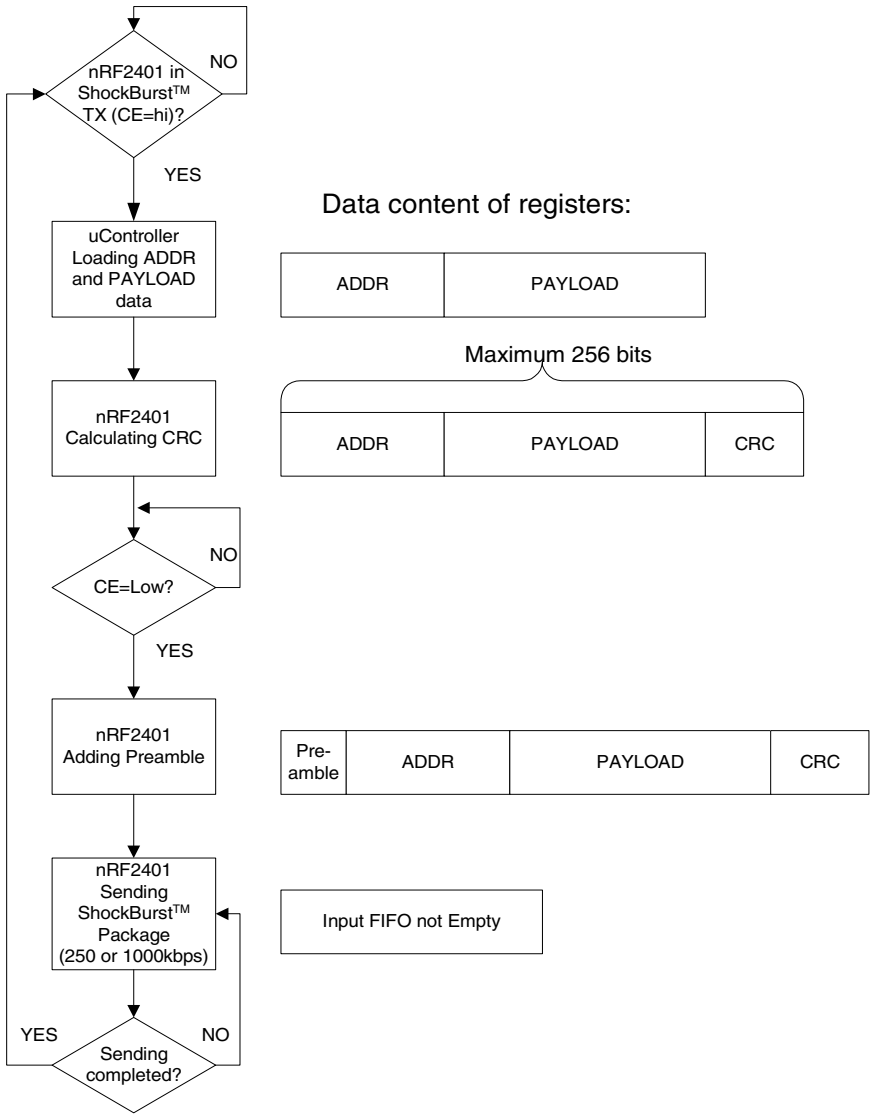


Figure 4-4 Flow Chart ShockBurst™ Transmit of transmitter subsystem

4.2.3.2 ShockBurst™ Transmit:

4.2.3.2.1 CPU interface pins: CE, CLK1, DATA

1. When the application CPU has data to send, set CE high. This activates nRF2401 on-board data processing.
2. The address of the receiving node (RX address) and payload data is clocked into the transmitter subsystem. The application protocol or CPU sets the speed <1Mbps (ex: 10kbps).
3. CPU sets CE low, this activates a ShockBurst™ transmission.
4. ShockBurst™:
   - RF front end is powered up
   - RF package is completed (preamble added, CRC calculated)
   - Data is transmitted at high speed (250 kbps or 1 Mbps configured by user).
   - transmitter subsystem returns to stand by when finished

4.3 Device configuration

All configuration of the transmitter subsystem is done via a 3-wire interface interface (CS, CLK1 and DATA) to a single configuration register. The configuration word can be up to 18 bits long. The configuration bits (DATA) must be clocked (by CLK1) into transmitter subsystem, with msb first, while CS=1. No more than 18 bits may be downloaded.

4.3.1 Configuration for ShockBurst™ operation

The configuration word in ShockBurst™ enables the transmitter subsystem to handle the RF protocol. Once the protocol is completed and loaded into transmitter subsystem only one byte, bit[7:0], needs to be updated during actual operation.

The configuration blocks dedicated to ShockBurst™ is as follows:

- CRC: Enables on-chip CRC generation and de-coding.

NOTE:
The CPU must generate an address and a payload section that fits the configuration of the nRF24x1 subsystem that is to receive the data.
When using the transmitter subsystem on-chip CRC feature ensures that CRC is enabled and uses the same length for both the TX and RX devices.

PRE-AMBLE	ADDRESS	PAYLOAD	CRC

Figure 4-5Data packet set-up

4.3.2 Configuration for Direct Mode operation

For direct mode operation only the two first bytes (bit[15:0]) of the configuring word is relevant.

4.3.3 Configuration Word overview

	Bit position	Number of bits	Name	Function
ShockBurst™ configuration	> 17		reserved	must not be written
	17	1	CRC_L	8 or 16 bit CRC
	16	1	CRC_EN	Enable on-chip CRC generation.
General device configuration	15	1	reserved, should be zero	
	14	1	CM	Communication mode (Direct or ShockBurst™)
	13	1	RFDR_SB	RF data rate (1Mbps requires 16MHz crystal)
	12:10	3	XO_F	Crystal frequency
	9:8	2	RF_PWR	RF output power
	7:1	7	RF_CH#	Frequency channel
	0	1	reserved, must be zero	

Table 4-5 Table of configuration words.

The configuration word is shifted in MSB first on positive CLK1 edges. New configuration is enabled on the falling edge of CS. Not more than maximum 18 bits must be shifted.

NOTE.
On the falling edge of CS, the transmitter subsystem updates the number of bits actually shifted in during the last configuration.

4.3.4 Configuration Word Detailed Description

The following describes the function of the 24 bits (bit 23 = MSB) that is used to configure the transmitter subsystem.
General Device Configuration: bit[15:0]
ShockBurst™ Configuration: bit[17:16]

CRC		
D17	D16	
CRC Mode 1 = 16bit, 0 = 8bit	CRC 1 = enable; 0 = disable	
0	1	Default

RF-Programming															LSB	
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
reserved	BUF	OD	XO Frequency			RF Power		Channel selection							reserved	
0	0	0	0	1	1	1	1	0	0	0	0	0	1	0	0	Default

Table 4-6 Configuration data word

The MSB bit should be loaded first into the configuration register.
Default configuration word: h1.0F04.