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nRF24L01+

Single Chip 2.4GHz Transceiver

Product Specification v1.0

Key Features

- Worldwide 2.4GHz ISM band operation
- 250kbps, 1Mbps and 2Mbps on air data rates
- Ultra low power operation
- 11.3mA TX at 0dBm output power
- 13.5mA RX at 2Mbps air data rate
- 900nA in power down
- 26µA in standby-I
- On chip voltage regulator
- 1.9 to 3.6V supply range
- Enhanced ShockBurst™
- Automatic packet handling
- Auto packet transaction handling
- 6 data pipe MultiCeiver™
- Drop-in compatibility with nRF24L01
- On-air compatible in 250kbps and 1Mbps with nRF2401A, nRF2402, nRF24E1 and nRF24E2
- Low cost BOM
- ±60ppm 16MHz crystal
- 5V tolerant inputs
- Compact 20-pin 4x4mm QFN package

Applications

- Wireless PC Peripherals
- Mouse, keyboards and remotes
- 3-in-1 desktop bundles
- Advanced Media center remote controls
- VoIP headsets
- Game controllers
- Sports watches and sensors
- RF remote controls for consumer electronics
- Home and commercial automation
- Ultra low power sensor networks
- Active RFID
- Asset tracking systems
- Toys

September 2008

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Objective product specification	This product specification contains target specifications for product development.
Preliminary product specification	This product specification contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
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Contact details

Visit www.nordicsemi.no for Nordic Semiconductor sales offices and distributors worldwide

Main office:

Otto Nielsens vei 12
7004 Trondheim
Phone: +47 72 89 89 00
Fax: +47 72 89 89 89
www.nordicsemi.no

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Writing Conventions

This product specification follows a set of typographic rules that makes the document consistent and easy to read. The following writing conventions are used:

- Commands, bit state conditions, and register names are written in `Courier`.
- Pin names and pin signal conditions are written in **`Courier bold`**.
- Cross references are underlined and highlighted in blue.

Revision History

Date	Version	Description
September 2008	1.0	

Attention!

Observe precaution for handling Electrostatic Sensitive Device.

HBM (Human Body Model) ≥ 1Kv
MM (Machine Model) ≥ 200V

Contents

1 Introduction

The nRF24L01+ is a single chip 2.4GHz transceiver with an embedded baseband protocol engine (Enhanced ShockBurst™), suitable for ultra low power wireless applications. The nRF24L01+ is designed for operation in the world wide ISM frequency band at 2.400 - 2.4835GHz.

To design a radio system with the nRF24L01+, you simply need an MCU (microcontroller) and a few external passive components.

You can operate and configure the nRF24L01+ through a Serial Peripheral Interface (SPI). The register map, which is accessible through the SPI, contains all configuration registers in the nRF24L01+ and is accessible in all operation modes of the chip.

The embedded baseband protocol engine (Enhanced ShockBurst™) is based on packet communication and supports various modes from manual operation to advanced autonomous protocol operation. Internal FIFOs ensure a smooth data flow between the radio front end and the system's MCU. Enhanced ShockBurst™ reduces system cost by handling all the high speed link layer operations.

The radio front end uses GFSK modulation. It has user configurable parameters like frequency channel, output power and air data rate. nRF24L01+ supports an air data rate of 250 kbps, 1 Mbps and 2Mbps. The high air data rate combined with two power saving modes make the nRF24L01+ very suitable for ultra low power designs.

nRF24L01+ is drop-in compatible with nRF24L01 and on-air compatible with nRF2401A, nRF2402, nRF24E1 and nRF24E2. Intermodulation and wideband blocking values in nRF24L01+ are much improved in comparison to the nRF24L01 and the addition of internal filtering to nRF24L01+ has improved the margins for meeting RF regulatory standards.

Internal voltage regulators ensure a high Power Supply Rejection Ratio (PSRR) and a wide power supply range.

1.1 Features

Features of the nRF24L01+ include:

- Radio
  - Worldwide 2.4GHz ISM band operation
  - 126 RF channels
  - Common RX and TX interface
  - GFSK modulation
  - 250kbps, 1 and 2Mbps air data rate
  - 1MHz non-overlapping channel spacing at 1Mbps
  - 2MHz non-overlapping channel spacing at 2Mbps
- Transmitter
  - Programmable output power: 0, -6, -12 or -18dBm
  - 11.3mA at 0dBm output power
- Receiver
  - Fast AGC for improved dynamic range
  - Integrated channel filters
  - 13.5mA at 2Mbps
  - -82dBm sensitivity at 2Mbps
  - -85dBm sensitivity at 1Mbps
  - -94dBm sensitivity at 250kbps
- RF Synthesizer
  - Fully integrated synthesizer
  - No external loop filer, VCO varactor diode or resonator
  - Accepts low cost ±60ppm 16MHz crystal
- Enhanced ShockBurst™
  - 1 to 32 bytes dynamic payload length
  - Automatic packet handling
  - Auto packet transaction handling
  - 6 data pipe MultiCeiver™ for 1:6 star networks
- Power Management
  - Integrated voltage regulator
  - 1.9 to 3.6V supply range
  - Idle modes with fast start-up times for advanced power management
  - 26µA Standby-I mode, 900nA power down mode
  - Max 1.5ms start-up from power down mode
  - Max 130us start-up from standby-I mode
- Host Interface
  - 4-pin hardware SPI
  - Max 10Mbps
  - 3 separate 32 bytes TX and RX FIFOs
  - 5V tolerant inputs
- Compact 20-pin 4x4mm QFN package

1.2 Block diagram

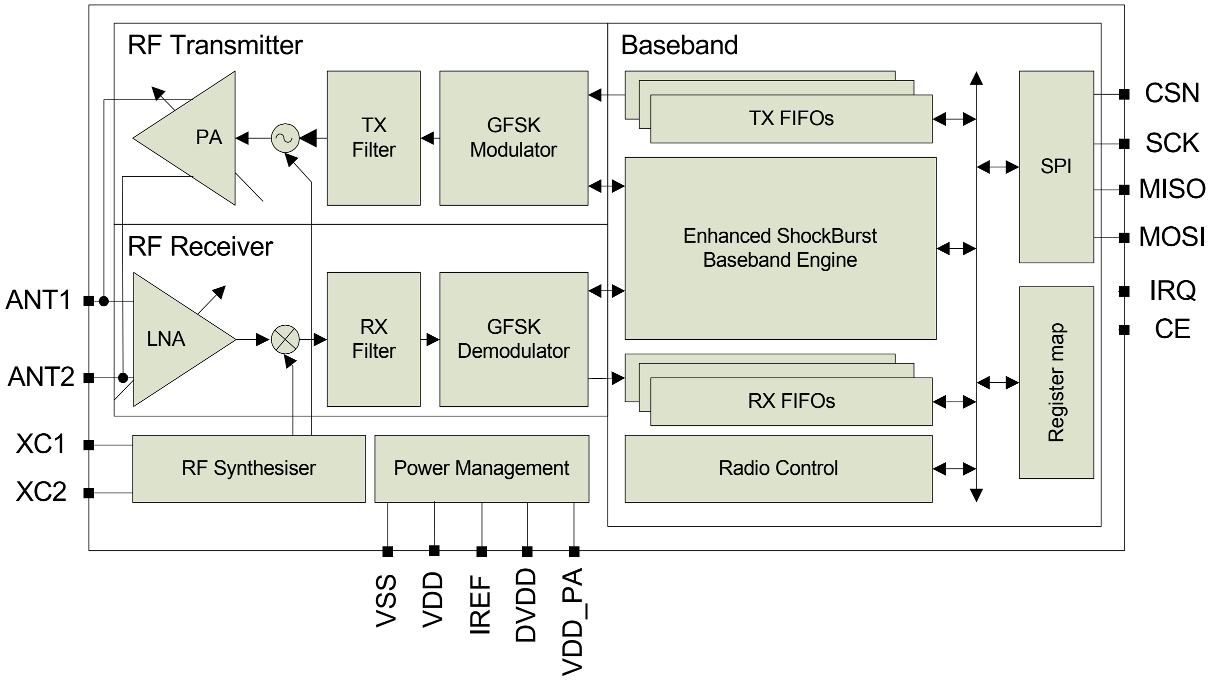

Figure 1. nRF24L01+ block diagram

2 Pin Information

2.1 Pin assignment

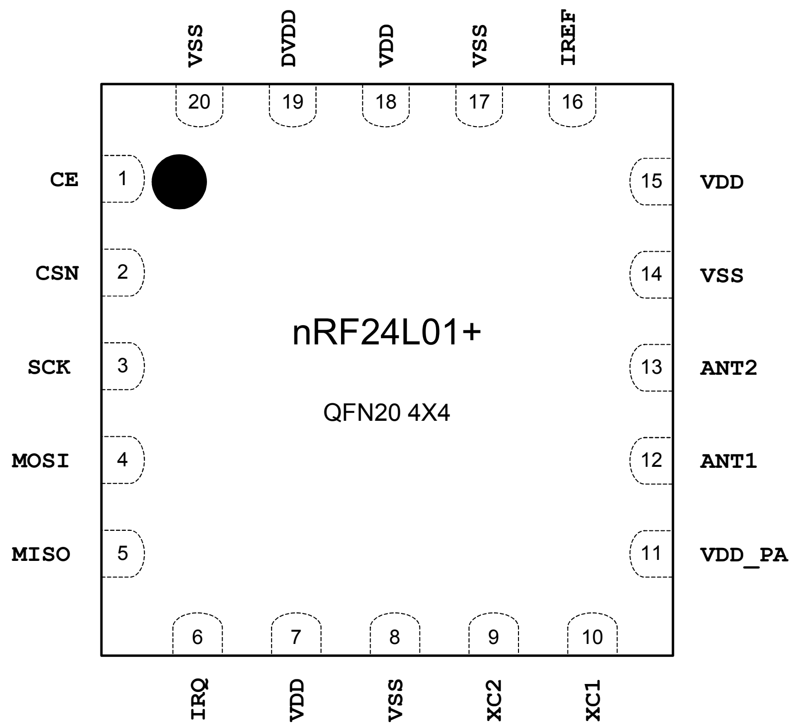

Figure 2. nRF24L01+ pin assignment (top view) for the QFN20 4x4 package

2.2 Pin functions

Pin	Name	Pin function	Description
1	**CE**	Digital Input	Chip Enable Activates RX or TX mode
2	**CSN**	Digital Input	SPI Chip Select
3	**SCK**	Digital Input	SPI Clock
4	**MOSI**	Digital Input	SPI Slave Data Input
5	**MISO**	Digital Output	SPI Slave Data Output, with tri-state option
6	**IRQ**	Digital Output	Maskable interrupt pin. Active low
7	**VDD**	Power	Power Supply (+1.9V - +3.6V DC)
8	**VSS**	Power	Ground (0V)
9	**XC2**	Analog Output	Crystal Pin 2
10	**XC1**	Analog Input	Crystal Pin 1
11	**VDD_PA**	Power Output	Power Supply Output (+1.8V) for the internal nRF24L01+ Power Amplifier. Must be connected to **ANT1** and **ANT2** as shown in Figure 32.
12	**ANT1**	RF	Antenna interface 1
13	**ANT2**	RF	Antenna interface 2
14	**VSS**	Power	Ground (0V)
15	**VDD**	Power	Power Supply (+1.9V - +3.6V DC)
16	**IREF**	Analog Input	Reference current. Connect a 22kΩ resistor to ground. See Figure 32.
17	**VSS**	Power	Ground (0V)
18	**VDD**	Power	Power Supply (+1.9V - +3.6V DC)
19	**DVDD**	Power Output	Internal digital supply output for de-coupling purposes. See Figure 32.
20	**VSS**	Power	Ground (0V)

Table 1. nRF24L01+ pin function

3 Absolute maximum ratings

Note: Exceeding one or more of the limiting values may cause permanent damage to nRF24L01+.

Operating conditions	Minimum	Maximum	Units
Supply voltages			
VDD	-0.3	3.6	V
VSS		0	V
Input voltage			
V_I	-0.3	5.25	V
Output voltage			
V_O	VSS to VDD	VSS to VDD	
Total Power Dissipation			
P_D (T_A=85°C)		60	mW
Temperatures			
Operating Temperature	-40	+85	°C
Storage Temperature	-40	+125	°C

Table 2. Absolute maximum ratings

4 Operating conditions

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
VDD	Supply voltage		1.9	3.0	3.6	V
VDD	Supply voltage if input signals >3.6V		2.7	3.0	3.3	V
TEMP	Operating Temperature		-40	+27	+85	ºC

Table 3. Operating conditions

5 Electrical specifications

Conditions: VDD = +3V, VSS = 0V, T_A = - 40ºC to + 85ºC

5.1 Power consumption

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
	Idle modes					
I_{VDD_PD}	Supply current in power down			900		nA
I_{VDD_ST1}	Supply current in standby-I mode	a		26		µA
I_{VDD_ST2}	Supply current in standby-II mode			320		µA
I_{VDD_SU}	Average current during 1.5ms crystal oscillator startup			400		µA
	Transmit					
I_{VDD_TX0}	Supply current @ 0dBm output power	b		11.3		mA
I_{VDD_TX6}	Supply current @ -6dBm output power	b		9.0		mA
I_{VDD_TX12}	Supply current @ -12dBm output power	b		7.5		mA
I_{VDD_TX18}	Supply current @ -18dBm output power	b		7.0		mA
I_{VDD_AVG}	Average Supply current @ -6dBm output power, ShockBurst™	c		0.12		mA
I_{VDD_TXS}	Average current during TX settling	d		8.0		mA
	Receive					
I_{VDD_2M}	Supply current 2Mbps			13.5		mA
I_{VDD_1M}	Supply current 1Mbps			13.1		mA
I_{VDD_250}	Supply current 250kbps			12.6		mA
I_{VDD_RXS}	Average current during RX settling	e		8.9		mA

a. This current is for a 12pF crystal. Current when using external clock is dependent on signal swing.
b. Antenna load impedance = 15Ω+j88Ω..
c. Antenna load impedance = 15Ω+j88Ω. Average data rate 10kbps and max. payload length packets.
d. Average current consumption during TX startup (130µs) and when changing mode from RX to TX (130µs).
e. Average current consumption during RX startup (130µs) and when changing mode from TX to RX (130µs).

Table 4. Power consumption

5.2 General RF conditions

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
f_{OP}	Operating frequency	a	2400		2525	MHz
PLL_{res}	PLL Programming resolution			1		MHz
f_{XTAL}	Crystal frequency			16		MHz
Δf_{250}	Frequency deviation @ 250kbps			±160		kHz
Δf_{1M}	Frequency deviation @ 1Mbps			±160		kHz
Δf_{2M}	Frequency deviation @ 2Mbps			±320		kHz
R_{GFSK}	Air Data rate	b	250		2000	kbps
$F_{CHANNEL\ 1M}$	Non-overlapping channel spacing @ 250kbps/ 1Mbps	c		1		MHz
$F_{CHANNEL\ 2M}$	Non-overlapping channel spacing @ 2Mbps	c		2		MHz

a. Regulatory standards determine the band range you can use.
b. Data rate in each burst on-air
c. The minimum channel spacing is 1MHz

Table 5. General RF conditions

5.3 Transmitter operation

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
P_{RF}	Maximum Output Power	a		0	+4	dBm
P_{RFC}	RF Power Control Range		16	18	20	dB
P_{RFCR}	RF Power Accuracy				±4	dB
P_{BW2}	20dB Bandwidth for Modulated Carrier (2Mbps)			1800	2000	kHz
P_{BW1}	20dB Bandwidth for Modulated Carrier (1Mbps)			900	1000	kHz
P_{BW250}	20dB Bandwidth for Modulated Carrier (250kbps)			700	800	kHz
$P_{RF1.2}$	1st Adjacent Channel Transmit Power 2MHz (2Mbps)				-20	dBc
$P_{RF2.2}$	2nd Adjacent Channel Transmit Power 4MHz (2Mbps)				-50	dBc
$P_{RF1.1}$	1st Adjacent Channel Transmit Power 1MHz (1Mbps)				-20	dBc
$P_{RF2.1}$	2nd Adjacent Channel Transmit Power 2MHz (1Mbps)				-45	dBc
$P_{RF1.250}$	1st Adjacent Channel Transmit Power 1MHz (250kbps)				-30	dBc
$P_{RF2.250}$	2nd Adjacent Channel Transmit Power 2MHz (250kbps)				-45	dBc

a. Antenna load impedance = 15Ω+j88Ω

Table 6. Transmitter operation

5.4 Receiver operation

Datarate	Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
	RX_{max}	Maximum received signal at <0.1% BER			0		dBm
2Mbps	RX_{SENS}	Sensitivity (0.1%BER) @2Mbps			-82		dBm
1Mbps	RX_{SENS}	Sensitivity (0.1%BER) @1Mbps			-85		dBm
250kbps	RX_{SENS}	Sensitivity (0.1%BER) @250kbps			-94		dBm

Table 7. RX Sensitivity

Datarate	Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
2Mbps	C/I_{CO}	C/I Co-channel			7		dBc
	C/I_{1ST}	1st ACS (Adjacent Channel Selectivity) C/I 2MHz			3		dBc
	C/I_{2ND}	2nd ACS C/I 4MHz			-17		dBc
	C/I_{3RD}	3rd ACS C/I 6MHz			-21		dBc
	C/I_{Nth}	Nth ACS C/I, f_i > 12MHz			-40		dBc
	C/I_{Nth}	Nth ACS C/I, f_i > 36MHz	a		-48		dBc
1Mbps	C/I_{CO}	C/I Co-channel			9		dBc
	C/I_{1ST}	1st ACS C/I 1MHz			8		dBc
	C/I_{2ND}	2nd ACS C/I 2MHz			-20		dBc
	C/I_{3RD}	3rd ACS C/I 3MHz			-30		dBc
	C/I_{Nth}	Nth ACS C/I, f_i > 6MHz			-40		dBc
	C/I_{Nth}	Nth ACS C/I, f_i > 25MHz	a		-47		dBc
250kbps	C/I_{CO}	C/I Co-channel			12		dBc
	C/I_{1ST}	1st ACS C/I 1MHz			-12		dBc
	C/I_{2ND}	2nd ACS C/I 2MHz			-33		dBc
	C/I_{3RD}	3rd ACS C/I 3MHz			-38		dBc
	C/I_{Nth}	Nth ACS C/I, f_i > 6MHz			-50		dBc
	C/I_{Nth}	Nth ACS C/I, f_i > 25MHz	a		-60		dBc

a. **Narrow Band (In Band) Blocking measurements:**
0 to ±40MHz; 1MHz step size
For Interferer frequency offsets n*2*fxtal, blocking performance is degraded by approximately 5dB compared to adjacent figures.

Table 8. RX selectivity according to ETSI EN 300 440-1 V1.3.1 (2001-09) page 27

Datarate	Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
2Mbps	C/I_{CO}	C/I Co-channel (Modulated carrier)			11		dBc
	C/I_{1ST}	1st ACS C/I 2MHz			4		dBc
	C/I_{2ND}	2nd ACS C/I 4MHz			-18		dBc
	C/I_{3RD}	3rd ACS C/I 6MHz			-24		dBc
	C/I_{Nth}	Nth ACS C/I, f_i > 12MHz			-40		dBc
	C/I_{Nth}	Nth ACS C/I, f_i > 36MHz	a		-48		dBc
1Mbps	C/I_{CO}	C/I Co-channel			12		dBc
	C/I_{1ST}	1st ACS C/I 1MHz			8		dBc
	C/I_{2ND}	2nd ACS C/I 2MHz			-21		dBc
	C/I_{3RD}	3rd ACS C/I 3MHz			-30		dBc
	C/I_{Nth}	Nth ACS C/I, f_i > 6MHz			-40		dBc
	C/I_{Nth}	Nth ACS C/I, f_i > 25MHz	a		-50		dBc
250kbps	C/I_{CO}	C/I Co-channel			7		dBc
	C/I_{1ST}	1st ACS C/I 1MHz			-12		dBc
	C/I_{2ND}	2nd ACS C/I 2MHz			-34		dBc
	C/I_{3RD}	3rd ACS C/I 3MHz			-39		dBc
	C/I_{Nth}	Nth ACS C/I, f_i >6MHz			-50		dBc
	C/I_{Nth}	Nth ACS C/I, f_i >25MHz	a		-60		dBc

a. **Narrow Band (In Band) Blocking measurements:**
0 to ±40MHz; 1MHz step size
Wide Band Blocking measurements:
30MHz to 2000MHz; 10MHz step size
2000MHz to 2399MHz; 3MHz step size
2484MHz to 3000MHz; 3MHz step size
3GHz to 12.75GHz; 25MHz step size
Wanted signal for wideband blocking measurements:
-67dBm in 1Mbps and 2Mbps mode
-77dBm in 250kbps mode
For Interferer frequency offsets n*2*fxtal, blocking performance are degraded by approximately 5dB compared to adjacent figures.
If the wanted signal is 3dB or more above the sensitivity level then, the carrier/interferer ratio is independent of the wanted signal level for a given frequency offset.

Table 9. RX selectivity with nRF24L01+ equal modulation on interfering signal. Measured using Pin = -67dBm for wanted signal.

Datarate	Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
2Mbps	P_IM(6	Input power of IM interferers at 6 and 12MHz offset from wanted signal			-42		dBm
	P_IM(8)	Input power of IM interferers at 8 and 16MHz offset from wanted signal			-38		dBm
	P_IM(10)	Input power of IM interferers at 10 and 20MHz offset from wanted signal			-37		dBm
1Mbps	P_IM(3)	Input power of IM interferers at 3 and 6MHz offset from wanted signal			-36		dBm
	P_IM(4)	Input power of IM interferers at 4 and 8MHz offset from wanted signal			-36		dBm
	P_IM(5)	Input power of IM interferers at 5 and 10MHz offset from wanted signal			-36		dBm
250kbps	P_IM(3)	Input power of IM interferers at 3 and 6MHz offset from wanted signal			-36		dBm
	P_IM(4)	Input power of IM interferers at 4 and 8MHz offset from wanted signal			-36		dBm
	P_IM(5)	Input power of IM interferers at 5 and 10MHz offset from wanted signal			-36		dBm

Note: Wanted signal level at Pin = -64 dBm. Two interferers with equal input power are used. The interferer closest in frequency is unmodulated, the other interferer is modulated equal with the wanted signal. The input power of interferers where the sensitivity equals BER = 0.1% is presented.

Table 10. RX intermodulation test performed according to Bluetooth Specification version 2.0

5.5 Crystal specifications

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
Fxo	Crystal Frequency			16		MHz
ΔF	Tolerance	a b			±60	ppm
C_0	Equivalent parallel capacitance			1.5	7.0	pF
Ls	Equivalent serial inductance	c		30		mH
C_L	Load capacitance		8	12	16	pF
ESR	Equivalent Series Resistance				100	Ω

a. Frequency accuracy including; tolerance at 25°C, temperature drift, aging and crystal loading.
b. Frequency regulations in certain regions set tighter requirements for frequency tolerance (For example, Japan and South Korea specify max. +/- 50ppm).
c. Startup time from power down to standby mode is dependant on the Ls parameter. See Table 16. on page 24 for details.

Table 11. Crystal specifications

The crystal oscillator startup time is proportional to the crystal equivalent inductance. The trend in crystal design is to reduce the physical outline. An effect of a small outline is an increase in equivalent serial inductance Ls, which gives a longer startup time. The maximum crystal oscillator startup time, Tpd2stby = 1.5 ms, is set using a crystal with equivalent serial inductance of maximum 30mH.

An application specific worst case startup time can be calculated as :

Tpd2stby= Ls/30mH *1.5ms if Ls exceeds 30mH.

Note: In some crystal datasheets Ls is called L1 or Lm and Cs is called C1 or Cm.

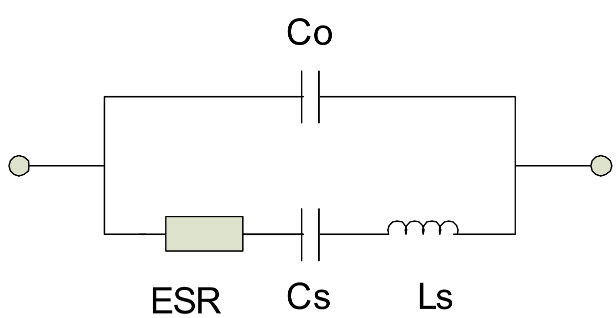

Figure 3. Equivalent crystal components

5.6 DC characteristics

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
V_{IH}	HIGH level input voltage		0.7**VDD**		5.25[a]	V
V_{IL}	LOW level input voltage		**VSS**		0.3**VDD**	V

a. If the input signal >3.6V, the **VDD** of the nRF24L01+ must be between 2.7V and 3.3V (3.0V±10%)

Table 12. Digital input pin

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
V_{OH}	HIGH level output voltage (I_{OH}=-0.25mA)		**VDD** -0.3		**VDD**	V
V_{OL}	LOW level output voltage (I_{OL}=0.25mA)				0.3	V

Table 13. Digital output pin

5.7 Power on reset

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
T_{PUP}	Power ramp up time	a			100	ms
T_{POR}	Power on reset	b	1		100	ms

a. From 0V to 1.9V.
b. Measured from when the **VDD** reaches 1.9V to when the reset finishes.

Table 14. Power on reset

6 Radio Control

This chapter describes the nRF24L01+ radio transceiver's operating modes and the parameters used to control the radio.

The nRF24L01+ has a built-in state machine that controls the transitions between the chip's operating modes. The state machine takes input from user defined register values and internal signals.

6.1 Operational Modes

You can configure the nRF24L01+ in power down, standby, RX or TX mode. This section describes these modes in detail.

6.1.1 State diagram

The state diagram in Figure 4. shows the operating modes and how they function. There are three types of distinct states highlighted in the state diagram:

- **Recommended operating mode:** is a recommended state used during normal operation.
- **Possible operating mode:** is a possible operating state, but is not used during normal operation.
- **Transition state:** is a time limited state used during start up of the oscillator and settling of the PLL.

When the VDD reaches 1.9V or higher nRF24L01+ enters the Power on reset state where it remains in reset until entering the Power Down mode.

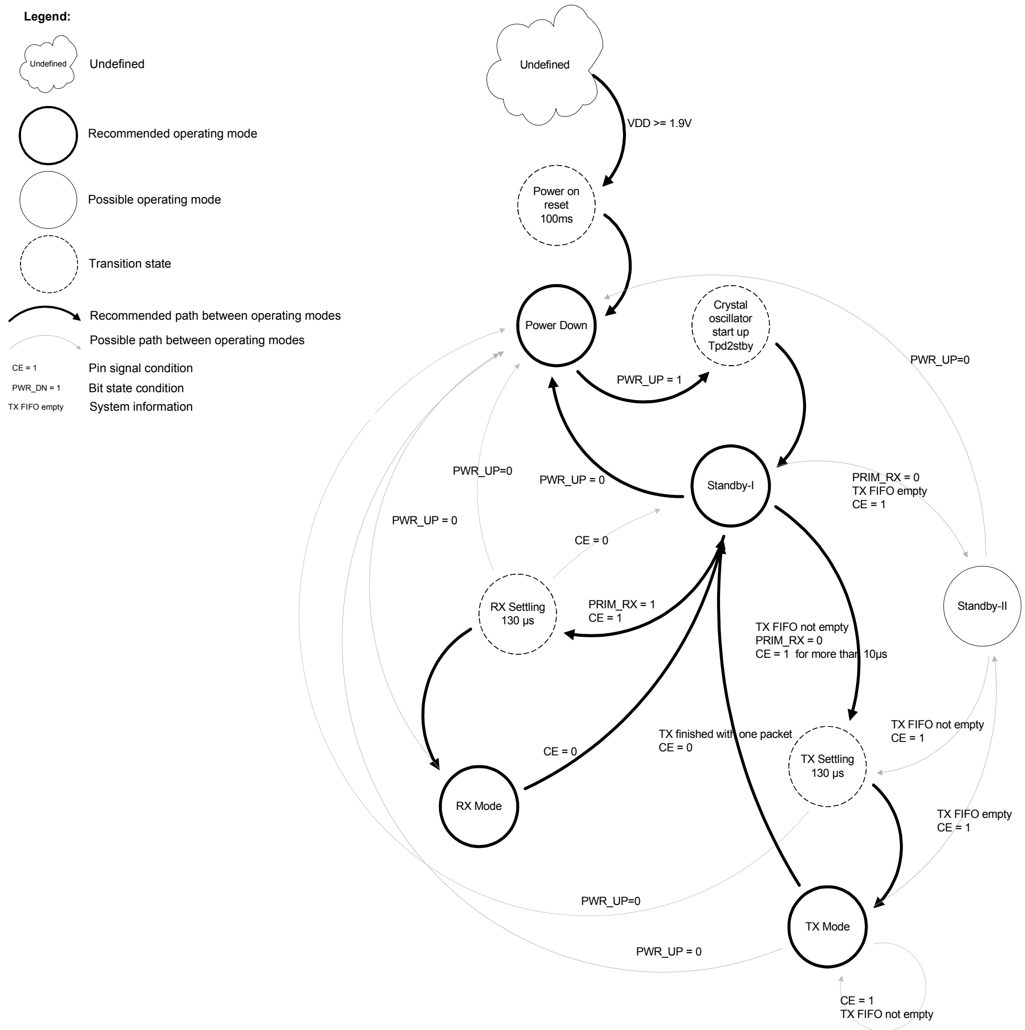

Figure 4. Radio control state diagram

6.1.2 Power Down Mode

In power down mode nRF24L01+ is disabled using minimal current consumption. All register values available are maintained and the SPI is kept active, enabling change of configuration and the uploading/downloading of data registers. For start up times see Table 16. on page 24. Power down mode is entered by setting the PWR_UP bit in the CONFIG register low.

6.1.3 Standby Modes

6.1.3.1 Standby-I mode

By setting the PWR_UP bit in the CONFIG register to 1, the device enters standby-I mode. Standby-I mode is used to minimize average current consumption while maintaining short start up times. In this mode only part of the crystal oscillator is active. Change to active modes only happens if **CE** is set high and when **CE** is set low, the nRF24L01 returns to standby-I mode from both the TX and RX modes.

6.1.3.2 Standby-II mode

In standby-II mode extra clock buffers are active and more current is used compared to standby-I mode. nRF24L01+ enters standby-II mode if **CE** is held high on a PTX device with an empty TX FIFO. If a new packet is uploaded to the TX FIFO, the PLL immediately starts and the packet is transmitted after the normal PLL settling delay (130µs).

Register values are maintained and the SPI can be activated during both standby modes. For start up times see Table 16. on page 24.

6.1.4 RX mode

The RX mode is an active mode where the nRF24L01+ radio is used as a receiver. To enter this mode, the nRF24L01+ must have the PWR_UP bit, PRIM_RX bit and the **CE** pin set high.

In RX mode the receiver demodulates the signals from the RF channel, constantly presenting the demodulated data to the baseband protocol engine. The baseband protocol engine constantly searches for a valid packet. If a valid packet is found (by a matching address and a valid CRC) the payload of the packet is presented in a vacant slot in the RX FIFOs. If the RX FIFOs are full, the received packet is discarded.

The nRF24L01+ remains in RX mode until the MCU configures it to standby-I mode or power down mode. However, if the automatic protocol features (Enhanced ShockBurst™) in the baseband protocol engine are enabled, the nRF24L01+ can enter other modes in order to execute the protocol.

In RX mode a Received Power Detector (RPD) signal is available. The RPD is a signal that is set high when a RF signal higher than -64 dBm is detected inside the receiving frequency channel. The internal RPD signal is filtered before presented to the RPD register. The RF signal must be present for at least 40µs before the RPD is set high. How to use the RPD is described in Section 6.4 on page 25.

6.1.5 TX mode

The TX mode is an active mode for transmitting packets. To enter this mode, the nRF24L01+ must have the PWR_UP bit set high, PRIM_RX bit set low, a payload in the TX FIFO and a high pulse on the **CE** for more than 10µs.

The nRF24L01+ stays in TX mode until it finishes transmitting a packet. If **CE** = 0, nRF24L01+ returns to standby-I mode. If **CE** = 1, the status of the TX FIFO determines the next action. If the TX FIFO is not empty the nRF24L01+ remains in TX mode and transmits the next packet. If the TX FIFO is empty the nRF24L01+ goes into standby-II mode. The nRF24L01+ transmitter PLL operates in open loop when in TX mode. It is important never to keep the nRF24L01+ in TX mode for more than 4ms at a time. If the Enhanced ShockBurst™ features are enabled, nRF24L01+ is never in TX mode longer than 4ms.

6.1.6 Operational modes configuration

The following table (Table 15.) describes how to configure the operational modes.

Mode	PWR_UP register	PRIM_RX register	CE input pin	FIFO state
RX mode	1	1	1	-
TX mode	1	0	1	Data in TX FIFOs. Will empty all levels in TX FIFOs[a].
TX mode	1	0	Minimum 10µs high pulse	Data in TX FIFOs.Will empty one level in TX FIFOs[b].
Standby-II	1	0	1	TX FIFO empty.
Standby-I	1	-	0	No ongoing packet transmission.
Power Down	0	-	-	-

a. If **CE** is held high all TX FIFOs are emptied and all necessary ACK and possible retransmits are carried out. The transmission continues as long as the TX FIFO is refilled. If the TX FIFO is empty when the **CE** is still high, nRF24L01+ enters standby-II mode. In this mode the transmission of a packet is started as soon as the **CSN** is set high after an upload (UL) of a packet to TX FIFO.

b. This operating mode pulses the **CE** high for at least 10µs. This allows one packet to be transmitted. This is the normal operating mode. After the packet is transmitted, the nRF24L01+ enters standby-I mode.

Table 15. nRF24L01+ main modes

6.1.7 Timing Information

The timing information in this section relates to the transitions between modes and the timing for the **CE** pin. The transition from TX mode to RX mode or vice versa is the same as the transition from the standby modes to TX mode or RX mode (max. 130µs), as described in Table 16.

Name	nRF24L01+	Notes	Max.	Min.	Comments
Tpd2stby	Power Down ➔ Standby mode		150µs		With external clock
		a	1.5ms		External crystal, Ls < 30mH
			3ms		External crystal, Ls = 60mH
			4.5ms		External crystal, Ls = 90mH
Tstby2a	Standby modes ➔ TX/RX mode		130µs		
Thce	Minimum **CE** high			10µs	
Tpece2csn	Delay from **CE** positive edge to **CSN** low			4µs	

a. See Table 11. on page 19 for crystal specifications.

Table 16. Operational timing of nRF24L01+

For nRF24L01+ to go from power down mode to TX or RX mode it must first pass through stand-by mode. There must be a delay of Tpd2stby (see Table 16.) after the nRF24L01+ leaves power down mode before the **CE** is set high.

Note: If **VDD** is turned off the register value is lost and you must configure nRF24L01+ before entering the TX or RX modes.

6.2 Air data rate

The air data rate is the modulated signaling rate the nRF24L01+ uses when transmitting and receiving data. It can be 250kbps, 1Mbps or 2Mbps. Using lower air data rate gives better receiver sensitivity than higher air data rate. But, high air data rate gives lower average current consumption and reduced probability of on-air collisions.

The air data rate is set by the `RF_DR` bit in the `RF_SETUP` register. A transmitter and a receiver must be programmed with the same air data rate to communicate with each other.

nRF24L01+ is fully compatible with nRF24L01. For compatibility with nRF2401A, nRF2402, nRF24E1, and nRF24E2 the air data rate must be set to 250kbps or 1Mbps.

6.3 RF channel frequency

The RF channel frequency determines the center of the channel used by the nRF24L01+. The channel occupies a bandwidth of less than 1MHz at 250kbps and 1Mbps and a bandwidth of less than 2MHz at 2Mbps. nRF24L01+ can operate on frequencies from 2.400GHz to 2.525GHz. The programming resolution of the RF channel frequency setting is 1MHz.

At 2Mbps the channel occupies a bandwidth wider than the resolution of the RF channel frequency setting. To ensure non-overlapping channels in 2Mbps mode, the channel spacing must be 2MHz or more. At 1Mbps and 250kbps the channel bandwidth is the same or lower than the resolution of the RF frequency.

The RF channel frequency is set by the `RF_CH` register according to the following formula:

$F_0 = 2400 + RF\_CH\ [MHz]$

You must program a transmitter and a receiver with the same RF channel frequency to communicate with each other.

6.4 Received Power Detector measurements

Received Power Detector (RPD), located in register 09, bit 0, triggers at received power levels above -64 dBm that are present in the RF channel you receive on. If the received power is less than -64 dBm, RDP = 0.

The RPD can be read out at any time while nRF24L01+ is in receive mode. This offers a snapshot of the current received power level in the channel. The RPD status is latched when a valid packet is received which then indicates signal strength from your own transmitter. If no packets are received the RPD is latched at the end of a receive period as a result of host MCU setting CE low or RX time out controlled by Enhanced ShockBurst™.

The status of RPD is correct when RX mode is enabled and after a wait time of Tstby2a +Tdelay_AGC= 130us + 40us. The RX gain varies over temperature which means that the RPD threshold also varies over temperature. The RPD threshold value is reduced by - 5dB at T = -40°C and increased by + 5dB at 85°C.