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nRF24LE1 OTP

Ultra-low Power Wireless System On-Chip Solution

Product Specification v1.2

Key Features

- nRF24L01+ 2.4 GHz transceiver (250 kbps, 1 Mbps and 2 Mbps air data rates)
- Fast microcontroller (8051 compatible)
- 16 kB program memory (on-chip OTP)
- 1 kB data memory (on-chip RAM)
- 1 kB OTP data memory
- AES encryption HW accelerator
- 16-32 bit multiplication/division co-processor (MDU)
- 6–12 bit ADC
- High flexibility IOs
- Serves a set of power modes from ultra low power to a power efficient active mode
- Several versions in various QFN packages:
 - ▶ 4×4 mm QFN24
 - ▶ 5×5 mm QFN32
 - ▶ 7×7 mm QFN48

Applications

- Computer peripherals
 - ▶ Mouse
 - ▶ Keyboard
 - ▶ Remote control
 - ▶ Gaming
- Advanced remote controls
 - ▶ Audio/Video
 - ▶ Entertainment centers
 - ▶ Home appliances
- Goods tracking and monitoring:
 - ▶ Active RFID
 - ▶ Sensor networks
- Security systems
 - ▶ Payment
 - ▶ Alarm
 - ▶ Access control
- Health, wellness and sports
 - ▶ Watches
 - ▶ Mini computers
 - ▶ Sensors
- Remote control toys

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Preliminary product specification	This product specification contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
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Contents

1	Introduction	11
1.1	Prerequisites	11
1.2	Writing conventions	11
2	Product overview	12
2.1	Features	12
2.2	Block diagram	14
2.3	Pin assignments	15
2.3.1	24-pin 4×4 QFN-package variant	15
2.3.2	32-pin 5×5 QFN-package variant	15
2.3.3	48-pin 7×7 QFN-package variant	16
2.4	Pin functions	16
3	RF transceiver	17
3.1	Features	17
3.2	Block diagram	18
3.3	Functional description	18
3.3.1	Operational Modes	18
3.3.1.1	State diagram	18
3.3.1.2	Power down mode	19
3.3.1.3	Standby modes	19
3.3.1.4	RX mode	20
3.3.1.5	TX mode	20
3.3.1.6	Operational modes configuration	21
3.3.1.7	Timing information	21
3.3.2	Air data rate	22
3.3.3	RF channel frequency	22
3.3.4	Received Power Detector measurements	22
3.3.5	PA control	22
3.3.6	RX/TX control	23
3.4	Enhanced ShockBurst™	23
3.4.1	Features	23
3.4.2	Enhanced ShockBurst™ overview	23
3.4.3	Enhanced Shockburst™ packet format	24
3.4.3.1	Preamble	24
3.4.3.2	Address	24
3.4.3.3	Packet Control Field (PCF)	25
3.4.3.4	Payload	25
3.4.3.5	CRC (Cyclic Redundancy Check)	26
3.4.4	Automatic packet assembly	27
3.4.5	Automatic packet disassembly	28
3.4.6	Automatic packet transaction handling	29
3.4.6.1	Auto Acknowledgement	29
3.4.6.2	Auto Retransmission (ART)	29
3.4.7	Enhanced ShockBurst™ flowcharts	31

3.4.7.1	PTX operation	31
3.4.7.2	PRX operation	33
3.4.8	MultiCeiver™	34
3.4.9	Enhanced ShockBurst™ timing	36
3.4.10	Enhanced ShockBurst™ transaction diagram	39
3.4.10.1	Single transaction with ACK packet and interrupts	40
3.4.10.2	Single transaction with a lost packet	40
3.4.10.3	Single transaction with a lost ACK packet	41
3.4.10.4	Single transaction with ACK payload packet	41
3.4.10.5	Single transaction with ACK payload packet and lost packet	42
3.4.10.6	Two transactions with ACK payload packet and the first ACK packet lost	42
3.4.10.7	Two transactions where max retransmissions is reached	43
3.4.11	Compatibility with ShockBurst™	43
3.4.11.1	ShockBurst™ packet format	43
3.5	Data and control interface	44
3.5.1	SFR registers	44
3.5.2	SPI operation	45
3.5.2.1	SPI commands	45
3.5.3	Data FIFO	47
3.5.4	Interrupt	48
3.6	Register map	49
3.6.1	Register map table	49
4	MCU	55
4.1	Block diagram	56
4.2	Features	56
4.3	Functional description	57
4.3.1	Arithmetic Logic Unit (ALU)	57
4.3.2	Instruction set summary	57
4.3.3	Opcode map	61
5	Memory and I/O organization	63
5.1	PDATA memory addressing	64
5.2	MCU Special Function Registers	64
5.2.1	Accumulator - ACC	64
5.2.2	B Register – B	64
5.2.3	Program Status Word Register - PSW	65
5.2.4	Stack Pointer – SP	65
5.2.5	Data Pointer – DPH, DPL	65
5.2.6	Data Pointer 1 – DPH1, DPL1	66
5.2.7	Data Pointer Select Register – DPS	66
5.2.8	PCON register	66
5.2.9	Special Function Register Map	67
5.2.10	Special Function Registers reset values	68
6	OTP memory	71
6.1	Features	71
6.2	Block diagram	71

6.3	Functional description	71
6.3.1	Using the NV data memory	72
6.3.2	OTP memory configuration.....	72
6.3.2.1	InfoPage content	72
6.3.2.2	Memory configuration SFR.....	73
6.3.3	Brown-out	73
6.3.4	Temperature restriction for OTP programming.....	74
6.3.5	OTP programming from the MCU.....	74
6.3.5.1	MCU operations in the main block	74
6.3.6	OTP programming through SPI	74
6.3.6.1	PROG pin requirements	75
6.3.6.2	SPI slave interface	75
7	Random Access memory (RAM).....	79
7.1	SRAM configuration	79
8	Timers/counters	81
8.1	Features	81
8.2	Block diagram	81
8.3	Functional description	82
8.3.1	Timer 0 and Timer 1	82
8.3.1.1	Mode 0 and Mode 1	82
8.3.1.2	Mode 2	83
8.3.1.3	Mode 3	84
8.3.2	Timer 2	84
8.3.2.1	Timer 2 description.....	85
8.3.2.2	Timer mode	85
8.3.2.3	Event counter mode	85
8.3.2.4	Gated timer mode.....	85
8.3.2.5	Timer 2 reload	86
8.4	SFR registers	86
8.4.1	Timer/Counter control register – TCON.....	86
8.4.2	Timer mode register - TMOD.....	87
8.4.3	Timer 0 – TH0, TL0	87
8.4.4	Timer 1 – TH1, TL1	87
8.4.5	Timer 2 control register – T2CON.....	88
8.4.6	Timer 2 – TH2, TL2	88
8.4.7	Compare/Capture enable register – CCEN	89
8.4.8	Capture registers – CC1, CC2, CC3.....	89
8.4.9	Compare/Reload/Capture register – CRCH, CRCL.....	90
8.5	Real Time Clock - RTC	90
8.5.1	Features	90
8.5.2	Functional description of SFR registers.....	90
9	Interrupts	94
9.1	Features	94
9.2	Block diagram	94
9.3	Functional description	95
9.4	SFR registers	95

9.4.1	Interrupt Enable 0 Register – IEN0	96
9.4.2	Interrupt Enable 1 Register – IEN1	96
9.4.3	Interrupt Priority Registers – IP0, IP1	96
9.4.4	Interrupt Request Control Registers – IRCON	97
10	Watchdog	98
10.1	Features	98
10.2	Block diagram	98
10.3	Functional description	98
11	Power and clock management	100
11.1	Block diagram	100
11.2	Modes of operation	100
11.3	Functional description	105
11.3.1	Clock control	105
11.3.2	Power down control – PWRDWN	107
11.3.3	Operational mode control - OPMCON	109
11.3.4	Reset result – RSTREAS	109
11.3.5	Wakeup configuration register – WUCON	110
11.3.6	Pin wakeup configuration	110
12	Power supply supervisor	112
12.1	Features	112
12.2	Block diagram	112
12.3	Functional description	112
12.3.1	Power-on reset	112
12.3.2	Brown-out reset	113
12.3.3	Power-fail comparator	113
12.4	SFR registers	114
13	On-chip oscillators	115
13.1	Features	115
13.2	Block diagrams	115
13.3	Functional description	116
13.3.1	16 MHz crystal oscillator	116
13.3.2	16 MHz RC oscillator	117
13.3.3	External 16 MHz clock	117
13.3.4	32.768 kHz crystal oscillator	117
13.3.5	32.768 kHz RC oscillator	118
13.3.6	Synthesized 32.768 kHz clock	118
13.3.7	External 32.768 kHz clock	118
14	MDU – Multiply Divide Unit	119
14.1	Features	119
14.2	Block diagram	119
14.3	Functional description	119
14.4	SFR registers	119
14.4.1	Loading the MDx registers	120
14.4.2	Executing calculation	121
14.4.3	Reading the result from the MDx registers	121
14.4.4	Normalizing	121

14.4.5	Shifting	121
14.4.6	The mdef flag	121
14.4.7	The mdov flag	122
15	Encryption/decryption accelerator	123
15.1	Features	123
15.2	Block diagram	123
15.3	Functional description	123
16	Random number generator	125
16.1	Features	125
16.2	Block diagram	125
16.3	Functional description	125
16.4	SFR registers	126
17	General purpose IO port and pin assignments	127
17.1	Block diagram	127
17.2	Functional description	128
17.2.1	General purpose IO pin functionality	128
17.2.2	PortCrossbar functionality	129
17.2.2.1	Dynamic allocation of pins	129
17.2.2.2	Dynamic pin allocation for digital blocks	129
17.2.2.3	Dynamic pin allocation for analog blocks	129
17.2.2.4	Default pin allocation	129
17.3	IO pin maps	130
17.3.1	Pin assignments in package 24 pin 4×4 mm	131
17.3.2	Pin assignments in package 32 pin 5×5 mm	132
17.3.3	Pin assignments in package 48 pin 7×7 mm	133
17.3.4	Programmable registers	135
18	SPI	143
18.1	Features	143
18.2	Block diagram	143
18.3	Functional description	144
18.3.1	SPI master	144
18.3.2	SPI slave	146
18.3.3	Slave SPI timing	147
19	Serial port (UART)	150
19.1	Features	150
19.2	Block diagram	150
19.3	Functional description	150
19.3.1	Serial port 0 control register – S0CON	151
19.3.2	Serial port 0 data buffer – S0BUF	152
19.3.3	Serial port 0 reload register – S0RELH, S0RELL	152
19.3.4	Serial port 0 baud rate select register - ADCON	153
20	2-Wire	154
20.1	Features	154
20.2	Functional description	154
20.2.1	Recommended use	154
20.2.2	Master transmitter/receiver	154

20.2.2.1	TX mode	154
20.2.2.2	RX mode	155
20.2.3	Slave transmitter/receiver	155
20.2.3.1	2-Wire timing	156
20.3	SFR registers	157
21	ADC	160
21.1	Features	160
21.2	Block diagram	160
21.3	Functional description	160
21.3.1	Activation	160
21.3.2	Input selection	161
21.3.3	Reference selection	161
21.3.4	Resolution	161
21.3.5	Conversion modes	161
21.3.6	Output data coding	162
21.3.7	Driving the analog input	163
21.3.8	SFR registers	164
22	Analog comparator	166
22.1	Features	166
22.2	Block diagram	166
22.3	Functional description	166
22.3.1	Activation	166
22.3.2	Input selection	166
22.3.3	Reference selection	167
22.3.4	Output polarity	167
22.3.5	Input voltage range	167
22.3.6	Configuration examples	167
22.3.7	Driving the analog input	167
22.3.8	SFR registers	168
23	PWM	169
23.1	Features	169
23.2	Block diagram	169
23.3	Functional description	169
24	Absolute maximum ratings	171
25	Operating condition	172
26	Electrical specifications	173
26.1	Power consumption	178
27	Mechanical specifications	180
28	Reference circuits	182
28.1	nRF24LE1 OTP, 7×7 mm QFN48	182
28.1.1	Schematics	182
28.1.2	Layout	183
28.1.3	Bill of Materials (BOM)	183
28.2	nRF24LE1 OTP, 5×5 mm QFN32	184
28.2.1	Schematics	184
28.2.2	Layout	185

28.2.3	Bill Of Materials (BOM)	185
28.3	nRF24LE1 OTP, 4×4 mm QFN24	186
28.3.1	Schematics	186
28.3.2	Layout	187
28.3.3	Bill Of Materials (BOM)	187
29	Ordering information	188
29.1	Package marking	188
29.1.1	Abbreviations	188
29.2	Product options	188
29.2.1	RF silicon	188
29.2.2	Development tools	189
30	Glossary	190

1 Introduction

The nRF24LE1 OTP is a member of the low-cost, high-performance family of intelligent 2.4 GHz RF transceivers with embedded microcontrollers. The nRF24LE1 OTP is optimized to provide a single chip solution for ULP wireless applications. The combination of processing power, memory, low power oscillators, real-time counter, AES encryption accelerator, random generator and a range of power saving modes provides an ideal platform for implementation of RF protocols. Benefits of using nRF24LE1 OTP include tighter protocol timing, security, lower power consumption and improved co-existence performance. For the application layer the nRF24LE1 OTP offers a rich set of peripherals including: SPI, 2-wire, UART, 6 to 12 bit ADC, PWM and an ultra low power analog comparator for voltage level system wake-up.

The nRF24LE1 OTP comes in different package variants:

- nRF24LE1: An ultra compact 4×4mm 24 pin QFN (7 generic I/O pins)
- nRF24LE1: A compact 5×5mm 32 pin QFN (15 generic I/O pins)
- nRF24LE1: A 7×7mm 48 pin QFN (31 generic I/O pins)

The 4×4mm 24 pin QFN is ideal for low I/O count applications where small size is key. Examples include wearable sports sensors and watches. The 5×5mm 32 pin QFN is ideal for medium I/O count applications such as wireless mouse, remote controls and toys. The 7×7mm 48 pin QFN is designed for high I/O count products like wireless keyboards.

1.1 Prerequisites

In order to fully understand the product specification, a good knowledge of electronic and software engineering is necessary.

1.2 Writing conventions

This product specification follows a set of typographic rules to make the document consistent and easy to read. The following writing conventions are used:

- Commands, bit state conditions, and register names are written in `Courier New`.
- Pin names and pin signal conditions are written in **Courier New bold**.
- Cross references are [underlined and highlighted in blue](#).

2 Product overview

2.1 Features

Features of the nRF24LE1 OTP include:

- Fast 8-bit microcontroller:
 - Intel MCS 51 compliant instruction set
 - Reduced instruction cycle time, up to 12 times compared to legacy 8051
 - 32 bit multiplication – division unit
- Memory:
 - Program memory: 16 kB of OTP memory with security features
 - Data memory: 1 kB of on-chip RAM memory
 - Non-volatile data memory: 1 kB
- A number of on-chip hardware resources are available through programmable multi purpose input/output pins (7–31 pins dependent on package variant):
 - GPIO
 - SPI master
 - SPI slave
 - 2-Wire master/ slave
 - Full duplex serial port
 - PWM
 - ADC
 - Analog comparator
 - External interrupts
 - Timer inputs
 - 32.768 kHz crystal oscillator
- High performance 2.4 GHz RF transceiver
 - True single chip GFSK transceiver
 - Enhanced ShockBurst™ link layer support in HW:
 - Packet assembly/disassembly
 - Address and CRC computation
 - Auto ACK and retransmit
 - On the air data rate 250 kbps, 1 Mbps or 2 Mbps
 - Digital interface (SPI) speed 0–8 Mbps
 - 125 RF channels operation, with 79 (2.402 GHz – 2.480 GHz) channels within 2.400–2.4835 GHz
 - Short switching time enable frequency hopping
 - Fully RF compatible with nRF24LXX
 - RF compatible with nRF2401A, nRF2402, nRF24E1, nRF24E2 in 250 kbps and 1 Mbps mode
- A/D converter:
 - 6, 8, 10 or 12 bit resolution
 - 14 input channels
 - Single ended or differential input
 - Full-scale range set by internal reference, external reference or VDD
 - Single step mode with conversion time down to 3 μs
 - Continuous mode with 2, 4, 8 or 16 kbps sampling rate
 - Low current consumption; only 0.1mA at 2 ksps
 - Mode for measuring supply voltage

- Analog comparator:
 - ▶ Used as wakeup source
 - ▶ Low current consumption (0.75µA typical)
 - ▶ Differential or single-ended input
 - ▶ Single-ended threshold programmable to 25%, 50%, 75% or 100% of VDD or an arbitrary reference voltage from pin
 - ▶ 14-channel input multiplexer
 - ▶ Rail-to-rail input voltage range
 - ▶ Programmable output polarity
- Encryption/decryption accelerator
 - ▶ Utilize time and power effective AES firmware
- Random number generator:
 - ▶ Non-deterministic architecture based on thermal noise
 - ▶ No seed value required
 - ▶ Non-repeating sequence
 - ▶ Corrector algorithm ensures uniform statistical distribution
 - ▶ Data rate up to 10 kB per second
 - ▶ Operational while the processor is in standby
- System reset and power supply monitoring:
 - ▶ On-chip power-on and brown-out reset
 - ▶ Watchdog timer reset
 - ▶ Reset from pin
 - ▶ Power-fail comparator with programmable threshold and interrupt to MCU
- On-chip timers:
 - ▶ Three 16-bit timers/counters operating at the system clock (sources from the 16 MHz on-chip oscillators)
 - ▶ One 16-bit timer/counter operating at the low frequency clock (32.768 kHz)
- On-chip oscillators:
 - ▶ 16 MHz crystal oscillator XOSC16M
 - ▶ 16 MHz RC-oscillator RCOSC16M
 - ▶ 32.768 kHz crystal oscillator XOSC32K
 - ▶ 32.768 kHz RC-oscillator RCOSC32K
- Power management function:
 - ▶ Low power design supporting fully static stop/ standby
 - ▶ Programmable MCU clock frequency from 125 kHz to 16 MHz
 - ▶ On chip voltage regulators supporting low power mode
 - ▶ Watchdog and wakeup functionality running in low power mode
- Complete firmware platform available:
 - ▶ Hardware abstraction layer (HAL) Functions
 - ▶ Library functions
 - ▶ Gazell Wireless protocol
 - ▶ Application examples

2.2 Block diagram

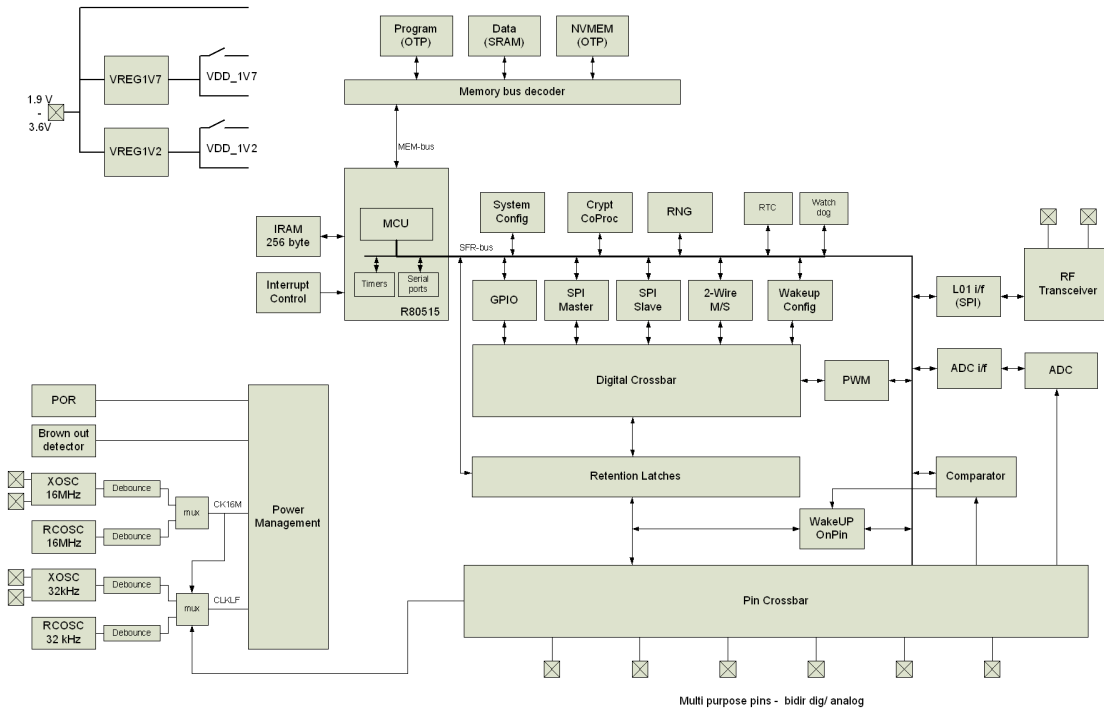


Figure 1. nRF24LE1 OTP block diagram

To find more information on the blocks shown in Figure 1, see [Table 1](#). below:

Name	Reference
Memory (Program, Data, NVMEM)	Chapter 5 on page 63
Power management	Chapter 11 on page 100
RF transceiver	Chapter 3 on page 17
2-Wire	Chapter 20 on page 154
SPI (Master and Slave)	Chapter 18 on page 143
GPIO	Chapter 17 on page 127
PWM	Chapter 23 on page 169
Watchdog	Chapter 10 on page 98

Table 1. Block diagram cross references

2.3 Pin assignments

2.3.1 24-pin 4x4 QFN-package variant

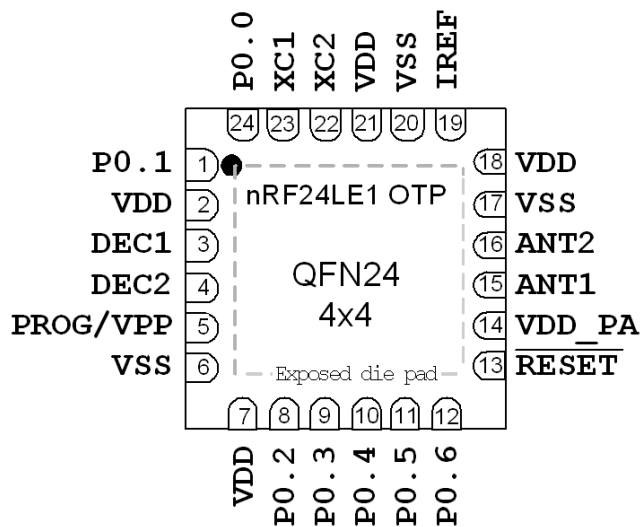


Figure 2. nRF24LE1 OTP pin assignment (top view) for a QFN24 4x4 mm package

2.3.2 32-pin 5x5 QFN-package variant

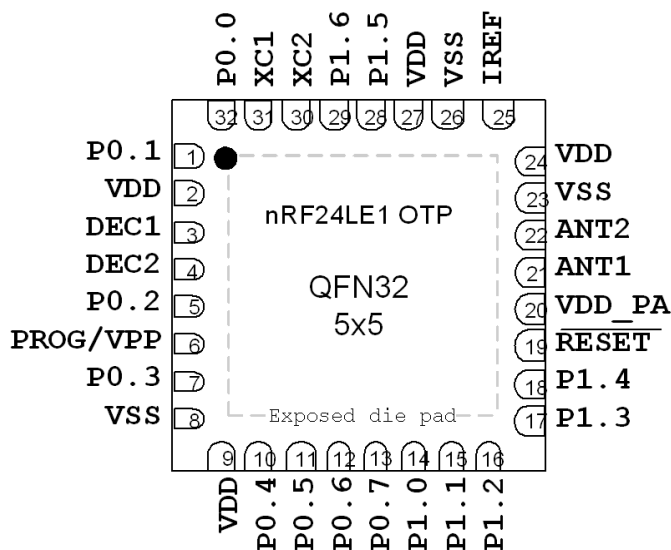


Figure 3. nRF24LE1 OTP pin assignment (top view) for a QFN32 5x5 mm package

2.3.3 48-pin 7×7 QFN-package variant

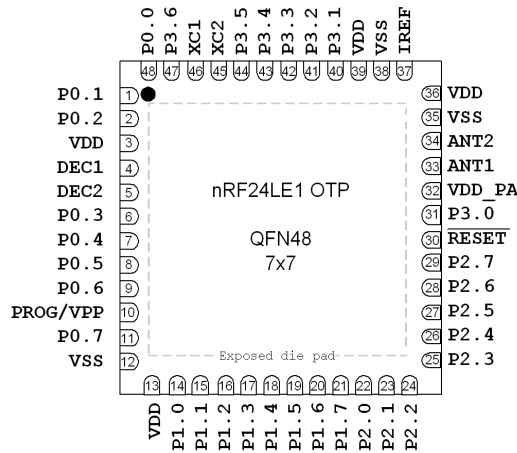


Figure 4. nRF24LE1 OTP pin assignment (top view) for a QFN48 7×7 mm package

2.4 Pin functions

Name	Type	Description
VDD	Power	Power supply (+1.9V to +3.6V DC)
VSS	Power	Ground (0V)
DEC1 DEC2	Power	Power supply outputs for de-coupling purposes (100nF for DEC1, 33nF for DEC2)
P0.0 – P3.6	Digital or analog I/O	General purpose I/O pins. Number of I/O available depends on package type.
PROG/VPP	Digital Input, High Voltage	Input to enable OTP programming. This pin requires an external pull-down resistor, or must be connected to ground if external programming is not needed.
RESET	Digital Input	Reset for microcontroller, active low
IREF	Analog Input	Device reference current output. To be connected to reference resistor on PCB.
VDD_PA	Power Output	Power supply output (+1.8V) for on-chip RF Power amplifier
ANT1, ANT2	RF	Differential antenna connection (TX and RX)
XC1, XC2	Analog Input	Crystal connection for 16 MHz crystal
Exposed die pad	Power/heat relief	For the nRF24LE1 OTP QFN48 7×7mm and QFN32 5×5mm connect the die pad to GND. For nRF24LE1 OTP QFN24 4×4mm do not connect the die pad to GND.

Table 2. nRF24LE1 OTP pin functions

3 RF transceiver

The nRF24LE1 OTP uses the same 2.4 GHz GFSK RF transceiver with embedded protocol engine (Enhanced ShockBurst™) that is found in the nRF24L01+ single chip RF transceiver. The RF transceiver is designed for operation in the world wide ISM frequency band at 2.400–2.4835 GHz and is very well suited for ultra low power wireless applications.

The RF transceiver module is configured and operated through the RF transceiver map. This register map is accessed by the MCU through a dedicated on-chip Serial Peripheral interface (SPI) and is available in all power modes of the RF transceiver module.

The embedded protocol engine (Enhanced ShockBurst™) enables data packet communication and supports various modes from manual operation to advanced autonomous protocol operation. Data FIFOs in the RF transceiver module ensure a smooth data flow between the RF transceiver module and the nRF24LE1 OTP MCU.

The rest of this chapter is written in the context of the RF transceiver module as the core and the rest of the nRF24LE1 OTP as external circuitry to this module.

3.1 Features

Features of the RF transceiver include:

- General
 - ▶ Worldwide 2.4 GHz ISM band operation
 - ▶ Common antenna interface in transmit and receive
 - ▶ GFSK modulation
 - ▶ 250 kbps, 1 and 2 Mbps on air data rate
- Transmitter
 - ▶ Programmable output power: 0, -6, -12 or -18dBm
 - ▶ 11.1mA at 0dBm output power
- Receiver
 - ▶ Integrated channel filters
 - ▶ 13.3mA at 2 Mbps
 - ▶ -82 dBm sensitivity at 2 Mbps
 - ▶ -85 dBm sensitivity at 1 Mbps
 - ▶ -94 dBm sensitivity at 250 kbps
- RF Synthesizer
 - ▶ Fully integrated synthesizer
 - ▶ 1 MHz frequency programming resolution
 - ▶ Accepts low cost ± 60 ppm 16 MHz crystal
 - ▶ 1 MHz non-overlapping channel spacing at 1 Mbps
 - ▶ 2 MHz non-overlapping channel spacing at 2 Mbps
- Enhanced ShockBurst™
 - ▶ 1 to 32 bytes dynamic payload length
 - ▶ Automatic packet handling (assembly/disassembly)
 - ▶ Automatic packet transaction handling (auto ACK, auto retransmit)
- 6 data pipe MultiCeiver™ for 6:1 star networks

3.2 Block diagram

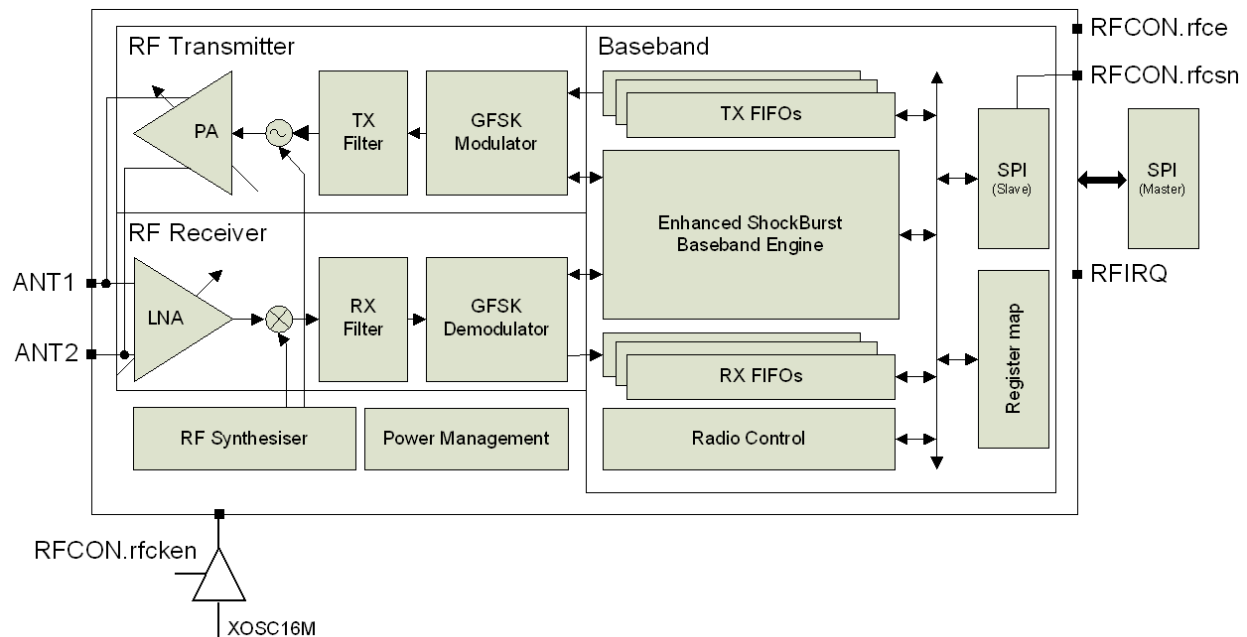


Figure 5. RF transceiver block diagram

3.3 Functional description

This section describes the different operating modes of the RF transceiver and the parameters used to control it.

The RF transceiver module has a built-in state machine that controls the transitions between the different operating modes. The state machine is controlled by SFR register `RFCON` and RF transceiver register `CONFIG`, see [section 3.5](#) for details.

3.3.1 Operational Modes

You can configure the RF transceiver to power down, standby, RX and TX mode. This section describes these modes in detail.

3.3.1.1 State diagram

The state diagram ([Figure 6.](#)) shows the operating modes of the RF transceiver and how they function. At the end of the reset sequence the RF transceiver enters Power Down mode. When the RF transceiver enters Power Down mode the MCU can still control the module through the SPI and the `rfcsn` bit in the `RFCON` register.

There are three types of distinct states highlighted in the state diagram:

- **Recommended operating mode:** is a recommended state used during normal operation.
- **Possible operating mode:** is a possible operating state, but is not used during normal operation.
- **Transition state:** is a time limited state used during start up of the oscillator and settling of the PLL.

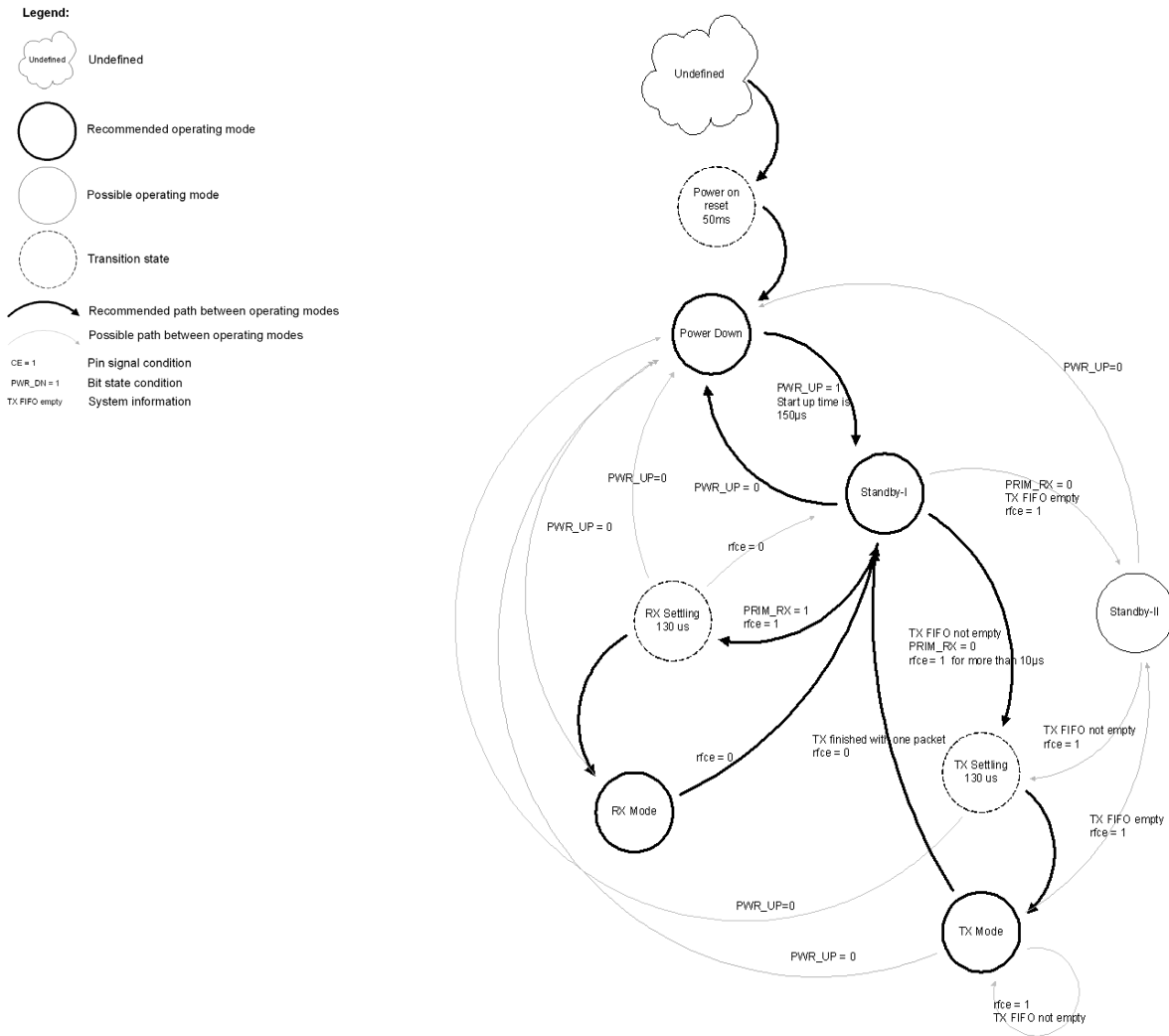


Figure 6. Radio control state diagram

3.3.1.2 Power down mode

In power down mode the RF transceiver is disabled with minimal current consumption. All the register values available from the SPI are maintained and the SPI can be activated. For start up times see [Table 5. on page 23](#). Power down mode is entered by setting the `PWR_UP` bit in the `CONFIG` register low.

3.3.1.3 Standby modes

Standby-I mode

By setting the `PWR_UP` bit in the `CONFIG` register to 1, the RF transceiver enters standby-I mode. Standby-I mode is used to minimize average current consumption while maintaining short start up times. Change to the active mode only happens if the `rfce` bit is enabled and when it is not enabled, the RF transceiver returns to standby-I mode from both the TX and RX modes.

Standby-II mode

In standby-II mode extra clock buffers are active and more current is used compared to standby-I mode. The RF transceiver enters standby-II mode if the `rfce` bit is held high on a PTX operation with an empty TX FIFO. If a new packet is downloaded to the TX FIFO, the PLL immediately starts and the packet is transmitted after the normal PLL settling delay (130 μ s).

The register values are maintained and the SPI can be activated during both standby modes. For start up times see [Table 5. on page 23](#).

3.3.1.4 RX mode

The RX mode is an active mode where the RF transceiver is used as a receiver. To enter this mode, the RF transceiver must have the `PWR_UP` bit, `PRIM_RX` bit and the `rfce` bit is set high.

In RX mode the receiver demodulates the signals from the RF channel, constantly presenting the demodulated data to the baseband protocol engine. The baseband protocol engine constantly searches for a valid packet. If a valid packet is found (by a matching address and a valid CRC) the payload of the packet is presented in a vacant slot in the RX FIFOs. If the RX FIFOs are full, the received packet is discarded.

The RF transceiver remains in RX mode until the MCU configures it to standby-I mode or power down mode. However, if the automatic protocol features (Enhanced ShockBurst™) in the baseband protocol engine are enabled, the RF transceiver can enter other modes in order to execute the protocol.

In RX mode a Received Power Detector (RPD) signal is available. The RPD is a signal that is set high when a RF signal higher than -64 dBm is detected inside the receiving frequency channel. The internal RPD signal is filtered before presented to the RPD register. The RF signal must be present for at least 40 μ s before the RPD is set high. How to use the RPD is described in [Section 3.3.4 on page 22](#).

3.3.1.5 TX mode

The TX mode is an active mode for transmitting packets. To enter this mode, the RF transceiver must have the `PWR_UP` bit set high, `PRIM_RX` bit set low, a payload in the TX FIFO and a high pulse on the `rfce` bit for more than 10 μ s.

The RF transceiver stays in TX mode until it finishes transmitting a packet. If `rfce` = 0, RF transceiver returns to standby-I mode. If `rfce` = 1, the status of the TX FIFO determines the next action. If the TX FIFO is not empty the RF transceiver remains in TX mode and transmits the next packet. If the TX FIFO is empty the RF transceiver goes into standby-II mode. The RF transceiver transmitter PLL operates in open loop when in TX mode. It is important never to keep the RF transceiver in TX mode for more than 4 ms at a time. If the Enhanced ShockBurst™ features are enabled, RF transceiver is never in TX mode longer than 4 ms.

3.3.1.6 Operational modes configuration

The following table ([Table 3.](#)) describes how to configure the operational modes.

Mode	PWR_UP register	PRIM_RX register	rfce	FIFO state
RX mode	1	1	1	-
TX mode	1	0	1	Data in TX FIFO. Will empty all levels in TX FIFO ^a .
TX mode	1	0	Minimum 10 μ s high pulse	Data in TX FIFO. Will empty one level in TX FIFO ^b .
Standby-II	1	0	1	TX FIFO empty
Standby-I	1	-	0	No ongoing packet transmission
Power Down	0	-	-	-

- If the `rfce` bit is held high the TX FIFO is emptied and all necessary ACK and possible retransmits are carried out. The transmission continues as long as the TX FIFO is refilled. If the TX FIFO is empty when the `rfce` bit is still high, the RF transceiver enters standby-II mode. In this mode the transmission of a packet is started as soon as the `rfcsn` is set high after an upload (UL) of a packet to TX FIFO.
- This operating mode pulses the `rfce` bit high for at least 10 μ s. This allows one packet to transmit. This is the normal operating mode. After the packet is transmitted, the RF transceiver enters standby-I mode.

Table 3. RF transceiver main modes

3.3.1.7 Timing information

The timing information in this section relates to the transitions between modes and the timing for the `rfce` bit. The transition from TX mode to RX mode or vice versa is the same as the transition from the standby modes to TX mode or RX mode (130 μ s), as described in [Table 4.](#)

Name	RF transceiver	Max.	Min.	Comments
Tpd2stby	Power Down → Standby mode	1 μ s ^a		
Tstby2a	Standby modes → TX/RX mode	130 μ s		
Thce	Minimum <code>rfce</code> high		10 μ s	
Tpece2csn	Delay from <code>rfce</code> pos. edge to <code>rfcsn</code> low		4 μ s	

- This presupposes that the XO is running. Please refer to `CLKLFCTRL` for bit 3 in [Table 58. on page 107.](#)

Table 4. Operational timing of RF transceiver

Note: If VDD is turned off, or if the nRF24LE1 OTP enters Deep Sleep or Memory Retention mode, the register values are lost and you must configure the RF transceiver before entering the TX or RX modes.

3.3.2 Air data rate

The air data rate is the modulated signaling rate the RF transceiver uses when transmitting and receiving data. It can be 250 kbps, 1 Mbps or 2 Mbps. Using lower air data rate gives better receiver sensitivity than higher air data rate. But, high air data rate gives lower average current consumption and reduced probability of on-air collisions.

The air data rate is set by the `RF_DR` bit in the `RF_SETUP` register. A transmitter and a receiver must be programmed with the same air data rate to communicate with each other.

The RF transceiver is fully compatible with nRF24L01. For compatibility with nRF2401A, nRF2402, nRF24E1, and nRF24E2 the air data rate must be set to 250 kbps or 1 Mbps.

3.3.3 RF channel frequency

The RF channel frequency determines the center of the channel used by the RF transceiver. The channel occupies a bandwidth of less than 1 MHz at 250 kbps and 1 Mbps and a bandwidth of less than 2 MHz at 2 Mbps. The RF transceiver can operate on frequencies from 2.400 GHz to 2.525 GHz. The programming resolution of the RF channel frequency setting is 1 MHz.

At 2 Mbps the channel occupies a bandwidth wider than the resolution of the RF channel frequency setting. To ensure non-overlapping channels in 2 Mbps mode, the channel spacing must be 2 MHz or more. At 1 Mbps and 250 kbps the channel bandwidth is the same or lower than the resolution of the RF frequency.

The RF channel frequency is set by the `RF_CH` register according to the following formula:

$$F_0 = 2400 + RF_CH \text{ MHz}$$

You must program a transmitter and a receiver with the same RF channel frequency to communicate with each other.

3.3.4 Received Power Detector measurements

Received Power Detector (RPD), located in register 09, bit 0, triggers at received power levels above -64 dBm that are present in the RF channel you receive on. If the received power is less than -64 dBm, RDP = 0.

The RPD can be read out at any time while the RF transceiver is in receive mode. This offers a snapshot of the current received power level in the channel. The RPD is latched whenever a packet is received or when the MCU sets `rfce` low.

The status of RPD is correct when RX mode is enabled and after a wait time of $T_{stby2a} + T_{delay_AGC} = 130 \mu s + 40 \mu s$. The RX gain varies over temperature which means that the RPD threshold also varies over temperature. The RPD threshold value is reduced by -5dB at $T = -40^\circ C$ and increased by +5dB at $85^\circ C$.

3.3.5 PA control

The PA (Power Amplifier) control is used to set the output power from the RF transceiver power amplifier. In TX mode PA control has four programmable steps, see [Table 5. on page 23](#)

The PA control is set by the `RF_PWR` bits in the `RF_SETUP` register.

SPI RF-SETUP (<code>RF_PWR</code>)	RF output power	DC current consumption
11	0 dBm	11.1mA
10	-6 dBm	8.8mA
01	-12 dBm	7.3mA
00	-18 dBm	6.8mA

Conditions: $V_{DD} = 3.0V$, $V_{SS} = 0V$, $T_A = 27^{\circ}C$, Load impedance = $15\Omega + j88\Omega$.

Table 5. RF output power setting for the RF transceiver

3.3.6 RX/TX control

The RX/TX control is set by `PRIM_RX` bit in the `CONFIG` register and sets the RF transceiver in transmit/receive.

3.4 Enhanced ShockBurst™

Enhanced ShockBurst™ is a packet based data link layer that features automatic packet assembly and timing, automatic acknowledgement and retransmissions of packets. Enhanced ShockBurst™ enables the implementation of ultra low power and high performance communication. The Enhanced ShockBurst™ features enable significant improvements of power efficiency for bi-directional and uni-directional systems, without adding complexity on the host controller side.

3.4.1 Features

The main features of Enhanced ShockBurst™ are:

- 1 to 32 bytes dynamic payload length
- Automatic packet handling
- Auto packet transaction handling
 - Auto Acknowledgement
 - Auto retransmit
- 6 data pipe MultiCeiver™ for 1:6 star networks

3.4.2 Enhanced ShockBurst™ overview

Enhanced ShockBurst™ uses ShockBurst™ for automatic packet handling and timing. During transmit, ShockBurst™ assembles the packet and clocks the bits in the data packet for transmission. During receive, ShockBurst™ constantly searches for a valid address in the demodulated signal. When ShockBurst™ finds a valid address, it processes the rest of the packet and validates it by CRC. If the packet is valid the payload is moved into a vacant slot in the RX FIFOs. All high speed bit handling and timing is controlled by ShockBurst™.

Enhanced ShockBurst™ features automatic packet transaction handling for the easy implementation of a reliable bi-directional data link. An Enhanced ShockBurst™ packet transaction is a packet exchange between two transceivers, with one transceiver acting as the Primary Receiver (PRX) and the other transceiver acting as the Primary Transmitter (PTX). An Enhanced ShockBurst™ packet transaction is always initiated by a packet transmission from the PTX, the transaction is complete when the PTX has

received an acknowledgment packet (ACK packet) from the PRX. The PRX can attach user data to the ACK packet enabling a bi-directional data link.

The automatic packet transaction handling works as follows:

1. You begin the transaction by transmitting a data packet from the PTX to the PRX. Enhanced ShockBurst™ automatically sets the PTX in receive mode to wait for the ACK packet.
2. If the packet is received by the PRX, Enhanced ShockBurst™ automatically assembles and transmits an acknowledgment packet (ACK packet) to the PTX before returning to receive mode.
3. If the PTX does not receive the ACK packet immediately, Enhanced ShockBurst™ automatically retransmits the original data packet after a programmable delay and sets the PTX in receive mode to wait for the ACK packet.

In Enhanced ShockBurst™ it is possible to configure parameters such as the maximum number of retransmits and the delay from one transmission to the next retransmission. All automatic handling is done without the involvement of the MCU.

3.4.3 Enhanced Shockburst™ packet format

The format of the Enhanced ShockBurst™ packet is described in this section. The Enhanced ShockBurst™ packet contains a preamble field, address field, packet control field, payload field and a CRC field. [Figure 7](#). shows the packet format with MSB to the left.



Figure 7. An Enhanced ShockBurst™ packet with payload (0-32 bytes)

3.4.3.1 Preamble

The preamble is a bit sequence used to synchronize the receivers demodulator to the incoming bit stream. The preamble is one byte long and is either 01010101 or 10101010. If the first bit in the address is 1 the preamble is automatically set to 10101010 and if the first bit is 0 the preamble is automatically set to 01010101. This is done to ensure there are enough transitions in the preamble to stabilize the receiver.

3.4.3.2 Address

This is the address for the receiver. An address ensures that the correct packet is detected by the receiver. The address field can be configured to be 3, 4 or, 5 bytes long with the **AW** register.

Note: Addresses where the level shifts only one time (that is, 000FFFFFFF) can often be detected in noise and can give a false detection, which may give a raised Packet-Error-Rate. Addresses as a continuation of the preamble (hi-low toggling) raises the Packet-Error-Rate.

3.4.3.3 Packet Control Field (PCF)

[Figure 8.](#) shows the format of the 9 bit packet control field, MSB to the left.

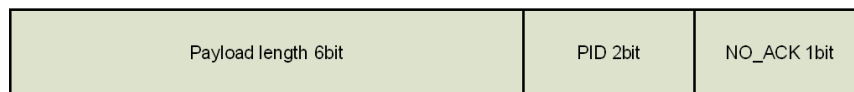


Figure 8. Packet control field (PCF)

The packet control field contains a 6 bit payload length field, a 2 bit PID (Packet Identity) field and a 1 bit NO_ACK flag.

Payload length

This 6 bit field specifies the length of the payload in bytes. The length of the payload can be from 0 to 32 bytes.

Coding: 000000 = 0 byte (only used in empty ACK packets.) 100000 = 32 byte, 100001 = Don't care.

This field is only used if the Dynamic Payload Length function is enabled.

PID (Packet identification)

The 2 bit PID field is used to detect if the received packet is new or retransmitted. PID prevents the PRX operation from presenting the same payload more than once to the MCU. The PID field is incremented at the TX side for each new packet received through the SPI. The PID and CRC fields (see [section 3.4.3.5 on page 26](#)) are used by the PRX operation to determine if a packet is retransmitted or new. When several data packets are lost on the link, the PID fields may become equal to the last received PID. If a packet has the same PID as the previous packet, the RF transceiver compares the CRC sums from both packets. If the CRC sums are also equal, the last received packet is considered a copy of the previously received packet and discarded.

No Acknowledgment flag (NO_ACK)

The Selective Auto Acknowledgement feature controls the NO_ACK flag.

This flag is only used when the auto acknowledgement feature is used. Setting the flag high, tells the receiver that the packet is not to be auto acknowledged.

3.4.3.4 Payload

The payload is the user defined content of the packet. It can be 0 to 32 bytes wide and is transmitted on-air when it is uploaded (unmodified) to the device.

Enhanced ShockBurst™ provides two alternatives for handling payload lengths; static and dynamic.

The default is static payload length. With static payload length all packets between a transmitter and a receiver have the same length. Static payload length is set by the **RX_PW_Px** registers on the receiver side. The payload length on the transmitter side is set by the number of bytes clocked into the TX_FIFO and must equal the value in the **RX_PW_Px** register on the receiver side.