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nRF24LE1

Ultra-low Power Wireless System On-Chip Solution

Product Specification v1.6

Key Features

- nRF24L01+ 2.4 GHz transceiver (250 kbps, 1 Mbps and 2 Mbps air data rates)
- Fast microcontroller (8051 compatible)
- 16 kB program memory (on-chip Flash)
- 1 kB data memory (on-chip RAM)
- 1 kB NV data memory
- 512 bytes NV data memory (extended endurance)
- AES encryption HW accelerator
- 16-32bit multiplication/division co-processor (MDU)
- 6-12 bit ADC
- High flexibility IOs
- Serves a set of power modes from ultra low power to a power efficient active mode
- Several versions in various QFN packages:
  - 4×4mm QFN24
  - 5×5mm QFN32
  - 7×7mm QFN48
- Support for HW debugger
- HW support for firmware upgrade

Applications

- Computer peripherals
  - Mouse
  - Keyboard
  - Remote control
  - Gaming
- Advanced remote controls
  - Audio/Video
  - Entertainment centers
  - Home appliances
- Goods tracking and monitoring:
  - Active RFID
  - Sensor networks
- Security systems
  - Payment
  - Alarm
  - Access control
- Health, wellness and sports
  - Watches
  - Mini computers
  - Sensors
- Remote control toys

August 2010

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Data sheet status	
Objective product specification	This product specification contains target specifications for product development.
Preliminary product specification	This product specification contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
Product specification	This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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Revision History

Date	Version	Description
March 2009	1.2	Updated Figure 33., Figure 34. and Table 35..
September 2009	1.3	Added Table 93. Updated BOM, Table 28., Table 29.,Table 34.,Table 46., Table 53., Table 61.,Table 87., Table 101., Table 113., Table 115., sections 6.3.4.1, 9.1, 9.3 13.3.3, 29.1.2, 29.2.2, 29.3.2 and 30.1. Simplified way of writing binary numbers and denoting register bits.
April 2010	1.4	Updated Figure 9., Figure 10., Figure 30., Note: on page 87, Figure 46., Figure 51. and Figure 52. Updated section 2.1, section 12.3 , section 13.3.1, Table 14. , Table 15., Table 27.,Table 58., Table 111. ,Table 114. and Table 115. Updated BOM information in chapter 29.
July 2010	1.5	Updated 6.3.5.1 on page 77, Table 57. on page 109, Table 58. on page 111, Table 88. on page 150, and Human Body Model Class in chapter 24 on page 176.
August 2010	1.6	Added RoHS statement and updated Table 88. on page 150.

RoHS statement

Nordic Semiconductor's products meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substances (RoHS). Complete hazardous substance reports as well as material composition reports for all active Nordic products can be found on our web site www.nordicsemi.com.

Contents

1 Introduction

The nRF24LE1 is a member of the low-cost, high-performance family of intelligent 2.4 GHz RF transceivers with embedded microcontrollers. The nRF24LE1 is optimized to provide a single chip solution for ULP wireless applications. The combination of processing power, memory, low power oscillators, real-time counter, AES encryption accelerator, random generator and a range of power saving modes provides an ideal platform for implementation of RF protocols. Benefits of using nRF24LE1 include tighter protocol timing, security, lower power consumption and improved co-existence performance. For the application layer the nRF24LE1 offers a rich set of peripherals including: SPI, 2-wire, UART, 6 to 12 bit ADC, PWM and an ultra low power analog comparator for voltage level system wake-up.

The nRF24LE1 comes in three different package variants:

- An ultra compact 4×4mm 24 pin QFN (7 generic I/O pins)
- A compact 5×5mm 32 pin QFN (15 generic I/O pins)
- A 7×7mm 48 pin QFN (31 generic I/O pins)

The 4×4mm 24 pin QFN is ideal for low I/O count applications where small size is key. Examples include wearable sports sensors and watches. The 5×5mm 32 pin QFN is ideal for medium I/O count applications such as wireless mouse, remote controls and toys. The 7×7mm 48 pin QFN is designed for high I/O count products like wireless keyboards.

1.1 Prerequisites

In order to fully understand the product specification, a good knowledge of electronics and software engineering is necessary.

1.2 Writing conventions

This product specification follows a set of typographic rules that makes the document consistent and easy to read. The following writing conventions are used:

- Commands, bit state conditions, and register names are written in `Courier`.
- Pin names and pin signal conditions are written in **`Courier bold`**.
- Cross references are underlined and highlighted in blue.

2 Product overview

2.1 Features

Features of the nRF24LE1 include:

- Fast 8-bit microcontroller:
  - Intel MCS 51 compliant instruction set
  - Reduced instruction cycle time, up to 12 times compared to legacy 8051
  - 32 bit multiplication – division unit
- Memory:
  - Program memory: 16 kB of Flash memory with security features (up to 1k erase/ write cycles)
  - Data memory: 1 kB of on-chip RAM memory
  - Non-volatile data memory: 1 kB
  - Non-volatile data memory extended endurance: 512 bytes (up to 20k erase/ write cycles)
- A number of on-chip hardware resources are available through programmable multi-purpose input/ output pins (7-31 pins dependent on package variant):
  - GPIO
  - SPI master
  - SPI slave
  - 2-Wire master/ slave
  - Full duplex serial port
  - PWM
  - ADC
  - Analog comparator
  - External interrupts
  - Timer inputs
  - 32.768 kHz crystal oscillator
  - Debug interface
- High performance 2.4 GHz RF-transceiver
  - True single chip GFSK transceiver
  - Enhanced ShockBurst™ link layer support in HW:
    - Packet assembly/disassembly
    - Address and CRC computation
    - Auto ACK and retransmit
  - On the air data rate 250 kbps, 1 Mbps or 2 Mbps
  - Digital interface (SPI) speed 0-8 Mbps
  - 125 RF channel option, with 79 (2.402 GHz-2.480 GHz) channels within 2.400 - 2.4835 GHz
  - Short switching time enable frequency hopping
  - Fully RF compatible with nRF24LXX
  - RF compatible with nRF2401A, nRF2402, nRF24E1, nRF24E2 in 250 kbps and 1 Mbps mode
- A/D converter:
  - 6, 8, 10 or 12 bit resolution
  - 14 input channels
  - Single ended or differential input
  - Full-scale range set by internal reference, external reference or VDD
  - Single step mode with conversion time down to 3 µs
  - Continuous mode with 2, 4, 8 or 16 kbps sampling rate
  - Low current consumption; only 0.1mA at 2 ksps
  - Mode for measuring supply voltage

- Analog comparator:
  - Used as wakeup source
  - Low current consumption (0.75µA typical)
  - Differential or single-ended input
  - Single-ended threshold programmable to 25%, 50%, 75% or 100% of VDD or an arbitrary reference voltage from pin
  - 14-channel input multiplexer
  - Rail-to-rail input voltage range
  - Programmable output polarity
- Encryption/decryption accelerator
  - Utilize time and power effective AES firmware
- Random number generator:
  - Non-deterministic architecture based on thermal noise
  - No seed value required
  - Non-repeating sequence
  - Corrector algorithm ensures uniform statistical distribution
  - Data rate up to 10 kB per second
  - Operational while the processor is in standby
- System reset and power supply monitoring:
  - On-chip power-on and brown-out reset
  - Watchdog timer reset
  - Reset from pin
  - Power-fail comparator with programmable threshold and interrupt to MCU
- On-chip timers:
  - Three16-bit timers/counters operating at the system clock (sources from the 16 MHz on-chip oscillators)
  - One 16-bit timer/counter operating at the low frequency clock (32.768 kHz)
- On-chip oscillators:
  - 16 MHz crystal oscillator XOSC16M
  - 16 MHz RC-oscillator RCOSC16M
  - 32.768 kHz crystal oscillator XOSC32K
  - 32.768 kHz RC-oscillator RCOSC32K
- Power management function:
  - Low power design supporting fully static stop/ standby
  - Programmable MCU clock frequency from 125 kHz to 16 MHz
  - On chip voltage regulators supporting low power mode
  - Watchdog and wakeup functionality running in low power mode
- On chip support for FS2 or nRFprobe™ HW debug
- Complete firmware platform available:
  - Hardware abstraction layer (HAL) Functions
  - Library functions
  - Gazell Wireless protocol
  - Application examples

2.2 Block diagram

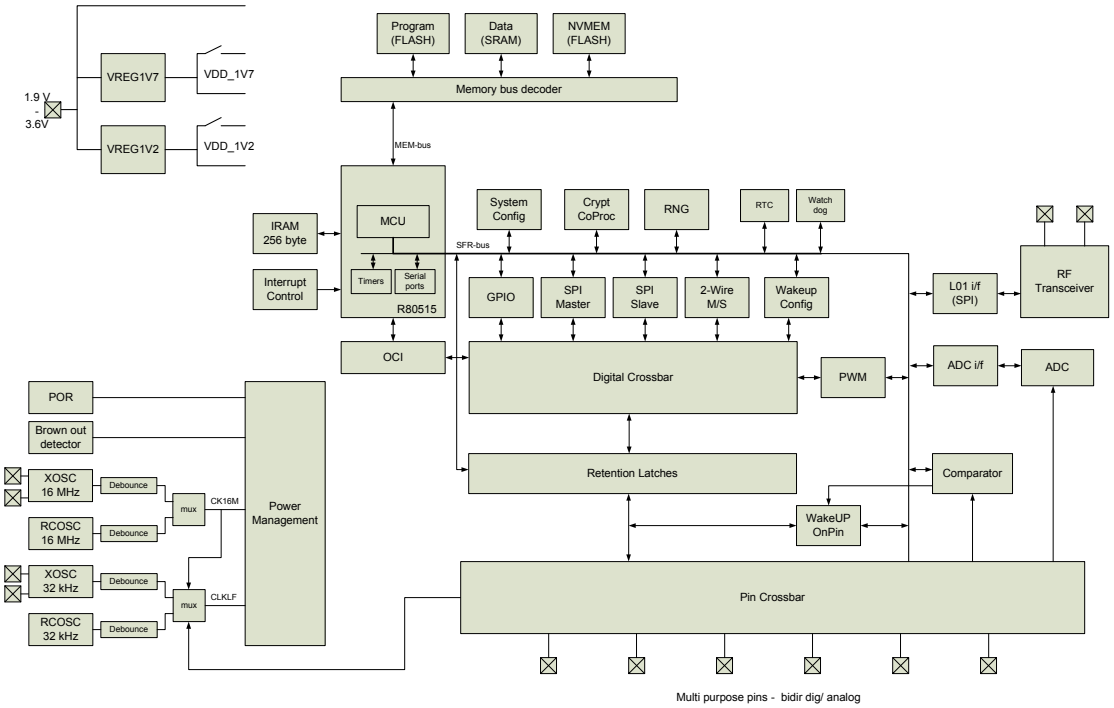

Figure 1. nRF24LE1 block diagram

To find more information on the blocks, see Table 1. below:

Name	Reference
Memory (Program, Data, NVMEM)	Chapter 5 on page 62
Power management	Chapter 11 on page 105
RF Transceiver	Chapter 3 on page 16
2-Wire	Chapter 20 on page 159
SPI (Master and Slave)	Chapter 18 on page 147
GPIO	Chapter 17 on page 132
PWM	Chapter 23 on page 174
Watchdog	Chapter 10 on page 103

Table 1. Block diagram cross references

2.3 Pin assignments

2.3.1 24-pin 4x4 QFN-package variant

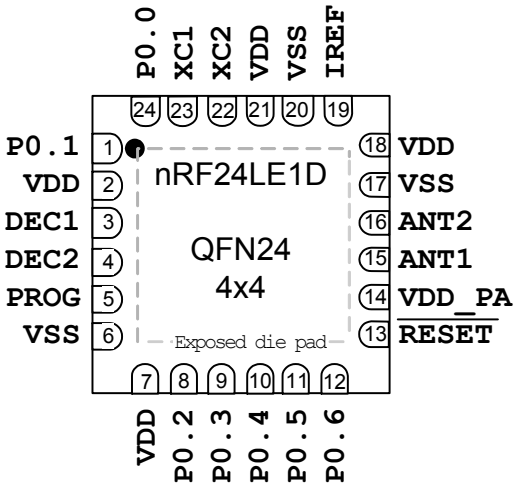

Figure 2. nRF24LE1D pin assignment (top view) for a QFN24 4×4 mm package

2.3.2 32-pin 5x5 QFN-package variant

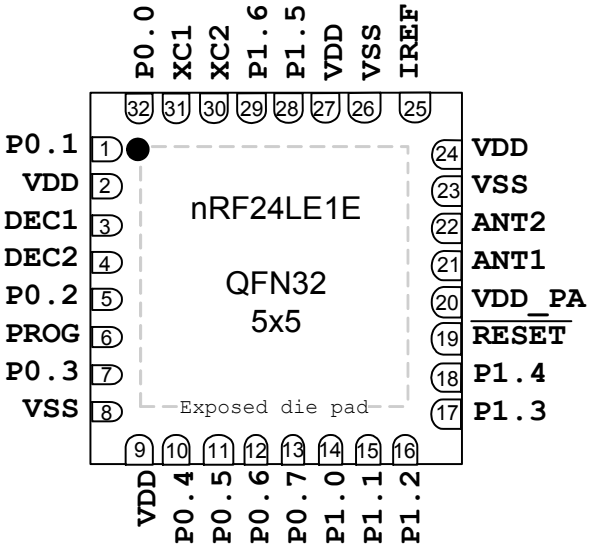

Figure 3. nRF24LE1E pin assignment (top view) for a QFN32 5×5 mm package

2.3.3 48-pin 7x7 QFN-package variant

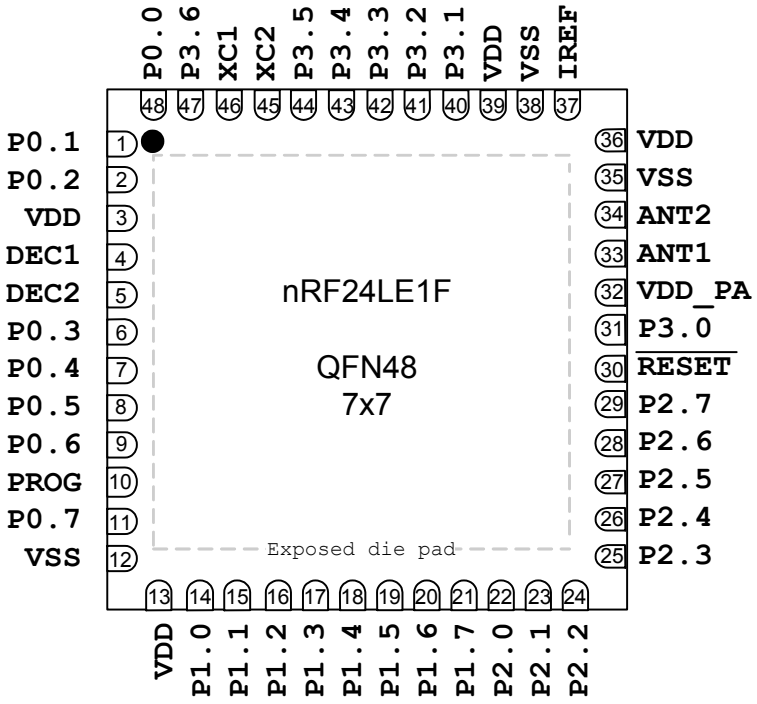

Figure 4. nRF24LE1F pin assignment (top view) for a QFN48 7×7 mm package

2.4 Pin functions

Name	Type	Description
VDD	Power	Power supply (+1.9V to +3.6V DC)
VSS	Power	Ground (0V)
DEC1 DEC2	Power	Power supply outputs for de-coupling purposes (100nF for DEC1, 33nF for DEC2)
P0.0 – P3.6	Digital or analog I/O	General purpose I/O pins. Number of I/O available depends on package type.
PROG	Digital Input	Input to enable flash programming
RESET	Digital Input	Reset for microcontroller, active low
IREF	Analog Input	Device reference current output. To be connected to reference resistor on PCB.
VDD_PA	Power Output	Power supply output (+1.8V) for on-chip RF Power amplifier
ANT1, ANT2	RF	Differential antenna connection (TX and RX)
XC1, XC2	Analog Input	Crystal connection for 16M crystal
Exposed die pad	Power/heat relief	For the nRF24LE1 QFN48 7×7mm and QFN32 5×5mm connect the die pad to GND. For nRF24LE1 QFN24 4×4mm do not connect the die pad to GND.

Table 2. nRF24LE1 pin functions

3 RF transceiver

The nRF24LE1 uses the same 2.4 GHz GFSK RF transceiver with embedded protocol engine (Enhanced ShockBurst™) that is found in the nRF24L01+ single chip RF transceiver. The RF transceiver is designed for operation in the world wide ISM frequency band at 2.400 - 2.4835 GHz and is very well suited for ultra low power wireless applications.

The RF transceiver module is configured and operated through the RF transceiver map. This register map is accessed by the MCU through a dedicated on-chip Serial Peripheral interface (SPI) and is available in all power modes of the RF transceiver module.

The embedded protocol engine (Enhanced ShockBurst™) enables data packet communication and supports various modes from manual operation to advanced autonomous protocol operation. Data FIFOs in the RF transceiver module ensure a smooth data flow between the RF transceiver module and the nRF24LE1 MCU.

The rest of this chapter is written in the context of the RF transceiver module as the core and the rest of the nRF24LE1 as external circuitry to this module.

3.1 Features

Features of the RF transceiver include:

- General
  - Worldwide 2.4 GHz ISM band operation
  - Common antenna interface in transmit and receive
  - GFSK modulation
  - 250kbps, 1 and 2Mbps on air data rate
- Transmitter
  - Programmable output power: 0, -6, -12 or -18dBm
  - 11.1mA at 0dBm output power
- Receiver
  - Integrated channel filters
  - 13.3mA at 2Mbps
  - -82dBm sensitivity at 2 Mbps
  - -85dBm sensitivity at 1 Mbps
  - -94dBm sensitivity at 250 kbps
- RF Synthesizer
  - Fully integrated synthesizer
  - 1 MHz frequency programming resolution
  - Accepts low cost ±60 ppm 16 MHz crystal
  - 1 MHz non-overlapping channel spacing at 1 Mbps
  - 2 MHz non-overlapping channel spacing at 2 Mbps
- Enhanced ShockBurst™
  - 1 to 32 bytes dynamic payload length
  - Automatic packet handling (assembly/disassembly)
  - Automatic packet transaction handling (auto ACK, auto retransmit)
- 6 data pipe MultiCeiver™ for 6:1 star networks

3.2 Block diagram

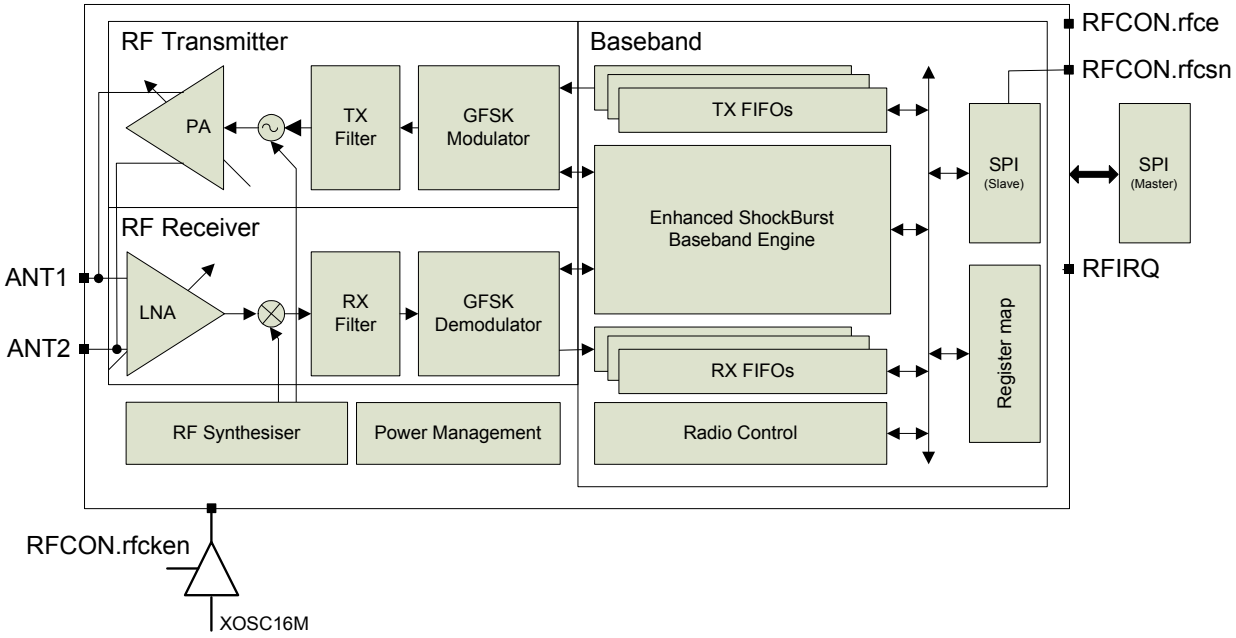

Figure 5. RF transceiver block diagram

3.3 Functional description

This section describes the different operating modes of the RF transceiver and the parameters used to control it.

The RF transceiver module has a built-in state machine that controls the transitions between the different operating modes. The state machine is controlled by SFR register `RFCON` and RF transceiver register `CONFIG`, see section 3.5 for details.

3.3.1 Operational Modes

You can configure the RF transceiver to power down, standby, RX and TX mode. This section describes these modes in detail.

3.3.1.1 State diagram

The state diagram (Figure 6.) shows the operating modes of the RF transceiver and how they function. At the end of the reset sequence the RF transceiver enters Power Down mode. When the RF transceiver enters Power Down mode the MCU can still control the module through the SPI and the `rfcsn` bit in the `RFCON` register.

There are three types of distinct states highlighted in the state diagram:

- **Recommended operating mode:** is a recommended state used during normal operation.
- **Possible operating mode:** is a possible operating state, but is not used during normal operation.
- **Transition state:** is a time limited state used during start up of the oscillator and settling of the PLL.

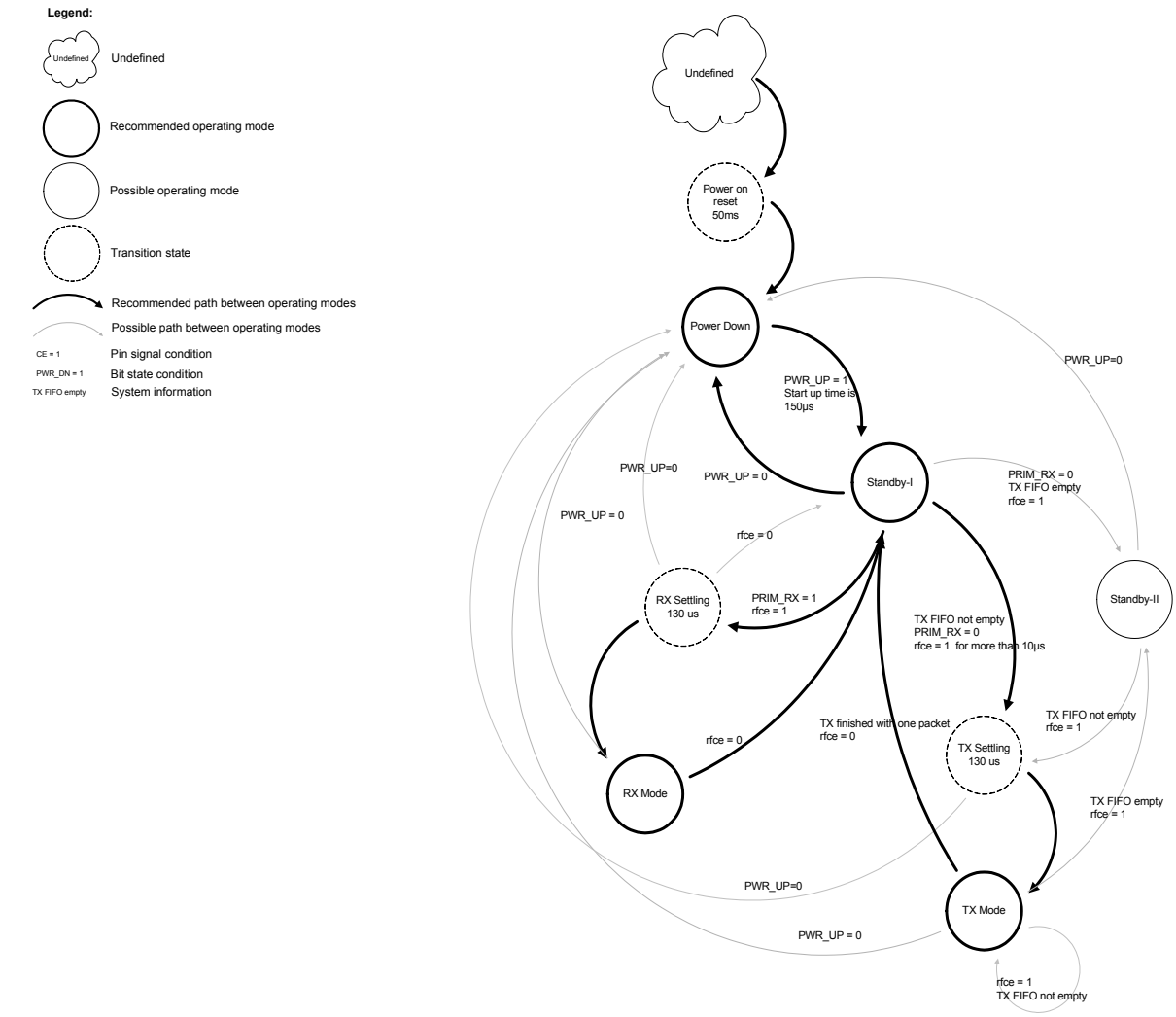

Figure 6. Radio control state diagram

3.3.1.2 Power down mode

In power down mode the RF transceiver is disabled with minimal current consumption. All the register values available from the SPI are maintained and the SPI can be activated. For start up times see Table 4. on page 20. Power down mode is entered by setting the `PWR_UP` bit in the `CONFIG` register low.

3.3.1.3 Standby modes

Standby-I mode

By setting the `PWR_UP` bit in the `CONFIG` register to 1, the RF transceiver enters standby-I mode. Standby-I mode is used to minimize average current consumption while maintaining short start up times. Change to the active mode only happens if the `rfce` bit is enabled and when it is not enabled, the RF transceiver returns to standby-I mode from both the TX and RX modes.

Standby-II mode

In standby-II mode extra clock buffers are active and more current is used compared to standby-I mode. The RF transceiver enters standby-II mode if the `rfce` bit is held high on a PTX operation with an empty TX FIFO. If a new packet is downloaded to the TX FIFO, the PLL immediately starts and the packet is transmitted after the normal PLL settling delay (130µs).

The register values are maintained and the SPI can be activated during both standby modes. For start up times see Table 4. on page 20.

3.3.1.4 RX mode

The RX mode is an active mode where the RF transceiver is used as a receiver. To enter this mode, the RF transceiver must have the `PWR_UP` bit, `PRIM_RX` bit and the `rfce` bit is set high.

In RX mode the receiver demodulates the signals from the RF channel, constantly presenting the demodulated data to the baseband protocol engine. The baseband protocol engine constantly searches for a valid packet. If a valid packet is found (by a matching address and a valid CRC) the payload of the packet is presented in a vacant slot in the RX FIFOs. If the RX FIFOs are full, the received packet is discarded.

The RF transceiver remains in RX mode until the MCU configures it to standby-I mode or power down mode. However, if the automatic protocol features (Enhanced ShockBurst™) in the baseband protocol engine are enabled, the RF transceiver can enter other modes in order to execute the protocol.

In RX mode a Received Power Detector (RPD) signal is available. The RPD is a signal that is set high when a RF signal higher than -64 dBm is detected inside the receiving frequency channel. The internal `RPD` signal is filtered before presented to the `RPD` register. The RF signal must be present for at least 40µs before the `RPD` is set high. How to use the RPD is described in Section 3.3.4 on page 21.

3.3.1.5 TX mode

The TX mode is an active mode for transmitting packets. To enter this mode, the RF transceiver must have the `PWR_UP` bit set high, `PRIM_RX` bit set low, a payload in the TX FIFO and a high pulse on the `rfce` bit for more than 10 µs.

The RF transceiver stays in TX mode until it finishes transmitting a packet. If `rfce` = 0, RF transceiver returns to standby-I mode. If `rfce` = 1, the status of the TX FIFO determines the next action. If the TX FIFO is not empty the RF transceiver remains in TX mode and transmits the next packet. If the TX FIFO is empty the RF transceiver goes into standby-II mode. The RF transceiver transmitter PLL operates in open loop when in TX mode. It is important never to keep the RF transceiver in TX mode for more than 4ms at a time. If the Enhanced ShockBurst™ features are enabled, RF transceiver is never in TX mode longer than 4 ms.

3.3.1.6 Operational modes configuration

The following table (Table 3.) describes how to configure the operational modes.

Mode	PWR_UP register	PRIM_RX register	rfce	FIFO state
RX mode	1	1	1	-
TX mode	1	0	1	Data in TX FIFO. Will empty all levels in TX FIFO[a].
TX mode	1	0	Minimum 10µs high pulse	Data in TX FIFO.Will empty one level in TX FIFO[b].
Standby-II	1	0	1	TX FIFO empty
Standby-I	1	-	0	No ongoing packet transmission
Power Down	0	-	-	-

a. If the rfce bit is held high the TX FIFO is emptied and all necessary ACK and possible retransmits are carried out. The transmission continues as long as the TX FIFO is refilled. If the TX FIFO is empty when the rfce bit is still high, the RF transceiver enters standby-II mode. In this mode the transmission of a packet is started as soon as the rfcsn is set high after an upload (UL) of a packet to TX FIFO.

b. This operating mode pulses the rfce bit high for at least 10µs. This allows one packet to transmit. This is the normal operating mode. After the packet is transmitted, the RF transceiver enters standby-I mode.

Table 3. RF transceiver main modes

3.3.1.7 Timing information

The timing information in this section relates to the transitions between modes and the timing for the rfce bit. The transition from TX mode to RX mode or vice versa is the same as the transition from the standby modes to TX mode or RX mode (130µs), as described in Table 4.

Name	RF Transceiver	Max.	Min.	Comments
Tpd2stby	Power Down ➔ Standby mode	1µs[a]		
Tstby2a	Standby modes ➔ TX/RX mode	130µs		
Thce	Minimum rfce high		10µs	
Tpece2csn	Delay from rfce pos. edge to rfcsn low		4µs	

a. This presupposes that the XO is running. Please refer to CLKLFCTRL for bit 3 in Table 59. on page 112.

Table 4. Operational timing of RF transceiver

Note: If VDD is turned off, or if the nRF24LE1 enters Deep Sleep or Memory Retention mode, the register values are lost and you must configure the RF transceiver before entering the TX or RX modes.

3.3.2 Air data rate

The air data rate is the modulated signaling rate the RF transceiver uses when transmitting and receiving data. It can be 250 kbps, 1 Mbps or 2 Mbps. Using lower air data rate gives better receiver sensitivity than higher air data rate. But, high air data rate gives lower average current consumption and reduced probability of on-air collisions.

The air data rate is set by the `RF_DR` bit in the `RF_SETUP` register. A transmitter and a receiver must be programmed with the same air data rate to communicate with each other.

The RF transceiver is fully compatible with nRF24L01. For compatibility with nRF2401A, nRF2402, nRF24E1, and nRF24E2 the air data rate must be set to 250 kbps or 1 Mbps.

3.3.3 RF channel frequency

The RF channel frequency determines the center of the channel used by the RF transceiver. The channel occupies a bandwidth of less than 1 MHz at 250kbps and 1Mbps and a bandwidth of less than 2 MHz at 2Mbps. The RF transceiver can operate on frequencies from 2.400 GHz to 2.525 GHz. The programming resolution of the RF channel frequency setting is 1 MHz.

At 2Mbps the channel occupies a bandwidth wider than the resolution of the RF channel frequency setting. To ensure non-overlapping channels in 2Mbps mode, the channel spacing must be 2 MHz or more. At 1Mbps and 250kbps the channel bandwidth is the same or lower than the resolution of the RF frequency.

The RF channel frequency is set by the `RF_CH` register according to the following formula:

$F_0 = 2400 + RF\_CH$ *MHz*

You must program a transmitter and a receiver with the same RF channel frequency to communicate with each other.

3.3.4 Received Power Detector measurements

Received Power Detector (RPD), located in register 09, bit 0, triggers at received power levels above -64 dBm that are present in the RF channel you receive on. If the received power is less than -64 dBm, RDP = 0.

The RPD can be read out at any time while the RF transceiver is in receive mode. This offers a snapshot of the current received power level in the channel. The RPD is latched whenever a packet is received or when the MCU sets rfce low.

The status of RPD is correct when RX mode is enabled and after a wait time of Tstby2a +Tdelay_AGC= 130us + 40µs. The RX gain varies over temperature which means that the RPD threshold also varies over temperature. The RPD threshold value is reduced by - 5dB at T = -40°C and increased by + 5dB at 85°C.

3.3.5 PA control

The PA (Power Amplifier) control is used to set the output power from the RF transceiver power amplifier. In TX mode PA control has four programmable steps, see Table 5. on page 22.

The PA control is set by the RF_PWR bits in the RF_SETUP register.

SPI RF-SETUP (RF_PWR)	RF output power	DC current consumption
11	0dBm	11.1mA
10	-6dBm	8.8mA
01	-12dBm	7.3mA
00	-18dBm	6.8mA

Conditions: VDD = 3.0V, VSS = 0V, T_A = 27ºC, Load impedance = 15Ω+j88Ω.

Table 5. RF output power setting for the RF transceiver

3.3.6 RX/TX control

The RX/TX control is set by PRIM_RX bit in the CONFIG register and sets the RF transceiver in transmit/ receive.

3.4 Enhanced ShockBurst™

Enhanced ShockBurst™ is a packet based data link layer that features automatic packet assembly and timing, automatic acknowledgement and retransmissions of packets. Enhanced ShockBurst™ enables the implementation of ultra low power and high performance communication. The Enhanced ShockBurst™ features enable significant improvements of power efficiency for bi-directional and uni-directional systems, without adding complexity on the host controller side.

3.4.1 Features

The main features of Enhanced ShockBurst™ are:

- 1 to 32 bytes dynamic payload length
- Automatic packet handling
- Auto packet transaction handling
  - Auto Acknowledgement
  - Auto retransmit
- 6 data pipe MultiCeiver™ for 1:6 star networks

3.4.2 Enhanced ShockBurst™ overview

Enhanced ShockBurst™ uses ShockBurst™ for automatic packet handling and timing. During transmit, ShockBurst™ assembles the packet and clocks the bits in the data packet for transmission. During receive, ShockBurst™ constantly searches for a valid address in the demodulated signal. When ShockBurst™ finds a valid address, it processes the rest of the packet and validates it by CRC. If the packet is valid the payload is moved into a vacant slot in the RX FIFOs. All high speed bit handling and timing is controlled by ShockBurst™.

Enhanced ShockBurst™ features automatic packet transaction handling for the easy implementation of a reliable bi-directional data link. An Enhanced ShockBurst™ packet transaction is a packet exchange between two transceivers, with one transceiver acting as the Primary Receiver (PRX) and the other transceiver acting as the Primary Transmitter (PTX). An Enhanced ShockBurst™ packet transaction is always initiated by a packet transmission from the PTX, the transaction is complete when the PTX has received an

acknowledgment packet (ACK packet) from the PRX. The PRX can attach user data to the ACK packet enabling a bi-directional data link.

The automatic packet transaction handling works as follows:

1. You begin the transaction by transmitting a data packet from the PTX to the PRX. Enhanced ShockBurst™ automatically sets the PTX in receive mode to wait for the ACK packet.
2. If the packet is received by the PRX, Enhanced ShockBurst™ automatically assembles and transmits an acknowledgment packet (ACK packet) to the PTX before returning to receive mode.
3. If the PTX does not receive the ACK packet immediately, Enhanced ShockBurst™ automatically retransmits the original data packet after a programmable delay and sets the PTX in receive mode to wait for the ACK packet.

In Enhanced ShockBurst™ it is possible to configure parameters such as the maximum number of retransmits and the delay from one transmission to the next retransmission. All automatic handling is done without the involvement of the MCU.

3.4.3 Enhanced Shockburst™ packet format

The format of the Enhanced ShockBurst™ packet is described in this section. The Enhanced ShockBurst™ packet contains a preamble field, address field, packet control field, payload field and a CRC field. Figure 7. shows the packet format with MSB to the left.

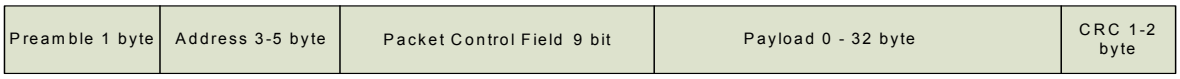

Figure 7. An Enhanced ShockBurst™ packet with payload (0-32 bytes)

3.4.3.1 Preamble

The preamble is a bit sequence used to synchronize the receivers demodulator to the incoming bit stream. The preamble is one byte long and is either 01010101 or 10101010. If the first bit in the address is 1 the preamble is automatically set to 10101010 and if the first bit is 0 the preamble is automatically set to 01010101. This is done to ensure there are enough transitions in the preamble to stabilize the receiver.

3.4.3.2 Address

This is the address for the receiver. An address ensures that the correct packet is detected by the receiver. The address field can be configured to be 3, 4 or, 5 bytes long with the `AW` register.

Note: Addresses where the level shifts only one time (that is, 000FFFFFFF) can often be detected in noise and can give a false detection, which may give a raised Packet-Error-Rate. Addresses as a continuation of the preamble (hi-low toggling) raises the Packet-Error-Rate.

3.4.3.3 Packet Control Field

Figure 8. shows the format of the 9 bit packet control field, MSB to the left.

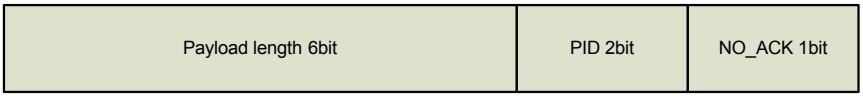

Figure 8. Packet control field

The packet control field contains a 6 bit payload length field, a 2 bit PID (Packet Identity) field and a 1 bit `NO_ACK` flag.

Payload length

This 6 bit field specifies the length of the payload in bytes. The length of the payload can be from 0 to 32 bytes.

Coding: 000000 = 0 byte (only used in empty ACK packets.) 100000 = 32 byte, 100001 = Don't care.

This field is only used if the Dynamic Payload Length function is enabled.

PID (Packet identification)

The 2 bit PID field is used to detect if the received packet is new or retransmitted. PID prevents the PRX operation from presenting the same payload more than once to the MCU. The PID field is incremented at the TX side for each new packet received through the SPI. The PID and CRC fields (see section 3.4.3.5 on page 25) are used by the PRX operation to determine if a packet is retransmitted or new. When several data packets are lost on the link, the PID fields may become equal to the last received PID. If a packet has the same PID as the previous packet, the RF transceiver compares the CRC sums from both packets. If the CRC sums are also equal, the last received packet is considered a copy of the previously received packet and discarded.

No Acknowledgment flag (NO_ACK)

The Selective Auto Acknowledgement feature controls the `NO_ACK` flag.

This flag is only used when the auto acknowledgement feature is used. Setting the flag high, tells the receiver that the packet is not to be auto acknowledged.

3.4.3.4 Payload

The payload is the user defined content of the packet. It can be 0 to 32 bytes wide and is transmitted on-air when it is uploaded (unmodified) to the device.

Enhanced ShockBurst™ provides two alternatives for handling payload lengths; static and dynamic.

The default is static payload length. With static payload length all packets between a transmitter and a receiver have the same length. Static payload length is set by the `RX_PW_Px` registers on the receiver side. The payload length on the transmitter side is set by the number of bytes clocked into the TX_FIFO and must equal the value in the `RX_PW_Px` register on the receiver side.

Dynamic Payload Length (DPL) is an alternative to static payload length. DPL enables the transmitter to send packets with variable payload length to the receiver. This means that for a system with different payload lengths it is not necessary to scale the packet length to the longest payload.

With the DPL feature the nRF24L01+ can decode the payload length of the received packet automatically instead of using the `RX_PW_Px` registers. The MCU can read the length of the received payload by using the `R_RX_PL_WID` command.

Note: Always check if the packet width reported is 32 bytes or shorter when using the `R_RX_PL_WID` command. If its width is longer than 32 bytes then the packet contains errors and must be discarded. Discard the packet by using the `Flush_RX` command.

In order to enable DPL the `EN_DPL` bit in the `FEATURE` register must be enabled. In RX mode the `DYNPD` register must be set. A PTX that transmits to a PRX with DPL enabled must have the `DPL_P0` bit in `DYNPD` set.

3.4.3.5 CRC (Cyclic Redundancy Check)

The CRC is the error detection mechanism in the packet. It may either be 1 or 2 bytes and is calculated over the address, Packet Control Field and Payload.

The polynomial for 1 byte CRC is $X^8 + X^2 + X + 1$. Initial value 0xFF.

The polynomial for 2 byte CRC is $X^{16} + X^{12} + X^5 + 1$. Initial value 0xFFFF.

No packet is accepted by Enhanced ShockBurst™ if the CRC fails.