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nRF24Z1

2.4 GHz wireless audio streamer

Product Specification v1.0

Key Features

- Low cost 0.18 µ CMOS process, 36 pin 6×6 mm QFN package
- Single chip 2.4 GHz RF transceiver
- 4 Mbit/sec RF link
- Input/output sample rate up to 48kSPS, 24 bit
- Programmable latency
- Quality of Service engine supporting up to 1.536 Mbit/s LPCM audio
- S/PDIF interface for direct connection to computer soundcard and surround receivers
- I2S interface for glue-less audio support
- SPI or 2-wire interface for up to 12 kbit/s peak bi-directional digital control/AUX data
- On-chip optional compression
- On-chip voltage regulators
- Few external components
- Uses global 2.4 GHz band

Applications

- CD quality headsets
- Headsets
- Speakers
- Surround speakers
- Microphone
- Audio streaming from computer soundcard to HiFi system

2010-11-03

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Revision History

Date	Version	Description
November 2010	1.0	Product specification

Contents

1 Introduction

nRF24Z1 provides a true single chip system for CD quality audio streaming of up to16 bit 48 kSPS audio, supporting up to 24 bit 48 kSPS input. I2S and S/PDIF interfaces are supported for audio input/output (I/O). Seamless interfacing of low cost A/D and D/A for analog audio input and output. SPI or 2-wire (I2C compatible) control serial interfaces. Embedded voltage regulators yield maximum noise immunity and allow operation from a single 2.0V to 3.6V supply.

1.1 Quick reference data

Parameter	Value	Unit
Minimum supply voltage	2.0	V
Temperature range	-20 to +80	°C
Peak supply current in transmit @ -5dBm output power	15	mA
Peak supply current in receive mode	32	mA
Supply current in power down mode	5	µA
Maximum transmit output power	0	dBm
Audio sample rate	8 to 48	kSPS
Audio resolution	16	bit
Receiver sensitivity	-80	dBm

Table 1.nRF24Z1 quick reference data

1.2 Prerequisites

In order to fully understand this product specification, a good knowledge of electronic and software engineering is necessary.

1.3 Writing conventions

This product specification follows a set of typographic rules to make the document consistent and easy to read. The following writing conventions are used:

- Commands, bit state conditions, and register names are written in `Courier New`.
- Pin names and pin signal conditions are written in **`Courier New bold`**.
- Cross references are underlined and highlighted in blue.

2 Product overview

2.1 Pin assignments

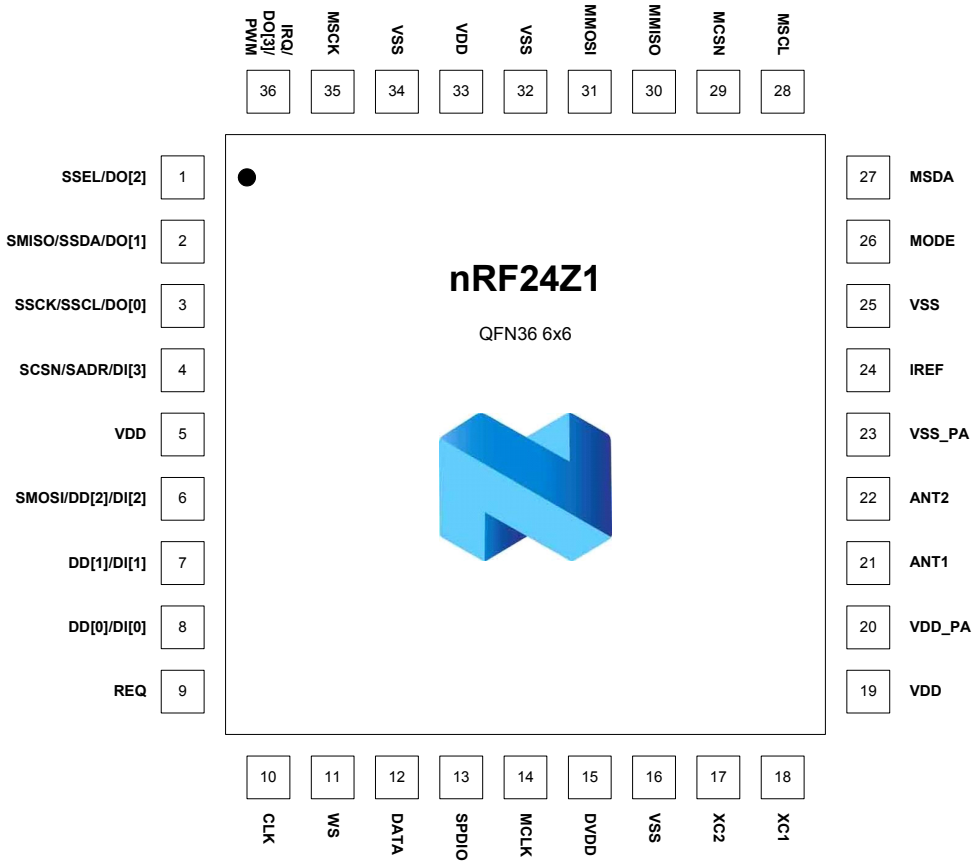

Figure 1. Pin assignments

2.2 Pin functions

Table 2. shows the nRF24Z1 pin functions. Note that pin functions depend on the functional mode of the device (ATX; audio source or ARX; audio recipient) and the interface of choice.

Pin number	Pin name		Pin function		Description	
	Serial slave interface	ARX GPIO	Serial slave interface	ARX GPIO interface	ATX/ARX w. serial slave interface	ARX w. GPIO interface
1	SSEL	DO[2]	Digital Input	Digital Output	Slave interface select 1:2-wire, 0:SPI	GPIO out bit #2
2	SMISO/SSDA	DO[1]	Digital Output / Digital IO		Slave SPI serial out / Slave 2-wire data (bidir)	GPIO out bit #1
3	SSCK/SSCL	DO[0]	Digital Input	Digital Output	Slave SPI clock / Slave 2-wire clock	GPIO out bit #0
4	SCSN/SADR	DI[3]	Digital Input		Slave SPI slave select / Address select 2-wire slave	GPIO in bit #2
5	VDD		Power		Power Supply (2.0-3.6 V DC)	
6	SMOSI/DD[2]	DI[2]	Digital Input		Slave SPI serial in / Direct data in bit #2	GPIO in bit #3
7	DD[1]	DI[1]	Digital Input		Direct data in bit #1	GPIO in bit #1
8	DD[0]	DI[0]	Digital Input		Direct data in bit #0	GPIO in bit #0
			ATX	ARX		
9	REQ		Dig. Out	Dig. In	For ATX not connected, for ARX connect to VSS	
10	CLK		Dig. IO	Dig. Out	I2S bit clock	
11	WS		Dig. IO	Dig. Out	I2S word clock	
12	DATA		Dig. In	Dig. Out	I2S word clock	
13	SPDIO		Dig. In	Dig. Out	S/PDIF interface	
14	MCLK		Digital Output		256X sample rate clock to ADC or DAC	
15	DVDD		Regulator output		Digital voltage regulator output for decoupling	
16	VSS		Power		Ground (0V)	
17	XC2		Analog output		Crystal Pin 2	
18	XC1		Analog input		Crystal Pin 1	
19	VDD		Power		Power Supply (2.0-3.6 V DC)	
20	VDD_PA		Regulator output		DC output (+1.8V) for RF interface (ANT1, ANT2)	
21	ANT1		RF		Antenna interface 1	

Pin number	Pin name		Pin function	Description	
22	ANT2		RF	Antenna interface 2	
23	VSS_PA		Power	Ground (0V)	
24	IREF		Analog input	Connection to external Bias reference resistor, or RESET if pulled to VDD	
25	VSS		Power	Ground (0V)	
26	MODE		Digital Input	nRF24Z1 function 1 : audio transmitter, 0: audio receiver	
27	MSDA		Digital IO	Master 2-wire bi-directional data	
28	MSCL		Digital IO	Master 2-wire bi-directional clock	
29	MCSN		Digital Output	Master SPI primary slave select (active low)	
30	MMISO		Digital Input	Master SPI serial input	
31	MMOSI		Digital Output	Master SPI serial output	
32	VSS		Power	Ground (0V)	
33	VDD		Power	Power Supply (2.0-3.6 V DC)	
34	VSS		Power	Ground (0V)	
35	MSCK		Digital Output	Master SPI clock	
36	IRQ	DO[3]/PWM	Digital Output	Interrupt request	GPIO out bit #3 / PWM output

Table 2. nRF24Z1 pin functions

3 Architectural overview

nRF24Z1 is a 4 Mbit/s single chip RF transceiver that operates in the world wide 2.4 GHz license free ISM band. The nR24Z1 is based on the proven nRF24xx radio- and ShockBurst™ platforms from Nordic Semiconductor.

The device offers a wireless channel for seamless streaming of LPCM or compressed audio in parallel with a low data rate control channel. To enable this, the device offers the following features in addition to the nRF24xx RF platform:

- Standard digital audio interfaces (I2S, S/PDIF)
- Fully embedded Quality of Service engine handling all RF protocol and RF link tasks.
- SPI and 2-wire master and slave control interfaces
- GPIO pins

As all processing related to audio I/O, RF protocol and RF link management is embedded, the nRF24Z1 offers a transparent audio channel with capacity of up to 1.54 Mbit/s, with no true time processing needed. The nRF24Z1 can be utilized in systems without external microcontroller or used in conjunction with a simple microcontroller that only need to handle low speed tasks over the serial or parallel ports (for example, volume up/down).

A block schematic of a typical nRF24Z1 based system is illustrated in Figure 2.

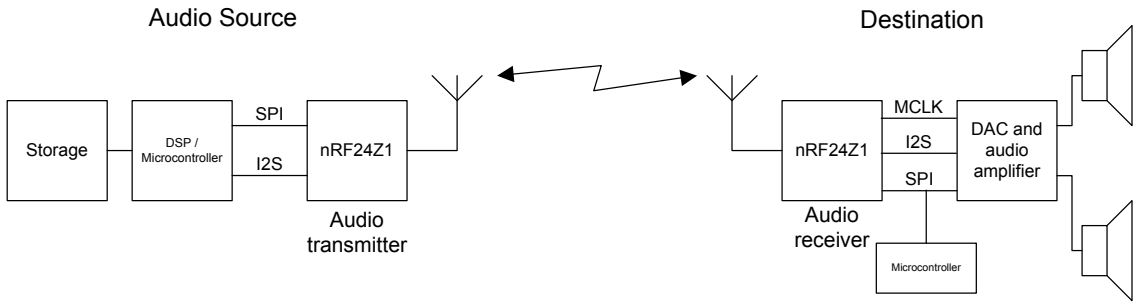

Figure 2. Typical audio application using nRF24Z1

In this system a DSP or microcontroller feeds data from a storage device to an nRF24Z1 using standard audio format (I2S). An nRF24Z1 pair transfers audio data from the source and presents it to a stereo DAC on the receiving side. From the application side, the nRF24Z1 link will appear as an open channel (like a cable).

Initial configuration of nRF24Z1 is done by the microcontroller through an SPI or 2-wire control interface.

3.1 Fundamental modes of operation

A wireless system streaming audio will have an asymmetrical load on the RF link as audio data is fed from an audio source (for example, CD player) to a destination (for example, loudspeakers). From the destination back to the audio source, only service- and control communication is needed.

nRF24Z1 is used both on the audio source side (for example in a CD player) transmitting audio data, and in the recipient (loudspeaker) side receiving audio data. Due to the asymmetry, nRF24Z1 has two main modes set by external pin **MODE**, depending on whether it represents the transmitter or the receiver. The two modes have significant differences both in internal and I/O functionality.

To differentiate between these two modes of operation, the following notation is introduced:

- Audio transmitter: ATX; nRF24Z1 on the audio source side, transmitting audio data
- Audio receiver: ARX; nRF24Z1 on the destination side, receiving audio data

In this context, the terms ‘transmitter’ and ‘receiver’ are referring to the directional flow of the audio; the nRF24Z1 radio transceiver is always operating in half-duplex (meaning bi-directional) mode.

3.2 Communication and data transfer principle

3.2.1 Data channel definition

To differentiate between audio data and other control- and status information, the data traffic between the ATX/ARX has been organized into two data channels, for the example used in this product specification.

The audio channel is defined as the communication channel sourcing audio data from the ATX to the ARX. The audio data is divided into two categories; real time data from the audio source and retransmitted audio information. When audio information is lost, the ARX requests retransmission of the lost packets. Real time audio bit rate is constant, whereas the amount of retransmitted audio varies over time.

The nRF24Z1 control channel is a two-way, low data rate channel superimposed on the audio stream. The audio transmitter is designated master, meaning that when an RF link is active, the 2-wire, SPI, GPIO and internal registers in the audio receiver can be seen and controlled as a virtual extension of the audio transmitters own I/O and registers. The implications of this is that external devices like audio DAC or volume control components connected to the audio receiver can be controlled by input to the ATX. User

actions (meaning push of a button) on the audio receiver side are similarly fed back to and can be processed on the audio-transmitter side.

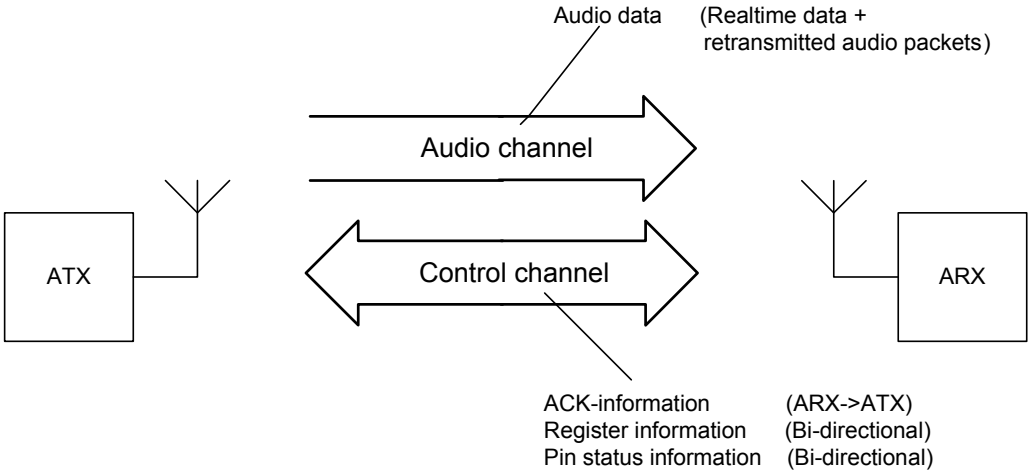

Figure 3. nRF24Z1 communication channel principle

3.2.2 Data flow- and organization

Figure 4. illustrates the communication principle of an nRF24Z1 wireless link. Data is transmitted from the ATX to the ARX on a cyclic basis.

ATX data is organized in frames transmitted with frequency 1/tp. A data frame contains the real time audio data and retransmitted audio data requested by the ARX. Poor operating conditions (meaning excessive range and/or high amount of interference) will result in a higher amount of retransmitted audio data per frame.

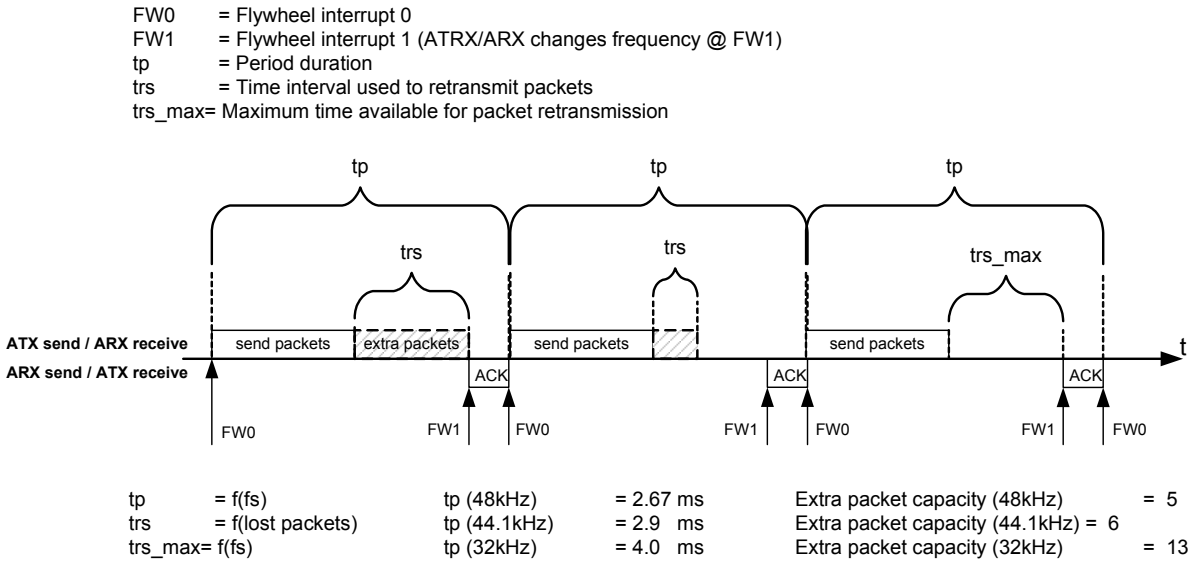

Figure 4. nRF24Z1 data streaming principle

Figure 4. also illustrates how period length, frame size and retransmission capacity vary with sample rate and time.

Audio data is organized in stereo samples (SS). The stereo samples are in turn organized in data packets consisting of 16 stereo samples. A data packet also contains preamble, recipient address, packet id, compression information, CRC-string and a limited amount of control and register data.

A data frame consists of a segment of real time data. In addition, the frame contains audio packets requested by the ARX for retransmission. The maximum number of packets for retransmission depends on the sample rate of choice.

When the ARX has received the data frame, an acknowledge packet is generated and sent to the ATX. This packet consists of acknowledge information (requesting retransmission of corrupt/lost packets) and control and status information.

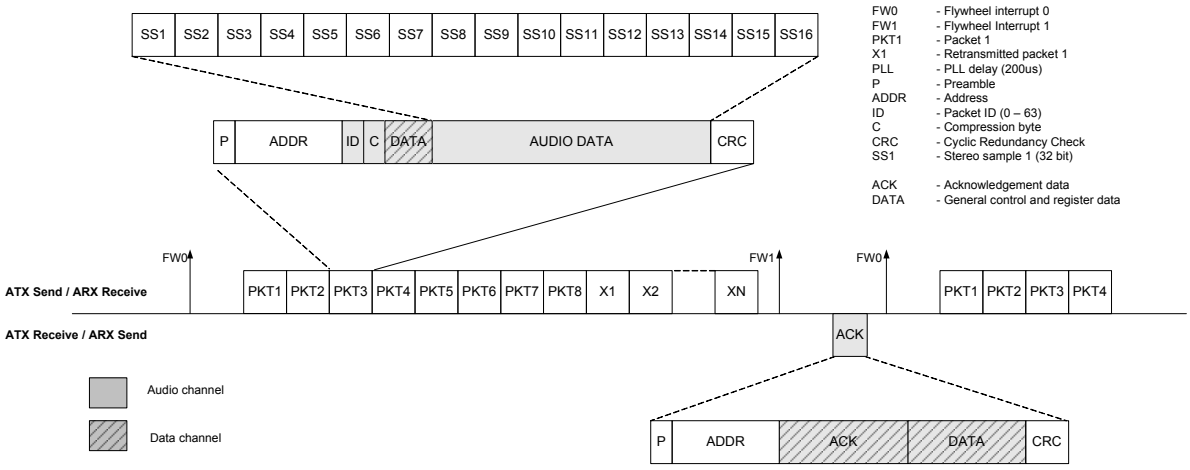

Figure 5. nRF24Z1 data frame and packet organization

3.3 Mode- and Interface alternatives

A number of interfaces are available for the nRF24Z1 device. The available interfaces depend on the nRF24Z1 mode of operation and the type of data to be transferred. Data is divided into two categories; audio data (audio channel) and configuration/status data (control channel). Figure 5. illustrates the available data interfaces for the various modes of operation.

Interface options are illustrated by grey bubbles, whilst functionality / operation modes are shown in white. Relevant configuration settings are shown in the links drawn between the bubbles. Note that interface choice is made by a combination of pin and register settings. Refer to chapter 6 on page 30 for details.

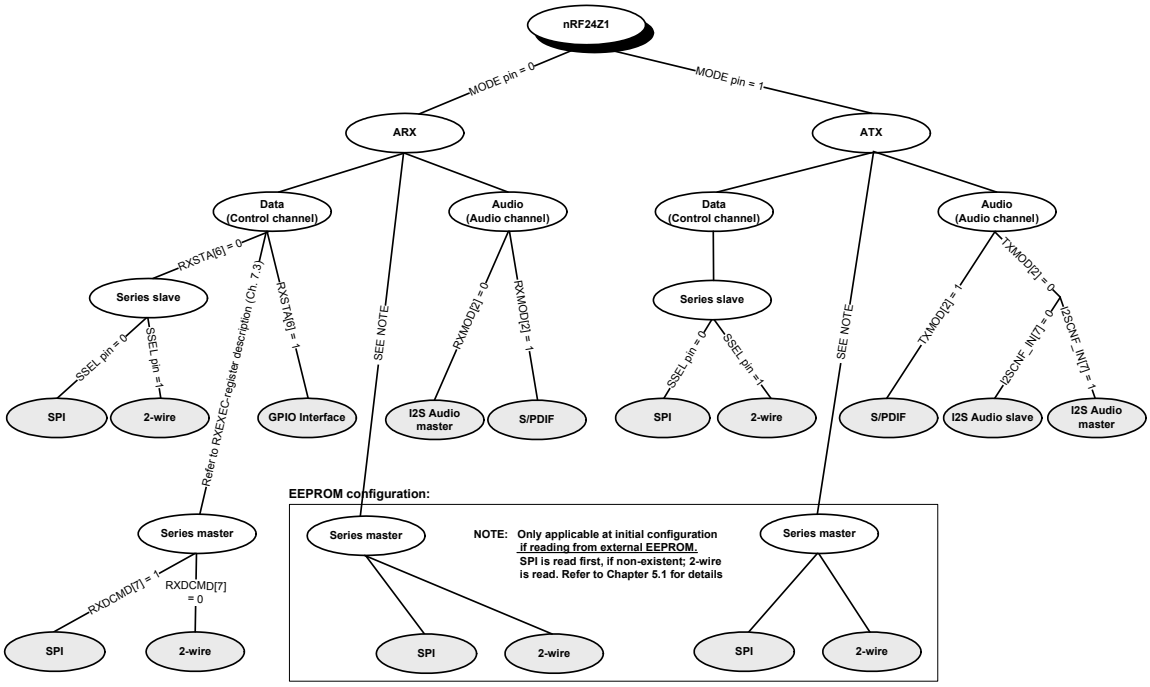

Figure 6. nRF24Z1 functional modes and interface alternatives

3.4 Audio transmitter (ATX)

When an nRF24Z1 is applied at the audio source side of the RF link, MODE must be high and nRF24Z1 becomes an audio transmitter (ATX). The block schematic of nRF24Z1 in ATX mode can be seen in Figure 7. on page 15

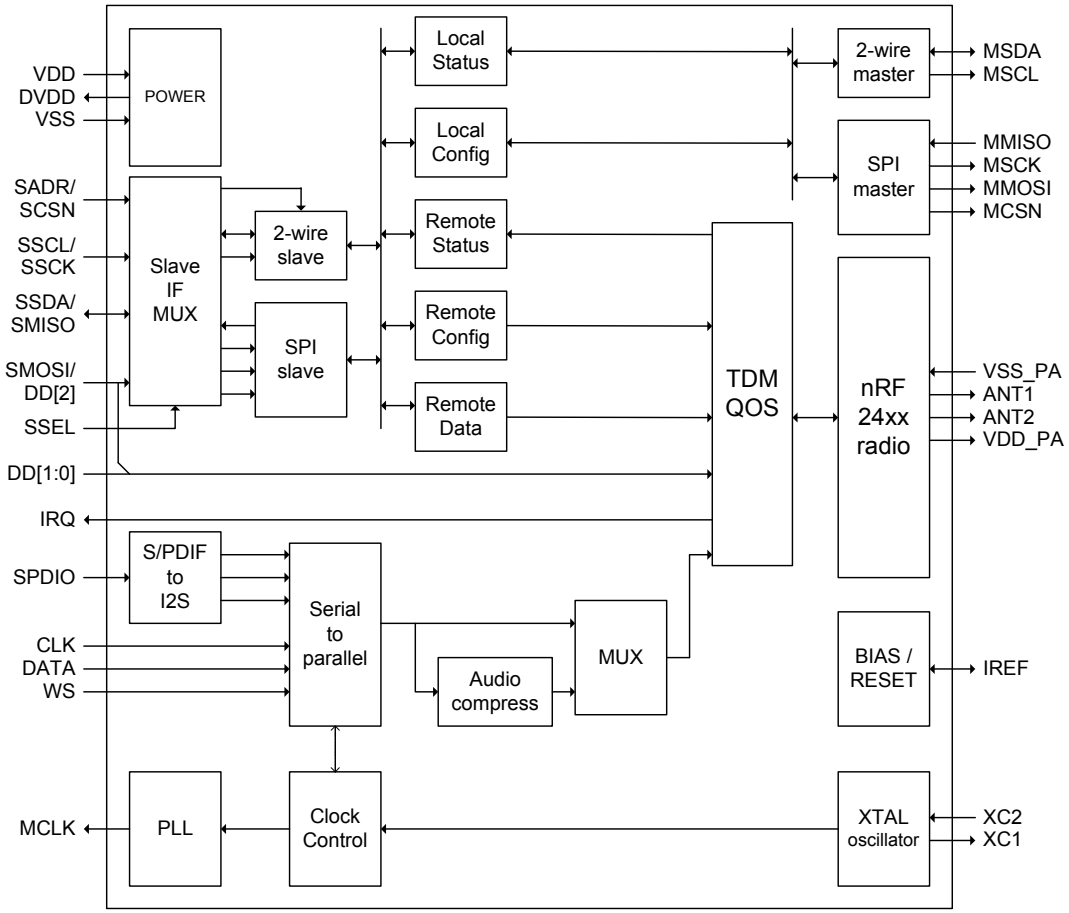

Figure 7. nRF24Z1 ATX mode block diagram

The I2S or S/PDIF interfaces can be used for audio data input.

3.4.1 I2S audio input

For seamless input from audio sources physically close to nRF24Z1, I2S is the preferred interface. The I2S interface consists of pins **CLK**, **DATA** and **WS**. This interface supports the three fundamental sampling rates 32, 44.1 and 48 kSPS plus these rates scaled by 0.5 or 0.25; yielding a total of nine sample rates : 8, 11.025, 12, 16, 22.05, 24, 32, 44.1 and 48 kSPS. Data may be in 16 or 24 bit format.[1] The nRF24Z1 can be configured to automatically detect the applied data rate.

I2S may be used with an external stereo ADC for analog audio sources. The nRF24Z1 offers a sampling rate clock (fS) of 256 times the audio fundamental sampling rate. The sample rate clock is available on the **MCLK** pin and may be used as system clock for the ADC.

1. Only 16-bit format can be transferred uncompressed within the available 1.54 Mbit/s data rate.

3.4.2 S/PDIF audio input

The ATX also offers a (CMOS level) S/PDIF input on pin **SPDIO**. This interface supports 32, 44.1 or 48 kSPS sampling rates with resolution of 16, 20 or 24 bit, as well as linear and nonlinear audio according to IEC standards. See section 3.4.2 on page 16 for details.

3.4.3 Serial control (slave) interfaces

When ATX is controlled by an external MCU, configuration and control data for the audio transmitter and the linked audio receiver may be entered through a 2-wire or SPI slave serial interface. The same interface is used for reading back status information. The register map is identical for both interfaces, but only one of the interfaces (selected by **SSEL** pin) may be used in a given application.

The two interfaces are:

- SSEL = 0; SPI (pins **SCSN**, **SSCK**, **SMISO**, **SMOSI**)
- SSEL = 1; 2-wire (pins **SADR**, **SSCL** and **SSDA**)

Pin **SADR** is not part of a standard 2-wire interface but selects one of two possible bus addresses for the nRF24Z1.

3.4.4 Master interfaces

For standalone operation of nRF24Z1, a serial EEPROM or FLASH memory may be connected to an SPI or 2-wire master interface. If a memory is present at any of these interfaces during power up or reset, the device will read default configuration data from the memory.

The SPI master is found on pins **MCSN, MMISO, MMOSI** and **MSCK** and 2-wire master on pins **MSDA** and **MSCL**.

3.4.5 Direct data input pins

The ATX has two general purpose input pins, **DD**[1:0]. The status of these pins may be transmitted directly to the ARX without the use of an external MCU. When SSEL is set high (2-wire interface selected), an additional direct data pin (**DD**[2]) is available.

If the logic level on pins **DD**[2:0] are mirrored (copied) over the control channel, ARX pins **DO**[2:0] will output identical levels.

These pins may thus be used to switch on/off audio receiver peripherals without microprocessor activity.

3.4.6 Interrupt output

The nRF24Z1 can interrupt the external application through pin **IRQ** based on a number of sources (meaning no audio input detected, loss of RF communication and so on.)

Once **IRQ** has triggered external MCU, interrupt status can be read through the serial slave interface.

3.5 Audio Receiver (ARX)

When nRF24Z1 is put at the destination side of the RF link, MODE must be low and nRF24Z1 becomes the audio receiver (ARX). ARX can be configured with GPIO interface or slave interface. The respective block schematics of nRF24Z1 in ARX mode can be seen in Figure 8. and Figure 9. on page 18 I2S or S/PDIF are now used for audio or other real time data output.

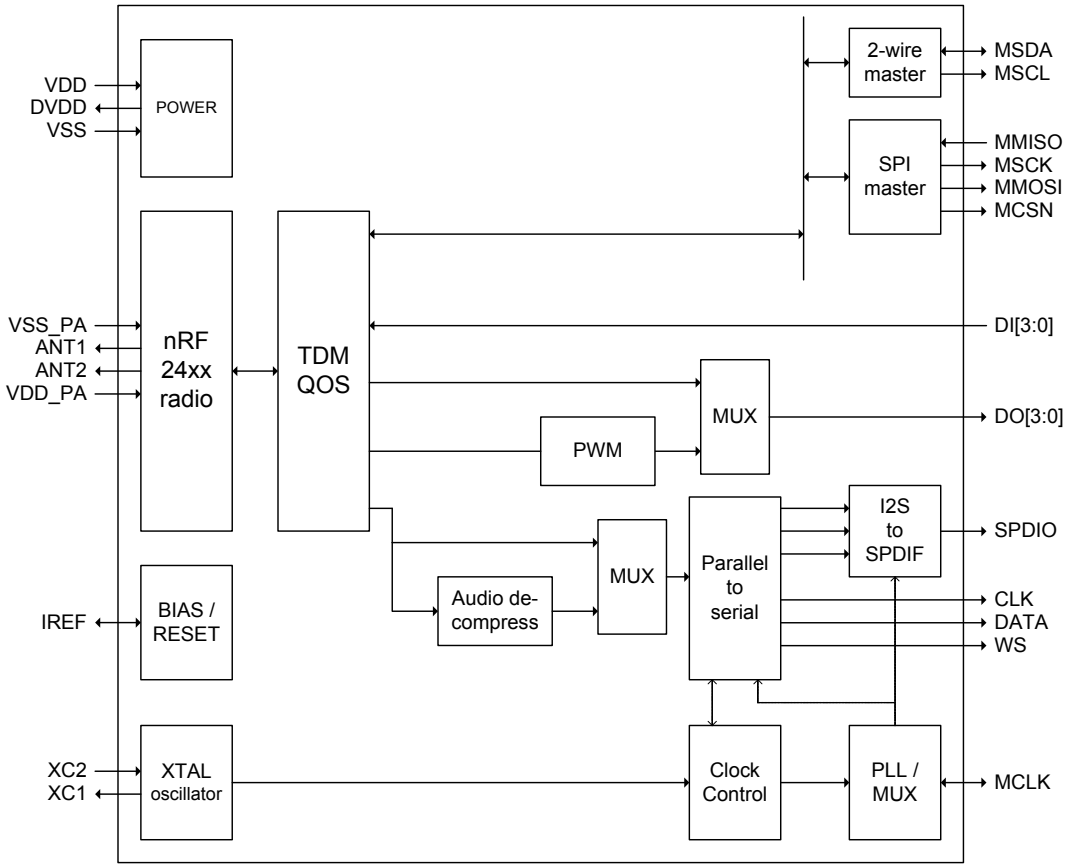

Figure 8. nRF24Z1 ARX mode with GPIO interface, block diagram

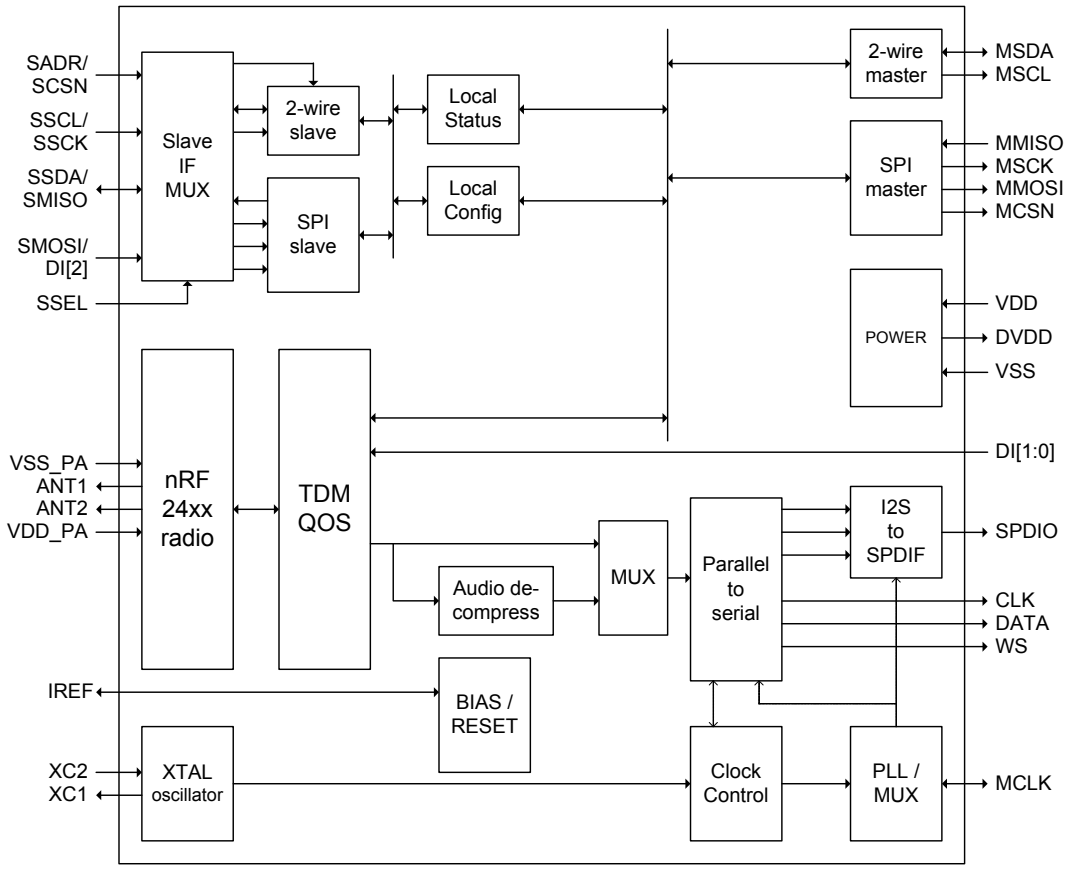

Figure 9. nRF24Z1 ARX mode with slave interface, block diagram

After a link has been established, you can control the SPI and 2-wire master on the ARX from the ATX. This feature enables the ATX to remotely control serial peripheral devices on the ARX (audio DACs, amplifiers and so on).

3.5.1 I2S audio output

Audio output to devices physically close to nRF24Z1 (typically a stereo DAC) are normally driven by the I2S output (pins **CLK, DATA** and **WS**). This interface supports the following sample rates: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1 and 48 kSPS. Audio rate on the ATX and ARX side must be identical. Data are in 16-bit format.

In audio receiver mode, the **MCLK** pin provides a sampling rate clock (fS) for an external DAC that is 256 times the audio fundamental sampling rate.

3.5.2 S/PDIF audio output

The ARX provides an S/PDIF (full swing CMOS) output on pin **SPDIO**. This interface supports 32, 44.1 and 48 kSPS, 16 or 24 bit data. Both linear and nonlinear audio may be received according to IEC standards, see section 6.2.2 on page 31 for more information.

3.5.3 Master interfaces

A serial EEPROM or FLASH memory may be connected to an SPI or 2-wire master interface. If a memory is present at any of these interfaces during power up or reset, the nRF24Z1 will read default configuration data from that memory. If not, hard coded default values will be used.

During audio receiver configuration, the SPI master (pins **MMSCK, MMISO, MMOSI, MCSN**) is operated at 1 MHz with the SPI format set to CPOL=0,CPHA=0 for EEPROM/FLASH compatibility. After a link has been established, the user may control the SPI master from the audio transmitter. The available clock speed is up to 8 MHz over the full operational range of the nRF24Z1.

During start-up, the audio receiver operates the 2-wire master (MSDA, MSCL) interface at 100 kHz. After a link has been established, you may control the 2-wire master from the audio transmitter to 100 kHz, 400 kHz or 1 MHz.

3.5.4 Serial control (slave) interfaces

When the ARX is controlled by an external MCU, configuration and control data for the audio receiver may be entered via a 2-wire or SPI slave serial interface. The same interface is used for reading back status information. The register map is identical for both interfaces, but only the interface selected by the **SSEL** pin may be used in a given application.

The two interfaces are:

- SSEL = 0; SPI (pins **SCSN, SSCK, SMISO, SMOSI**)
- SSEL = 1; 2-wire (pins **SADR, SSCL** and **SSDA**)

Pin **SADR** is not part of a standard 2-wire interface but selects one of two possible bus addresses for the nRF24Z1.

3.5.5 Parallel port and PWM

Alternatively to the serial slave interfaces, the **ARX** can be configured with an 8 bit parallel port, which can be controlled and read from the audio transmitter. The four input pins **DI**[3:0] are continuously monitored when a link is up. Changes on any of these inputs will be sent back to the audio transmitter where it can be accessed in a register (through the serial control interface). The audio receiver can also be programmed to wake up from power down mode upon a change of state on any of these pins.

There are four outputs **DO**[3:0] controlled from the audio transmitter. Pins **DO**[1] and **DO**[3] may be programmed for high current in order to drive application PCB LEDs or standard CMOS gates.

DO[3] may be programmed to provide a PWM signal, where the output duty cycle is programmable with 8-bit resolution from the audio transmitter. Note that this PWM cannot be used as an audio DAC.

The output pins **DO**[3:0] may also function as slave select signals if multiple slaves are present on the ARX SPI master bus.

3.6 Blocks and functionality common to the ATX abd ARX

3.6.1 Crystal oscillator

The crystal oscillator will provide a stable reference frequency with low phase noise for the radio and audio functions. See the section 17.2 on page 78 for more detail.

3.6.2 Radio transceiver

The RF transceiver part of the circuit is a member of nRF24xx family of low-power highly integrated 2.4 GHz ShockBurst™ transceivers. The transceiver interface is optimized for high speed streaming of up to 4 Mbps. Output power and some radio protocol parameters can be controlled by the user through the Quality of Service (QoS) module.

3.6.3 Quality of Service (QoS) engine

The primary function of the QoS engine is to ensure robust communication between the ATX and the ARX in an audio streaming application.

Various data streams with different properties are handled. The available bandwidth is shared between audio data, service data and remote data.

Data integrity is ensured through a number of RF protocol features:

- Packets of data are organized in frames with each packet consisting of an RF address, payload and CRC.
- Packets that are lost or received with errors are handled by the error correction level of the quality of service engine; a two way, acknowledge protocol:
  - When a packet is received by ARX, it is registered and CRC is verified. After ARX has received a frame, it sends a packet back to ATX acknowledging the packets successfully transferred. Packets lost or received with errors, are re-transmitted from ATX in the next frame.
- The information (audio data) is dispersed over the 2.4 GHz band by use of an adaptive frequency hopping algorithm. This enables the nRF24Z1 link to cope with RF propagation challenges like reflections, multi-path fading and avoiding heavily trafficked areas of the 2.4 GHz band. Handling coexistence scenarios with other contemporary RF systems using the 2.4 GHz ISM band, is increasingly important.

The nRF24Z1 is constantly monitoring the quality of the RF link. Link quality information is available for external control devices in registers. nRF24Z1 can also be set to interrupt external controller devices upon poor link quality before the RF link is lost. An external controller device can take action to improve link quality or warn end user if RF link margins are poor.

The secondary function of the QoS module is to run a link initialization algorithm which manages initial connect and re-connect if link is lost (for example: out of range) between paired nRF24Z1s. Several schemes are available to enable nRF24Z1 connection without end-user involvement.

3.6.4 Audio compression/decompression

An optional low latency compression option is available as an alternative to streaming of uncompressed audio.

The compression option enables 24-bit samples to be compressed to a 16-bit format by removing the least significant bits in the samples. All samples in a packet are scaled to the same exponent.

3.6.5 Power supply regulators

The power section of nRF24Z1 offers linear regulated supply to all internal parts of the device. This makes the device very robust towards external voltage supply noise and isolates (audio) devices in an application from any noise generated by the nRF24Z1.

3.6.6 Bias reference/RESET

The **IREF** pin sets up the bias reference for the nRF24Z1 by use of an external resistor. Shorting **IREF** to **VDD** will reset the device. When **IREF** pin is released, nRF24Z1 runs a full configuration procedure.

4 Operation overview

4.1 Power on/RESET sequence

When a power supply voltage is connected, nRF24Z1 performs a power-on-reset. Reset is held until the supply voltage has been above the minimum supply voltage for a few milliseconds. Pulling **IREF** to **VDD** will also put the device into reset.

When reset (power on or IREF high) is released, the device needs to be configured. There are two alternatives for nRF24Z1 configuration:

Upon reset release, nRF24Z1 will look for an external EEPROM/FLASH memory connected to the SPI master interface. If such a memory is present, configuration data is loaded, which implies that registers values are read from the external memory. If no memory is present on the SPI master interface, the procedure is repeated on the 2-wire master interface. If no SPI EEPROM is connected, MMISO must have an external pull down resistor to ground. Data in the external memory device will override any initial contents of nRF24Z1 registers.

If no external memory is present:

An external micro processor must configure the nRF24Z1 ATX and ARX through the slave SPI or 2-wire serial interface, otherwise hard coded initial register contents are used.

Note: A combination of the two power-up sequences may be used. One likely scenario is that the ATX is configured by an external MCU and that the ARX is configured from an external EEPROM/FLASH memory device.

nRF24Z1 will then start a link initialization procedure based on the link configuration data. The value of the **MODE** pin determines whether it will be in ATX or ARX mode.

In case an external EEPROM or Flash memory is present, please note that no access to the 2-wire slave interface should be started until configuration data from EEPROM/Flash is read in by the nRF24Z1.

4.2 RF link initialization

The process of establishing a communication link between the ATX and the ARX is referred to as RF link initialization. This involves the ATX systematically probing the frequency band in search for an active ARX with the correct identity. Once found, the ATX/ARX are synchronized before audio transmission starts.

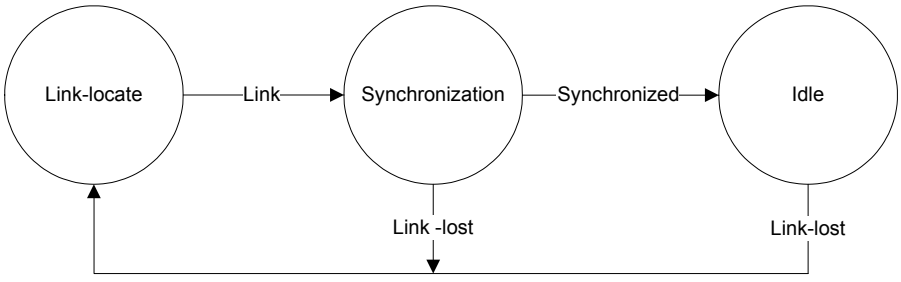

Figure 10. Link initialization algorithm

4.2.1 Idle state

The nRF24Z1 link initialization algorithm will be in idle state when a link is established. Once established, the frequency hopping engine is initiated and synchronized.

4.2.2 Link-locate state

If the link between ATX and ARX is broken, a special link-locate routine is initiated on both sides in order to re-establish the link. See Figure 10. on page 22. During initialization, nRF24Z1 uses the NLCH first positions of the frequency hopping table.

4.2.2.1 Link-locate on ATX

The ATX tries to establish a link with ARX by iteratively sending short search packets on all available channels until an acknowledge signal is received from the ARX. The ATX will send one packet on each channel and wait for acknowledge for a time long enough to secure that the ARX has time to respond. The accumulated time used by the ATX while looping through all available channels, is defined as the ATX-loop-time. After receiving an acknowledge packet from the ARX, the ATX will enter the synchronization state as illustrated in Figure 10. on page 22 . The dwell time for linking (tDWELL_L) is approximately 600 ms. The dwell time is defined as the time duration of which the ATX/ARX is active at a given frequency before changing frequency position.

4.2.2.2 Link-locate on ARX

The ARX tries to establish a link with the ATX by listening for incoming search packets on all available channels. When a search packet is received, the ARX will proceed by sending one acknowledge packet to confirm a feasible link. The ARX will listen for incoming search packets on each channel for a fixed time longer than the ATX-loop-time. This guarantees that at least one search packet gets through on each available channel used by the ARX, as long as this channel is not being occupied by another radio device. After sending the acknowledge packet, the ARX will enter the synchronization state. The dwell time is approximately (NLCH+1)×600 µs.

4.2.3 Synchronization state

This state synchronizes the frequency hopping engine on ATX and ARX, ensuring that both units follows the same hopping sequence. The initial start frequency is found in link-locate mode.

4.3 Audio channel

The input audio data can be one of the following common digital audio formats:

I2S (audio serial) interface:

- Left justified, I2S and right justified.

S/PDIF interface:

- Consumer Linear PCM Audio as described in IEC 60958-3. As the nRF24Z1 has a single ended CMOS interface, external adaptation circuitry is needed in order to fulfil the electrical requirements.

- Non-Linear PCM Audio as described in IEC 61937-1 (General) and IEC 61937-2 (Burst-info). The nRF24Z1 communication channel is transparent and is thus compatible with the audio compression algorithm formats described in IEC 61937-3 to 61937-7.

In the ATX, the input audio stream format is converted to the nRF24Z1 RF protocol and transferred over the air.

Upon reception in the ARX, the received data are validated and converted to the specified audio output format and fed to the corresponding audio output interface.

4.3.1 Audio receiver clock-rate recovery

Maintaining equal data rates on both sides of RF link is crucial in any RF system streaming true time data. This implies keeping the master clock frequency (MCLK) for the DAC on the receiving side, equal to the clock frequency used to feed data into the RF device on the transmitter side.

If these two clocks are not identical, the receiving end will either run out of samples for the DAC (ARX clock frequency > ATX clock frequency) or overflow (ARX clock frequency < ATX clock frequency), skipping samples.

This problem is solved in the nRF24Z1 device without the need for a tight tolerance crystal or extensive digital filtering.

As long as the nRF24Z1 QoS engine is able to maintain the RF link, the ARX locks its master clock output (MCLK) to the rate of the incoming audio stream. The MCLK signal on the ARX side is hence locked to the reference (crystal) of the device feeding audio data to the ATX, and *not* to the crystal of the nRF24Z1 ATX/ ARX devices.

One exception; if the MCLK output option is used in the audio transmitter (meaning clocking an external ADC), the nRF24Z1 ATX crystal is the reference for the audio speed on the entire nRF24Z1 link.

4.4 Control channel

A 2-way, low bit rate, control and signalling channel is running in parallel with the audio stream. This control channel is a part of the QoS overhead, i.e. difference between on the air data rate (4 Mbit/s) and the nominal audio data rate 1.5 Mbit/s. Data channel rate can hence not be traded for higher audio data rate. The functionality of the control channel is illustrated in Figure 11. on page 25.

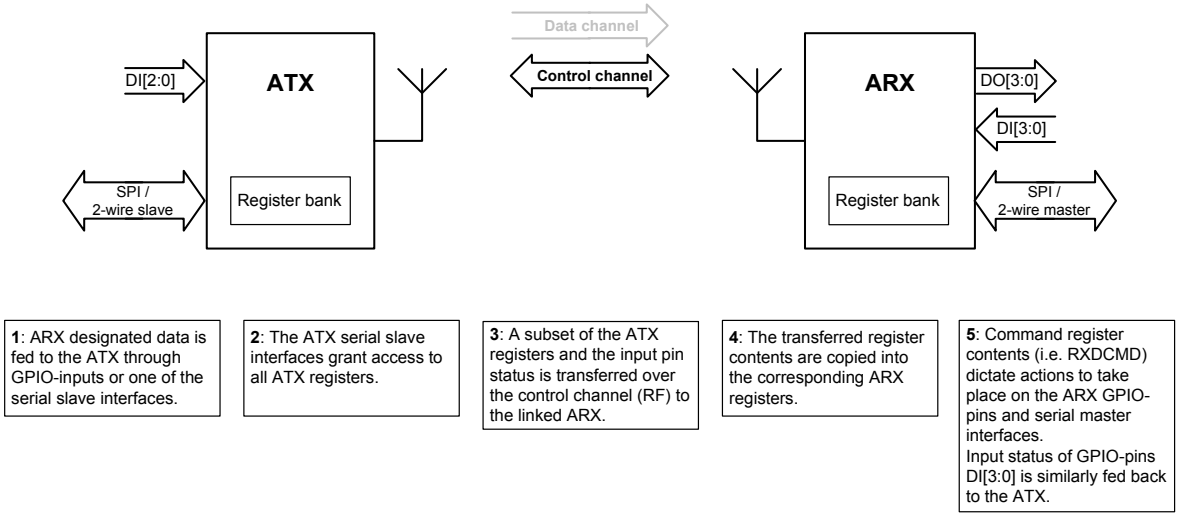

Figure 11. nRF24Z1 control channel transfer principle

Through the control channel the ATX has write access to a majority of registers which are related to ARX configuration. ATX can thereby access ARX GPIO (for LEDs and so on) and the ARX 2-wire and SPI master interface for configuring of DACs, volume control and other peripheral functions.

4.5 Power down mode

In power down mode, the QoS engine is shut down, and only a low frequency oscillator and some timers are active. A timer time-out or an external pin event can be used to exit power down mode. Once power down mode is aborted, the link initialization routine is initiated as described in section 4.2 on page 22.

The sleep and wake timers enable the nRF24Z1 to shut down on a cyclic basis if no transceiver counterpart is detected. The ARX may also be put out of power down mode by toggling a **GPIO**-pin.