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nRF51422

Multiprotocol ANT™/*Bluetooth*® low energy System on Chip

Product Specification v3.1

Key Features

- 2.4 GHz transceiver
  - -90 dBm sensitivity in ANT mode
  - -93 dBm sensitivity in *Bluetooth*® low energy mode
  - 250 kbps, 1 Mbps, 2 Mbps supported data rates
  - TX Power -20 to +4 dBm in 4 dB steps
  - TX Power -30 dBm Whisper mode
  - 13 mA peak RX, 10.5 mA peak TX (0 dBm)
  - 9.7 mA peak RX, 8 mA peak TX (0 dBm) with DC/DC
  - RSSI (1 dB resolution)
- ARM® Cortex™-M0 32 bit processor
  - 275 µA/MHz running from flash memory
  - 150 µA/MHz running from RAM
  - Serial Wire Debug (SWD)
- S200 and S300 series SoftDevice ready
- Memory
  - 256 kB or 128 kB embedded flash program memory
  - 16 kB or 32 kB RAM
- On-air compatibility with nRF24L series
- Flexible Power Management
  - Supply voltage range 1.8 V to 3.6 V
  - 4.2 µs wake-up using 16 MHz RCOSC
  - 0.6 µA at 3 V OFF mode
  - 1.2 µA at 3 V in OFF mode + 1 region RAM retention
  - 2.6 µA at 3 V ON mode, all blocks IDLE
- 8/9/10 bit ADC - 8 configurable channels
- 31 General Purpose I/O Pins
- One 32 bit and two 16 bit timers with counter mode
- SPI Master/Slave
- Low power comparator
- Temperature sensor
- Two-wire Master (I2C compatible)
- UART (CTS/RTS)
- CPU independent Programmable Peripheral Interconnect (PPI)
- Quadrature Decoder (QDEC)
- AES HW encryption
- Real Timer Counter (RTC)
- Package variants
  - QFN48 package, 6 x 6 mm
  - WLCSP package, 3.50 x 3.83 mm
  - WLCSP package, 3.83 x 3.83 mm
  - WLCSP package, 3.50 x 3.33 mm

Applications

- Personal Area Networks
  - Health/fitness sensor and monitor devices
  - Medical devices
  - Key-fobs + wrist watches
- Remote control toys
- Home/industrial automation
- Environmental sensor networks
- Active RFID
- Logistics/goods tracking
- Audience-response systems
- Interactive entertainment devices
  - Remote control
  - Gaming controller

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Datasheet Status

Status	Description
Objective Product Specification (OPS)	This product specification contains target specifications for product development.
Preliminary Product Specification (PPS)	This product specification contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
Product Specification (PS)	This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Revision History

Date	Version	Description
October 2014	3.1	Added documentation for the following versions of the chip: • nRF51422-CDAB AA0 • nRF51422-CDAB Ax0 • nRF51422-QFAC AB0 • nRF51422-QFAC Ax0 • nRF51422-CFAC AA0 • nRF51422-CFAC Ax0 (The x in the build codes can be any number between 0 and 9.) **Added content:** • ***Section 2.2.2 "CDAB WLCSP ball assignment and functions"*** on page 13 • ***Section 9.2 "CDAB WLCSP package"*** on page 67 • ***Section 9.4 "CFAC WLCSP package"*** on page 69 **Updated content:** • Feature list on the front page. • ***Section 2.2.3 "CEAA and CFAC WLCSP ball assignment and functions"*** on page 16 • ***Section 3.2.1 "Code organization"*** on page 21 • ***Section 3.2.2 "RAM organization"*** on page 21 • ***Section 3.3 "Memory Protection Unit (MPU)"*** on page 22 • ***Section 8.2 "Power management"*** on page 44 • ***Section 8.3 "Block resource requirements"*** on page 48 • ***Section 8.12 "Analog to Digital Converter (ADC) specifications"*** on page 60 • ***Section 10.6 "Code ranges and values"*** on page 73 • ***Section 10.7 "Product options"*** on page 75 •

Date	Version	Description
August 2014	3.0	Update to reflect the changes in build code: • nRF51422-QFAA Fx0 • nRF51422-CEAA Cx0 • nRF51422-QFAB Bx0 (The x in the build codes can be any number between 0 and 9.) If you are working with a previous revision of the chip, read version 2.x of the document. **Added content:** • ***Section 8.5.3 "Radio current consumption with DC/DC enabled"*** on page 50 • ***Section 11.1.1 "PCB layout example"*** on page 77 **Updated content:** • Feature list on the front page. • ***Section 2.1 "Block diagram"*** on page 10 • ***Section 3.2.1 "Code organization"*** on page 21 • ***Section 3.2.2 "RAM organization"*** on page 21 • ***Section 3.3 "Memory Protection Unit (MPU)"*** on page 22 • ***Section 3.4 "Power management (POWER)"*** on page 23 • ***Section 3.6 "Clock management (CLOCK)"*** on page 27 • ***Section 3.8 "Debugger support"*** on page 30 • ***Section 4.2 "Timer/counters (TIMER)"*** on page 32 • ***Chapter 5 "Instance table"*** on page 36 • ***Chapter 7 "Operating conditions"*** on page 38 • ***Section 8.1.2 "16 MHz crystal oscillator (16M XOSC)"*** on page 40 • ***Section 8.1.3 "32 MHz crystal oscillator (32M XOSC)"*** on page 41 • ***Section 8.1.4 "16 MHz RC oscillator (16M RCOSC)"*** on page 42 • ***Section 8.1.6 "32.768 kHz RC oscillator (32k RCOSC)"*** on page 43 • ***Section 8.1.7 "32.768 kHz Synthesized oscillator (32k SYNT)"*** on page 43 • ***Section 8.2 "Power management"*** on page 44 • ***Section 8.3 "Block resource requirements"*** on page 48 • ***Section 8.4 "CPU"*** on page 48 • ***Section 8.5.6 "Radio timing parameters"*** on page 54 • ***Section 8.5.7 "Antenna matching network requirements"*** on page 54 • ***Section 8.7 "Universal Asynchronous Receiver/Transmitter (UART) specifications"*** on page 55 • ***Section 8.8 "Serial Peripheral Interface Slave (SPIS) specifications"*** on page 56 • ***Section 8.12 "Analog to Digital Converter (ADC) specifications"*** on page 60 • ***Section 8.13 "Timer (TIMER) specifications"*** on page 61 • ***Section 8.15 "Temperature sensor (TEMP)"*** on page 61 • ***Section 8.22 "Non-Volatile Memory Controller (NVMC) specifications"*** on page 64 • ***Section 8.24 "Low Power Comparator (LPCOMP) specifications"*** on page 65 • ***Section 9.2 "CDAB WLCSP package"*** on page 67 • ***Chapter 11 "Reference circuitry"*** on page 76
February 2014	2.1	Added content about the nRF51422-QFAB chip variant. **Updated content:** • ***Chapter 3.2.1 "Code organization"*** on page 21 • ***Chapter 3.2.2 "RAM organization"*** on page 21 • ***Chapter 3.3 "Memory Protection Unit (MPU)"*** on page 22 • ***Chapter 10.7.1 "nRF ICs"*** on page 75 • ***Chapter 11.3.1.1 "Bill of Materials"*** on page 80 • ***Chapter 11.3.2.1 "Bill of Materials"*** on page 82 • ***Chapter 11.3.3.1 "Bill of Materials"*** on page 84

Date	Version	Description
December 2013	2.0	This version of the document will target the nRF51422 QFAA E0 revision and the nRF51422 CEAA B0 revision of the chip. If you are working with a previous revision of the chip, read version 1.2 or earlier of the document. **Added content:** • ***Section 3.3 "Memory Protection Unit (MPU)"*** on page 22 • ***Section 4.5 "AES CCM Mode Encryption (CCM)"*** on page 33 • ***Section 4.6 "Accelerated Address Resolver (AAR)"*** on page 33 • ***Section 4.16 "Low Power Comparator (LPCOMP)"*** on page 35 • ***Section 8.5.7 "Antenna matching network requirements"*** on page 54 • ***Section 8.8 "Serial Peripheral Interface Slave (SPIS) specifications"*** on page 56 • ***Section 8.18 "AES CCM Mode Encryption (CCM) specifications"*** on page 62 • ***Section 8.19 "Accelerated Address Resolver (AAR) specifications"*** on page 62 • ***Section 8.24 "Low Power Comparator (LPCOMP) specifications"*** on page 65 **Updated content:** • Feature list on the Front page • ***Chapter 1 "Introduction"*** on page 9 • ***Section 1.1 "Required reading"*** on page 9 • ***Section 2.1 "Block diagram"*** on page 10 • ***Section 2.2 "Pin assignments and functions"*** on page 11 • ***Section 3.2 "Memory"*** on page 20 • ***Section 3.5 "Programmable Peripheral Interconnect (PPI)"*** on page 26 • ***Section 3.7 "GPIO"*** on page 30 • ***Chapter 4 "Peripheral blocks"*** on page 31 • ***Section 4.1 "2.4 GHz radio (RADIO)"*** on page 31 • ***Section 4.2 "Timer/counters (TIMER)"*** on page 32 • ***Section 4.3 "Real Time Counter (RTC)"*** on page 32 • ***Section 4.10 "Serial Peripheral Interface (SPI/SPIS)"*** on page 34 • ***Section 4.12 "Universal Asynchronous Receiver/Transmitter (UART)"*** on page 35 • ***Section 4.14 "Analog to Digital Converter (ADC)"*** on page 35 • ***Section 4.15 "GPIO Task Event blocks (GPIOTE)"*** on page 35 • ***Chapter 5 "Instance table"*** on page 36 • ***Chapter 6 "Absolute maximum ratings"*** on page 37 • ***Section 8.1.2 "16 MHz crystal oscillator (16M XOSC)"*** on page 40 • ***Section 8.1.3 "32 MHz crystal oscillator (32M XOSC)"*** on page 41 • ***Section 8.1.5 "32.768 kHz crystal oscillator (32k XOSC)"*** on page 42 • ***Section 8.2 "Power management"*** on page 44 • ***Section 8.3 "Block resource requirements"*** on page 48 • ***Section 8.5.1 "General radio characteristics"*** on page 49 • ***Section 8.5.5 "Receiver specifications"*** on page 52 • ***Section 8.5.6 "Radio timing parameters"*** on page 54 • ***Section 8.7 "Universal Asynchronous Receiver/Transmitter (UART) specifications"*** on page 55 • ***Section 8.9 "Serial Peripheral Interface (SPI) Master specifications"*** on page 57 • ***Section 8.11 "GPIO Tasks and Events (GPIOTE) specifications"*** on page 59 • ***Section 8.13 "Timer (TIMER) specifications"*** on page 61 • ***Section 8.16 "Random Number Generator (RNG) specifications"*** on page 62 • ***Chapter 10 "Ordering information"*** on page 70 • ***Section 11.1 "PCB guidelines"*** on page 76 • ***Section 11.3 "QFAA QFN48 package"*** on page 79 • ***Section 11.7 "CEAA WLCSP package"*** on page 103

Date	Version	Description
April 2013	1.2	Added chip variant nRF51422-CEAA. Updated feature list on front page. **Updated** Section 3.2.1 on page 15, Section 3.2.2 on page 15, Chapter 6 on page 28, Section 10.4 on page 52, and Section 10.5.1 on page 53. **Added** Section 2.2.2 on page 10, Section 7.1 on page 29, Section 9.2 on page 50, and Section 11.3 on page 61. **Removed** PCB layouts in Chapter 11 on page 54.
March 2013	1.1	Added 32 MHz crystal oscillator feature. Moved subsection 'Calculating current when the DC/DC converter is enabled' from chapter 8 to the *nRF51 Series Reference Manual*. **Updated** Section 3.2 on page 12, Section 3.5 on page 16, Section 3.5.1 on page 17, Section 4.2 on page 21, Chapter 5 on page 24, Section 8.1 on page 27, Section 8.1.2 on page 28, Section 8.1.5 on page 30, Section 8.2 on page 32, Section 8.3 on page 34, Section 8.5.3 on page 36, Section 8.8 on page 40, Section 8.9 on page 41, Section 8.10 on page 42, and Section 8.14 on page 43. **Added** Section 3.5.4 on page 19, Section 8.1.3 on page 29, and Section 11.1 on page 50.
December 2012	1.0	Changed from PPS to PS. Updated the feature list on the front page. **Updated** Section 3.5.3 on page 18, Table 10 on page 24, Table 11 on page 25, Table 12 on page 26, Table 14 on page 27, Table 15 on page 28, Table 16 on page 28, Table 17 on page 29, Table 19 on page 30, Table 20 on page 31, Table 22 on page 32, Table 23 on page 32, Table 24 on page 33, Table 25 on page 35, Table 26 on page 36, Table 28 on page 36, Table 29 on page 37, Table 30 on page 37, Table 32 on page 38, Table 33 on page 38, Table 36 on page 39, Section 8.16 on page 40, Table 39 on page 40, Table 40 on page 40, Table 56 on page 47, and the reference design in Chapter 11 on page 48. **Added** Section 3.5.4 on page 19 and Table 18 on page 29.

Table of contents

1 Introduction

The nRF51422 is an ultra-low power 2.4 GHz wireless System on Chip (SoC) integrating the nRF51 series 2.4 GHz transceiver, a 32 bit ARM® Cortex™-M0 CPU, flash memory, and analog and digital peripherals. nRF51422 supports ANT, *Bluetooth*® low energy, and a range of proprietary 2.4 GHz protocols, such as Gazell from Nordic Semiconductor.

A range of fully qualified wireless protocol stacks for the nRF51422 are available as SoftDevices from www.nordicsemi.com.

nRF51422 supports the following SoftDevice series:

- S200 - ANT stacks
- S300 - ANT/*Bluetooth* low energy stack

Note: The S200 and S300 SoftDevices are restricted to run only on nRF51422 devices.

SoftDevices can be installed on the nRF51422 independent of your own application code.

1.1 Required reading

The following documentation is available for download from www.nordicsemi.com:

- *nRF51 Series Reference Manual*
- *nRF51422-PAN (Product Anomaly Notification)*
- *PCN-093 (nRF51422 Product Change Notification)*

1.2 Writing conventions

This product specification follows a set of typographic rules to ensure that the document is consistent and easy to read. The following writing conventions are used:

- Command, event names, and bit state conditions, are written in `Lucida Console`.
- Pin names and pin signal conditions are written in **`Consolas.`**
- File names and User Interface components are written in **bold**.
- Internal cross references are italicized and written in ***semi-bold.***
- Placeholders for parameters are written in italic regular text font. For example, a syntax description of Connect will be written as:
  Connect*(TimeOut, AdvInterval).*
- Fixed parameters are written in regular text font. For example, a syntax description of Connect will be written as:
  Connect(0x00F0, Interval).

2 Product overview

2.1 Block diagram

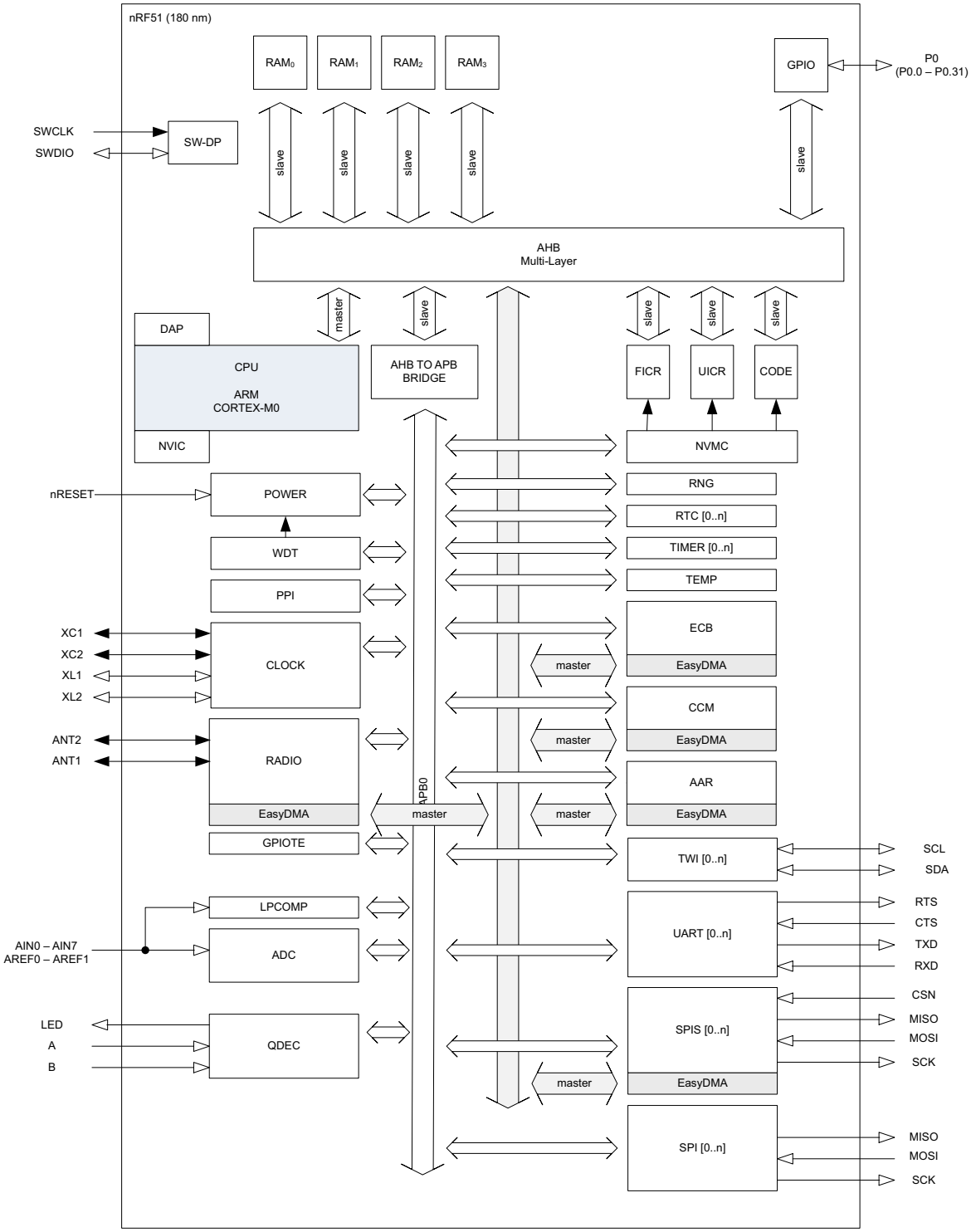

Figure 1 *Block diagram*

2.2 Pin assignments and functions

This section describes the pin assignment and the pin functions.

2.2.1 Pin assignment QFN48

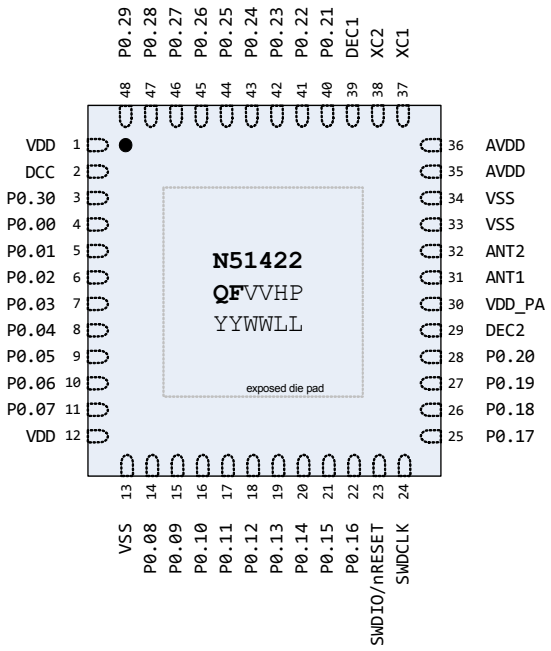

Figure 2 *Pin assignment - QFN48 packet*

Note: VV = Variant code, HP = Build code, YYWWLL = Tracking code.
For more information, see ***Section 10.6 "Code ranges and values"*** on page 73.

2.2.1.1 Pin functions QFN48

Pin	Pin name	Pin function	Description
1	VDD	Power	Power supply.
2	DCC	Power	DC/DC output voltage to external LC filter.
3	P0.30	Digital I/O	General purpose I/O pin.
4	P0.00 AREF0	Digital I/O Analog input	General purpose I/O pin. ADC/LPCOMP reference input 0.
5	P0.01 AIN2	Digital I/O Analog input	General purpose I/O pin. ADC/LPCOMP input 2.
6	P0.02 AIN3	Digital I/O Analog input	General purpose I/O pin. ADC/LPCOMP input 3.
7	P0.03 AIN4	Digital I/O Analog input	General purpose I/O pin. ADC/LPCOMP input 4.
8	P0.04 AIN5	Digital I/O Analog input	General purpose I/O pin. ADC/LPCOMP input 5.
9	P0.05 AIN6	Digital I/O Analog input	General purpose I/O pin. ADC/LPCOMP input 6.
10	P0.06 AIN7 AREF1	Digital I/O Analog input Analog input	General purpose I/O pin. ADC/LPCOMP input 7. ADC/LPCOMP reference input 1.
11	P0.07	Digital I/O	General purpose I/O pin.
12	VDD	Power	Power supply.
13	VSS	Power	Ground (0 V)[1].
14 to 22	P0.08 to P0.16	Digital I/O	General purpose I/O pin.
23	SWDIO/nRESET	Digital I/O	System reset (active low). Also hardware debug and flash programming I/O.
24	SWDCLK	Digital input	Hardware debug and flash programming I/O.
25 to 28	P0.17 to P0.20	Digital I/O	General purpose I/O pin.
29	DEC2	Power	Power supply decoupling.
30	VDD_PA	Power output	Power supply output (+1.6 V) for on-chip RF power amp.
31	ANT1	RF	Differential antenna connection (TX and RX).
32	ANT2	RF	Differential antenna connection (TX and RX).
33, 34	VSS	Power	Ground (0 V).
35, 36	AVDD	Power	Analog power supply (Radio).
37	XC1	Analog input	Connection for 16/32 MHz crystal or external 16 MHz clock reference.
38	XC2	Analog output	Connection for 16/32 MHz crystal.
39	DEC1	Power	Power supply decoupling.

Pin	Pin name	Pin function	Description
40 to 44	P0.21 to P0.25	Digital I/O	General purpose I/O pin.
45	P0.26 AIN0 XL2	Digital I/O Analog input Analog output	General purpose I/O pin. ADC/LPCOMP input 0. Connection for 32.768 kHz crystal.
46	P0.27 AIN1 XL1	Digital I/O Analog input Analog input	General purpose I/O pin. ADC/LPCOMP input 1. Connection for 32.768 kHz crystal or external 32.768 kHz clock reference.
47, 48	P0.28 and P0.29	Digital I/O	General purpose I/O pin.

1. The exposed center pad of the QFN48 package must be connected to ground for proper device operation.

Table 1 *Pin functions QFN48 packet*

2.2.2 CDAB WLCSP ball assignment and functions

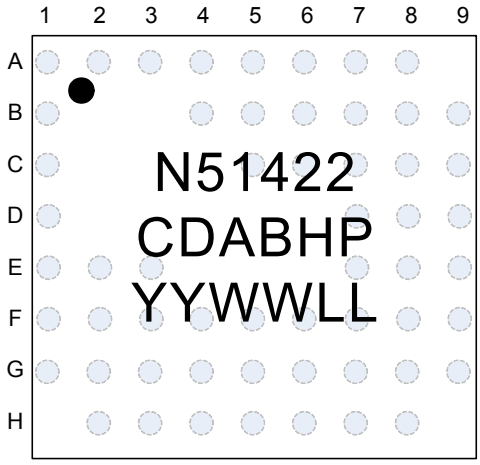

Figure 3 *Ball assignment CDAB packet (top side view)*

2.2.2.1 Ball functions CDAB

Ball	Name	Function	Description
A1	AVDD	Power	Analog power supply (Radio).
A2	XC1	Analog input	Crystal connection for 16/32 MHz crystal oscillator or external 16/32 MHz crystal reference.
A3	XC2	Analog output	Crystal connection for 16/32 MHz crystal.
A4	DEC1	Power	Power supply decoupling.
A5	P0.21	Digital I/O	General purpose I/O.
A6	P0.24	Digital I/O	General purpose I/O.
A7	P0.26 AIN0 XL2	Digital I/O Analog input Analog output	General purpose I/O. ADC input 0. Crystal connection for 32.768 kHz crystal oscillator.
A8	P0.27 AIN1 XL1	Digital I/O Analog input Analog input	General purpose I/O. ADC input 1. Crystal connection for 32.768 kHz crystal oscillator or external 32.768 kHz crystal reference.
B1	VSS	Power	Ground (0 V).
B4	VSS	Power	Ground (0 V).
B5	P0.22	Digital I/O	General purpose I/O.
B6	P0.23	Digital I/O	General purpose I/O.
B7	P0.28	Digital I/O	General purpose I/O.
B8	VDD	Power	Power supply.
B9	DCC	Power	DC/DC output voltage to external LC filter.
C1	ANT2	RF	Differential antenna connection (TX and RX).
C5	P0.25	Digital I/O	General purpose I/O.
C6	N.C.	No Connection	Must be soldered to PCB.
C7	P0.29	Digital I/O	General purpose I/O.
C8	P0.30	Digital I/O	General purpose I/O.
C9	P0.00 AREF0	Digital I/O Analog input	General purpose I/O. ADC Reference voltage.
D1	ANT1	RF	Differential antenna connection (TX and RX).
D7	VSS	Power	Ground (0 V).
D8	P0.31	Digital I/O	General purpose I/O.
D9	P0.02 AIN3	Digital I/O Analog input	General purpose I/O. ADC input 3.
E1	VDD_PA	Power output	Power supply output (+1.6 V) for on-chip RF power amp.
E2	N.C.	No Connection	Must be soldered to PCB.
E3	N.C.	No Connection	Must be soldered to PCB.
E7	P0.01 AIN2	Digital I/O Analog input	General purpose I/O. ADC input 2.
E8	P0.04 AIN5	Digital I/O Analog input	General purpose I/O. ADC input 5.

Ball	Name	Function	Description
E9	P0.03 AIN4	Digital I/O Analog input	General purpose I/O. ADC input 4.
F1	DEC2	Power	Power supply decoupling.
F2	P0.19	Digital I/O	General purpose I/O.
F3	P0.18	Digital I/O	General purpose I/O.
F4	VSS	Power	Ground (0 V).
F5	N.C.	No Connection	Must be soldered to PCB.
F6	VSS	Power	Ground (0 V).
F7	N.C.	No Connection	Must be soldered to PCB.
F8	P0.06 AIN7 AREF1	Digital I/O Analog input Analog input	General purpose I/O. ADC input 7. ADC Reference voltage.
F9	VSS	Power	Ground (0 V).
G1	P0.20	Digital I/O	General purpose I/O.
G2	SWDCLK	Digital input	Hardware debug and flash programming I/O.
G3	P0.17	Digital I/O	General purpose I/O.
G4	P0.14	Digital I/O	General purpose I/O.
G5	P0.13	Digital I/O	General purpose I/O.
G6	P0.10	Digital I/O	General purpose I/O.
G7	P0.07	Digital I/O	General purpose I/O.
G8	VDD	Power	Power supply.
G9	P0.05 AIN6	Digital I/O Analog input	General purpose I/O. ADC input 6.
H2	nRESET SWDIO	Digital I/O	System reset (active low). Hardware debug and flash programming I/O.
H3	P0.16	Digital I/O	General purpose I/O.
H4	P0.15	Digital I/O	General purpose I/O.
H5	P0.12	Digital I/O	General purpose I/O.
H6	P0.11	Digital I/O	General purpose I/O.
H7	P0.09	Digital I/O	General purpose I/O.
H8	P0.08	Digital I/O	General purpose I/O.

Table 2 *Ball functions CDAB packet*

2.2.3 CEAA and CFAC WLCSP ball assignment and functions

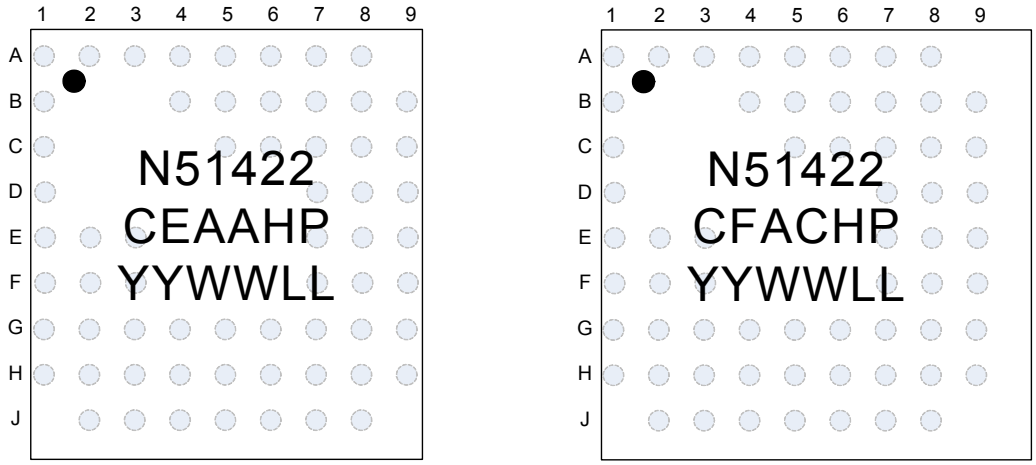

Figure 4 *Ball assignment CEAA and CFAC packet (top side view)*

Note: HP = Buildcode, YYWWLL = Tracking code
Solder balls not visible on the top side. Dot denotes A1 corner.

2.2.3.1 Ball functions CEAA and CFAC

Ball	Name	Function	Description
A1	AVDD	Power	Analog power supply (Radio).
A2	XC1	Analog input	Crystal connection for 16/32 MHz crystal oscillator or external 16/32 MHz crystal reference.
A3	XC2	Analog output	Crystal connection for 16/32 MHz crystal.
A4	DEC1	Power	Power supply decoupling.
A5	P0.21	Digital I/O	General purpose I/O.
A6	P0.24	Digital I/O	General purpose I/O.
A7	P0.26 AIN0 XL2	Digital I/O Analog input Analog output	General purpose I/O. ADC input 0. Crystal connection for 32.768 kHz crystal oscillator.
A8	P0.27 AIN1 XL1	Digital I/O Analog input Analog input	General purpose I/O. ADC input 1. Crystal connection for 32.768 kHz crystal oscillator or external 32.768 kHz crystal reference.
B1	VSS	Power	Ground (0 V).
B4	VSS	Power	Ground (0 V).
B5	P0.22	Digital I/O	General purpose I/O.
B6	P0.23	Digital I/O	General purpose I/O.
B7	P0.28	Digital I/O	General purpose I/O.
B8	VDD	Power	Power supply.
B9	DCC	Power	DC/DC output voltage to external LC filter.
C1	ANT2	RF	Differential antenna connection (TX and RX).
C5	P0.25	Digital I/O	General purpose I/O.
C6	N.C.	No Connection	Must be soldered to PCB.
C7	P0.29	Digital I/O	General purpose I/O.
C8	VSS	Power	Ground (0 V).
C9	P0.00 AREF0	Digital I/O Analog input	General purpose I/O. ADC Reference voltage.
D1	ANT1	RF	Differential antenna connection (TX and RX).
D7	VSS	Power	Ground (0 V).
D8	P0.30	Digital I/O	General purpose I/O.
D9	P0.02 AIN3	Digital I/O Analog input	General purpose I/O. ADC input 3.
E1	VDD_PA	Power output	Power supply output (+1.6 V) for on-chip RF power amp.
E2	N.C.	No Connection	Must be soldered to PCB.
E3	N.C.	No Connection	Must be soldered to PCB.
E7	N.C.	No Connection	Must be soldered to PCB.
E8	P0.31	Digital I/O	General purpose I/O.
E9	P0.01 AIN2	Digital I/O Analog input	General purpose I/O. ADC input 2.

Ball	Name	Function	Description
F1	DEC2	Power	Power supply decoupling.
F2	P0.19	Digital I/O	General purpose I/O.
F3	N.C.	No Connection	Must be soldered to PCB.
F7	N.C.	No Connection	Must be soldered to PCB.
F8	P0.04 AIN5	Digital I/O Analog input	General purpose I/O. ADC input 5.
F9	P0.03 AIN4	Digital I/O Analog input	General purpose I/O. ADC input 4.
G1	P0.20	Digital I/O	General purpose I/O.
G2	P0.17	Digital I/O	General purpose I/O.
G3	N.C.	No Connection	Must be soldered to PCB.
G4	N.C.	No Connection	Must be soldered to PCB.
G5	N.C.	No Connection	Must be soldered to PCB.
G6	VSS	Power	Ground (0 V).
G7	N.C.	No Connection	Must be soldered to PCB.
G8	P0.06 AIN7 AREF1	Digital I/O Analog input Analog input	General purpose I/O. ADC input 7. ADC Reference voltage.
G9	VSS	Power	Ground (0 V).
H1	P0.18	Digital I/O	General purpose I/O.
H2	SWDCLK	Digital input	Hardware debug and flash programming I/O.
H3	VSS	Power	Ground (0 V).
H4	P0.14	Digital I/O	General purpose I/O.
H5	P0.13	Digital I/O	General purpose I/O.
H6	P0.10	Digital I/O	General purpose I/O.
H7	P0.07	Digital I/O	General purpose I/O.
H8	VDD	Power	Power supply.
H9	P0.05 AIN6	Digital I/O Analog input	General purpose I/O. ADC input 6.
J2	SWDIO/ nRESET	Digital I/O	System reset (active low). Also Hardware debug and flash programming I/O.
J3	P0.16	Digital I/O	General purpose I/O.
J4	P0.15	Digital I/O	General purpose I/O.
J5	P0.12	Digital I/O	General purpose I/O.
J6	P0.11	Digital I/O	General purpose I/O.
J7	P0.09	Digital I/O	General purpose I/O.
J8	P0.08	Digital I/O	General purpose I/O.

Table 3 *Ball functions for CEAA and CFAC*

3 System blocks

The chip contains system-level features common to all nRF51 series devices including clock control, power and reset, interrupt system, Programmable Peripheral Interconnect (PPI), watchdog, and GPIO.

System blocks which have a register interface and/or interrupt vector assigned are instantiated in the device address space. The instances of system blocks, their associated ID (for those with interrupt vectors), and base addresses are found in ***Table 18*** on page 36. Detailed functional descriptions, configuration options, and register interfaces can be found in the *nRF51 Series Reference Manual*.

3.1 CPU

The ARM® Cortex™-M0 CPU has a 16 bit instruction set with 32 bit extensions (Thumb-2® technology) that delivers high-density code with a small-memory-footprint. By using a single-cycle 32 bit multiplier, a 3-stage pipeline, and a Nested Vector Interrupt Controller (NVIC), the ARM Cortex-M0 CPU makes program execution simple and highly efficient.

The ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM Cortex-M processor series is implemented and available for M0 CPU. Code is forward compatible with ARM Cortex M3 based devices.

3.2 Memory

All memory and registers are found in the same address space as shown in the Device Memory Map, see ***Figure 5***. Devices in the nRF51 series use flash based memory in the code, FICR, and UICR regions. The RAM region is SRAM.

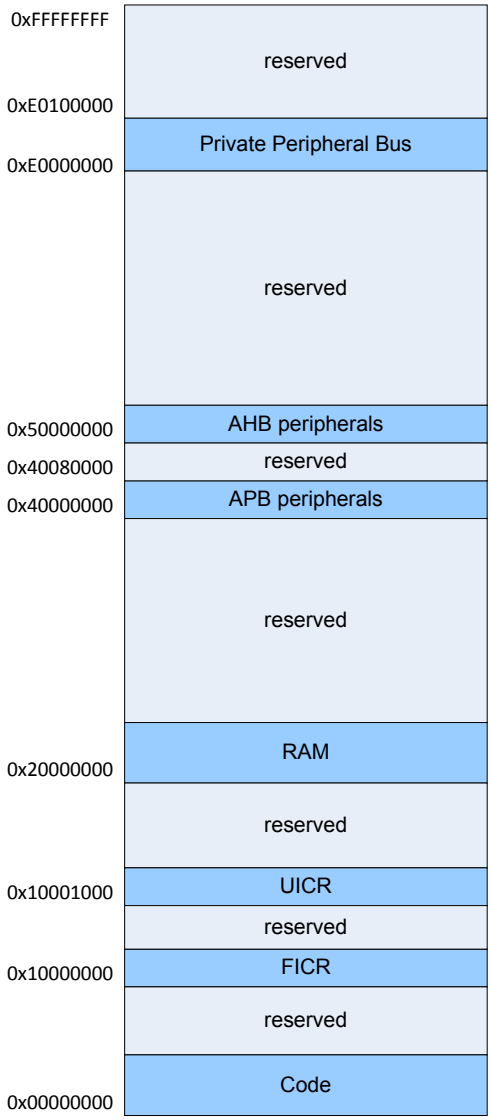

Figure 5 *Memory Map*

The embedded flash memory for program and static data can be programmed using In Application Programming (IAP) routines from RAM through the SWD interface, or in-system from a program executing from code area. The Non-Volatile Memory Controller (NVMC) is used for program/erase operations. Regions of flash memory can be protected from read, write, and erase by the Memory Protection Unit (MPU). A User Information Configuration Register (UICR) contains the lock byte for enabling readback protection to secure the IP, while individual block protection is controlled using registers which can only be cleared on chip reset.

3.2.1 Code organization

Chip variant	Code size	Page size	No of pages
nRF51422-QFAA nRF51422-CEAA	256 kB	1024 byte	256
nRF51422-QFAB nRF51422-CDAB	128 kB	1024 byte	128
nRF51422-QFAC nRF51422-CFAC	256 kB	1024 byte	256

Table 4 *Code organization*

3.2.2 RAM organization

RAM is divided into blocks for separate power management which is controlled by the POWER System Block. Each block is divided into two 4 kByte RAM sections with separate RAM AHB slaves.
Please see the *nRF51 Series Reference Manual* for more information.

Chip variant	RAM size	Block	Size
nRF51422-QFAA nRF51422-CEAA	16 kB	Block0 Block1	8 kB 8 kB
nRF51422-QFAB nRF51422-CDAB	16 kB	Block0 Block1	8 kB 8 kB
nRF51422-QFAC nRF51422-CFAC	32 kB	Block0 Block1 Block2 Block3	8 kB 8 kB 8 kB 8 kB

Table 5 *RAM organization*

How to organize the use of the RAM

For the best performance we recommend the following use of the RAM AHB slaves (Note that the Crypto consists of CCM, ECB, and AAR modules):

- If the Radio and Crypto buffers together are larger in size than one RAM section, the buffers should be separated so the memory used by the Radio is in one RAM section while the memory used by the Crypto is in another RAM section.
- The sections used by CODE should not be combined with sections used by the Radio, Crypto, or SPI.
- The Stack and Heap should be placed at the top section and should not be combined with sections used by the Radio, Crypto, or SPI.

Table 6 and ***Table 7*** shows how memory allocated to different functions can be distributed between RAM sections for parallel access. There is a table for chip variants with 16 kB or 32 kB RAM.

RAM Blocks/Sections		Radio buffers	Crypto buffers	SPIS buffers	CPU Stack/Heap	CODE	Global variables
Block0	RAM0	x	x				x
	RAM1					x	x
Block1	RAM2			x			x
	RAM3				x	x	x

Table 6 *16 kB RAM variants*

RAM Blocks/Sections		Radio buffers	Crypto buffers	SPIS buffers	CPU Stack/Heap	CODE	Global variables
Block0	RAM0	x	(x)				x
	RAM1	(x)	x				x
Block1	RAM2			x			x
	RAM3					x	x
Block2	RAM4					x	x
	RAM5					x	x
Block3	RAM6					x	x
	RAM7				x	x	x

Table 7 *32 kB RAM variants*

3.3 Memory Protection Unit (MPU)

The memory protection unit can be configured to protect all flash memory on the device from read-back, or to protect blocks of flash from over-write or erase.

Chip variant	Flash block size	Number of protectable Flash blocks
nRF51422-QFAA nRF51422-CEAA	4 kB	64
nRF51422-QFAB nRF51422-CDAB	4 kB	32
nRF51422-QFAC nRF51422-CFAC	4 kB	64

Table 8 *MPU flash blocks*

3.4 Power management (POWER)

3.4.1 Power supply

nRF51 supports three different power supply alternatives:

- Internal LDO setup
- DC/DC converter setup
- Low voltage mode setup

See ***Table 20*** on page 38 for the voltage range on the different alternatives. See ***Chapter 11 "Reference circuitry"*** on page 76 for details on the schematic used for the different power supply alternatives.

3.4.1.1 Internal LDO setup

In internal LDO mode the DC/DC converter is bypassed (disabled) and the system power is generated directly from the supply voltage VDD. This mode could be used as the only option or in combination with the DC/DC converter setup. See DC/DC converter section for more details.

3.4.1.2 DC/DC converter setup

The nRF51 DC/DC buck converter transforms battery voltage to lower internal voltage with minimal power loss. The converted voltage is then available for the linear regulator input. The DC/DC converter can be disabled when the supply voltage drops to the lower limit of the voltage range so the LDO can be used for low supply voltages. When enabled, the DC/DC converter operation is automatically suspended between radio events when only the low current regulator is needed internally.

This feature is particularly useful for applications using battery technologies with nominal cell voltages higher than the minimum supply voltage with DC/DC enabled. The reduction in supply voltage level from a high voltage to a low voltage reduces the peak power drain from the battery. Used with a 3 V coin-cell battery, the peak current drawn from the battery is reduced by approximately 25%.

3.4.1.3 Low voltage mode setup

Devices can be used in low voltage mode where a steady 1.8 V supply is available externally.

3.4.2 Power management

The power management system is highly flexible with functional blocks such as the CPU, Radio Transceiver, and peripherals having separate power state control in addition to the global System ON and OFF modes. In System OFF mode, RAM can be retained and the device state can be changed to System ON through Reset, GPIO DETECT signal, or LPCOMP ANADETECT signal. When in System ON mode, all functional blocks will independently be in IDLE or RUN mode depending on needed functionality.

Power management features:

- Supervisor HW to manage
  - Power on reset
  - Brownout reset
  - Power fail comparator
- System ON/OFF modes
- Pin wake-up from System OFF
  - Reset
  - GPIO DETECT signal
  - LPCOMP ANADETECT signal
- Functional block RUN/IDLE modes
- RAM retention in System OFF mode (8 kB blocks)
  - 16 kB version will have 2 blocks
  - 32 kB version will have 4 blocks

3.4.2.1 System OFF mode

In system OFF mode the chip is in the deepest power saving mode. The system's core functionality is powered down and all ongoing tasks are terminated. The only functionality that can be set up to be responsive is the Pin wake-up mechanism.

One or more blocks of RAM can be retained while in System OFF mode.

3.4.2.2 System ON mode

In system ON mode the system is fully operational and the CPU and selected peripherals can be brought into a state where they are functional and more or less responsive depending on the sub-power mode selected.

There are two sub-power modes:

- Low power
- Constant latency

Low Power

In Low Power mode the automatic power management system is optimized to save power. This is done by keeping as much as possible of the system powered down. The cost of this is that you will have varying CPU wakeup latency and PPI task response.

The CPU wakeup latency will be affected by the startup time of the 1V7 regulator. The PPI task response will vary depending on the resources required by the peripheral where the task originated.

The resources that could be involved are:

- 1V7 with the startup time $\mathbf{t_{1V7}}$
- 1V2 with the startup time $\mathbf{t_{1V2}}$
- One of the following clock sources
  - RC16 with the startup time $\mathbf{t_{START,RC16}}$
  - XO16M/XO32M with the startup time the clock management system $\mathbf{t_{XO}}$[1]

Constant Latency

In Constant Latency mode the system is optimized towards keeping the CPU latency and the PPI task response constant and at a minimum. This is secured by forcing a set of base resources on while in sleep mode. The cost is that the system will have higher power consumption.

The following resources are kept active while in sleep mode:

- 1V7 regulator with the standby current of I_{1V7}
- 1V2 regulator. Here the current consumption is specified in combination with the clock source
- One of the following clock sources:
  - RC16 with the standby current of $I_{1V2RC16}$
  - XO16M with the standby current of $I_{1V2XO16}$
  - XO32M with the standby current of $I_{1V2XO32}$

1. For the clock source XO16M and XO32M we assume that the crystal is already running (standby). This will give an increase of the power consumption in sleep mode given by $\mathbf{I_{STBY,X16M}}$ / $\mathbf{I_{STBY,X32M}}$.