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nRF51824

Multiprotocol *Bluetooth*® low energy/2.4 GHz RF System on Chip

Product Specification v1.0

Key Features

- Automotive AEC-Q100 Grade 2 compliance (-40 to +105°C)
- 2.4 GHz transceiver
  - -93 dBm sensitivity in *Bluetooth*® low energy mode
  - 250 kbps, 1 Mbps BLE, 2 Mbps supported data rates
  - TX Power -20 to +4 dBm in 4 dB steps
  - TX Power -30 dBm Whisper mode
  - 13 mA peak RX, 10.5 mA peak TX (0 dBm)
  - 9.7 mA peak RX, 8 mA peak TX (0 dBm) with DC/DC
  - RSSI (1 dB resolution)
- ARM® Cortex™-M0 32 bit processor
  - 275 µA/MHz running from flash memory
  - 150 µA/MHz running from RAM
  - Serial Wire Debug (SWD)
- S100 series SoftDevice ready
- Memory
  - 256 kB embedded flash program memory
  - 16 kB RAM
- On-air compatibility with nRF24L series for 250 kbps and 2 Mbps
- Flexible Power Management
  - Supply voltage range 1.9 V to 3.6 V
  - 4.2 µs wake-up using 16 MHz RCOSC
  - 0.6 µA at 3 V OFF mode
  - 1.2 µA at 3 V in OFF mode + 1 region RAM retention
  - 2.6 µA at 3 V ON mode, all blocks IDLE
- 8/9/10 bit ADC - 8 configurable channels
- 31 General Purpose I/O Pins
- One 32 bit and two 16 bit timers with counter mode
- SPI Master/Slave
- Low power comparator
- Temperature sensor
- Two-wire Master (I2C compatible)
- UART (CTS/RTS)
- CPU independent Programmable Peripheral Interconnect (PPI)
- Quadrature Decoder (QDEC)
- AES HW encryption
- Real Timer Counter (RTC)
- Package: QFN48 6 x 6 mm

Applications

- *Bluetooth* Smart and proprietary 2.4 GHz systems
- Remote keyless entry
- Infotainment and media
- Tire pressure monitoring
- Cable replacement
- Diagnostics
- Sensor nodes
- Wireless charging

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Datasheet Status

Status	Description
Objective Product Specification (OPS)	This product specification contains target specifications for product development.
Preliminary Product Specification (PPS)	This product specification contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
Product Specification (PS)	This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Revision History

Date	Version	Description
September 2016	1.0	Upgraded to Product Specification (PS).
August 2016	0.9	Added extended temperature range (+105°C instead of +85°C) for Automotive AEC-Q100 Grade 2 compliance.
November 2015	0.7	First release.

Table of contents

1 Introduction

The nRF51824 chip is an ultra-low power 2.4 GHz wireless System on Chip (SoC) integrating the nRF51 Series 2.4 GHz transceiver, a 32 bit ARM® Cortex™-M0 CPU, flash memory, and analog and digital peripherals. nRF51824 can support *Bluetooth*® low energy and a range of proprietary 2.4 GHz protocols, such as Gazell from Nordic Semiconductor.

The nRF51824 chip is fully qualified in accordance to AEC-Q100 Grade 2 specifications.

Fully qualified *Bluetooth* low energy stacks for nRF51824 are implemented in the S1x0 series of SoftDevices. The S1x0 series of SoftDevices are available for free and can be downloaded and installed on nRF51824 independent of your own application code.

1.1 Required reading

The following documentation is available for download from the Infocenter:

- *nRF51 Series Reference Manual*
- *nRF51824-PAN (Product Anomaly Notification)*

1.2 Writing conventions

This product specification follows a set of typographic rules to ensure that the document is consistent and easy to read. The following writing conventions are used:

- Command, event names, and bit state conditions, are written in `Lucida Console`.
- Pin names and pin signal conditions are written in **`Consolas.`**
- File names and User Interface components are written in **bold**.
- Internal cross references are italicized and written in ***semi-bold.***
- Placeholders for parameters are written in italic regular text font. For example, a syntax description of Connect will be written as:
  Connect*(TimeOut, AdvInterval)*.
- Fixed parameters are written in regular text font. For example, a syntax description of Connect will be written as:
  Connect(0x00F0, Interval).

2 Product overview

2.1 Block diagram

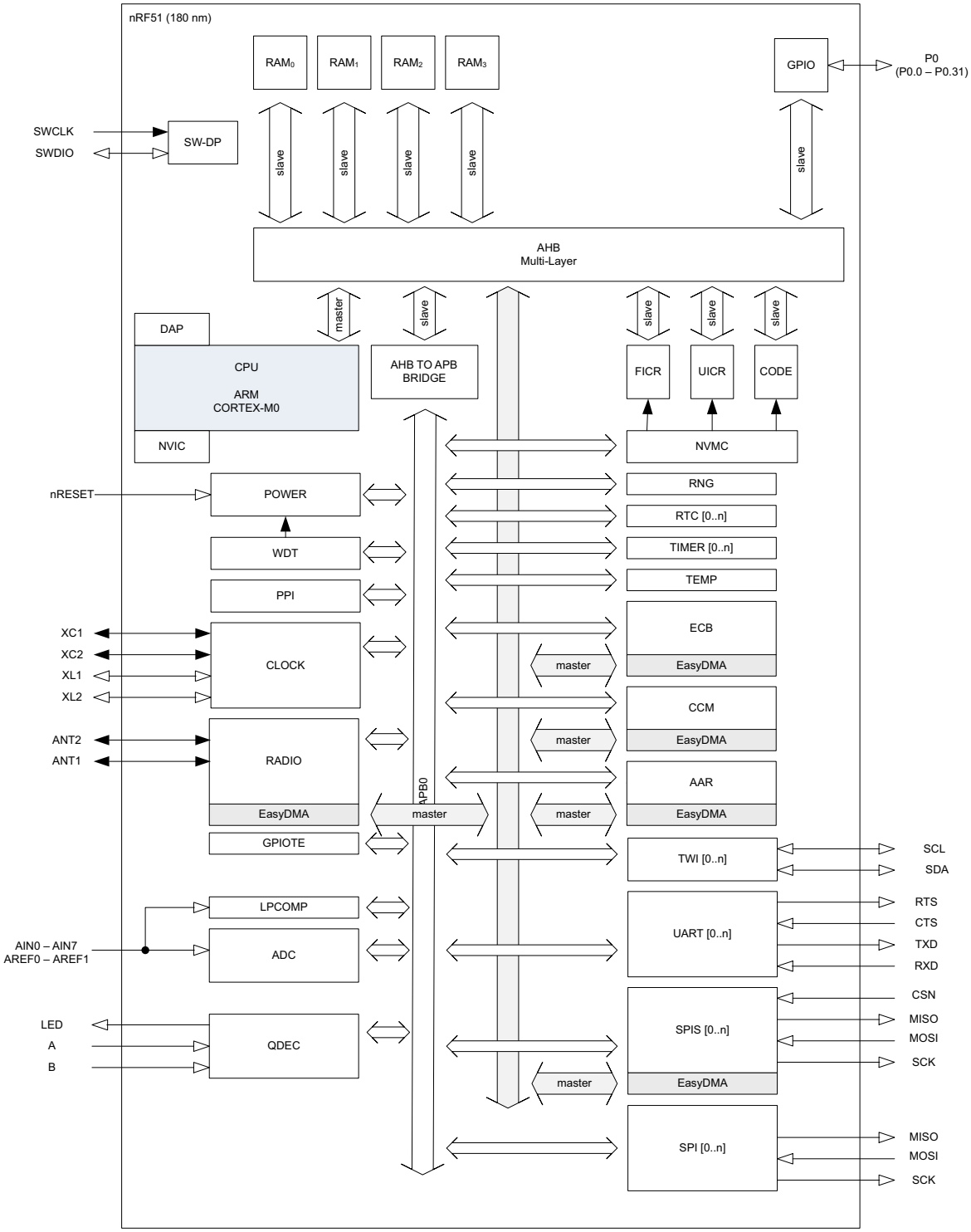

Figure 1 *Block diagram*

2.2 Pin assignments and functions

This section describes the pin assignment and the pin functions.

2.2.1 Pin assignment QFN48

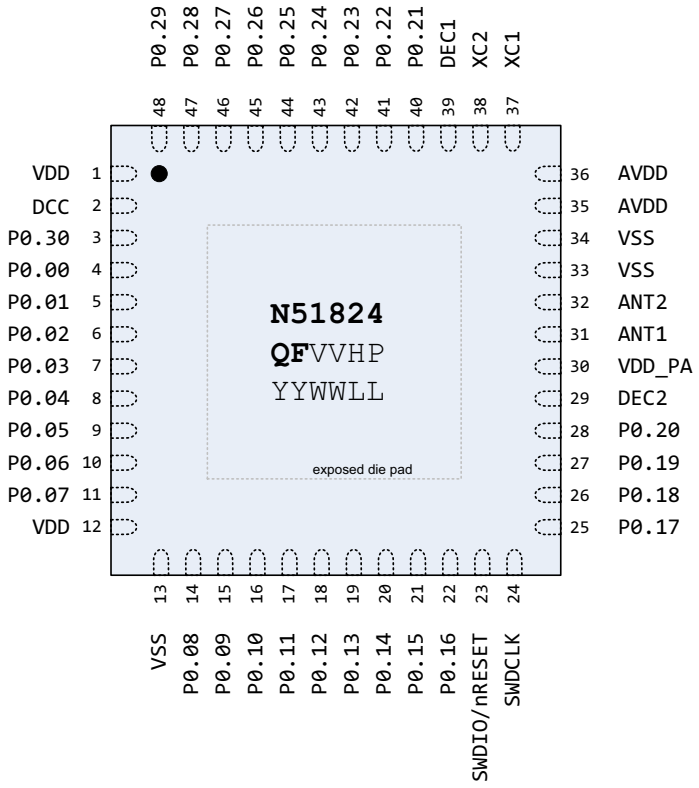

Figure 2 *Pin assignment - QFN48 packet*

Note: VV = Variant code, HP = Build code, YYWWLL = Tracking code.
For more information, see ***Section 10.6 "Code ranges and values"*** on page 61.

2.2.1.1 Pin functions QFN48

Pin	Pin name	Pin function	Description
1	VDD	Power	Power supply.
2	DCC	Power	DC/DC output voltage to external LC filter.
3	P0.30	Digital I/O	General purpose I/O pin.
4	P0.00 AREF0	Digital I/O Analog input	General purpose I/O pin. ADC/LPCOMP reference input 0.
5	P0.01 AIN2	Digital I/O Analog input	General purpose I/O pin. ADC/LPCOMP input 2.
6	P0.02 AIN3	Digital I/O Analog input	General purpose I/O pin. ADC/LPCOMP input 3.
7	P0.03 AIN4	Digital I/O Analog input	General purpose I/O pin. ADC/LPCOMP input 4.
8	P0.04 AIN5	Digital I/O Analog input	General purpose I/O pin. ADC/LPCOMP input 5.
9	P0.05 AIN6	Digital I/O Analog input	General purpose I/O pin. ADC/LPCOMP input 6.
10	P0.06 AIN7 AREF1	Digital I/O Analog input Analog input	General purpose I/O pin. ADC/LPCOMP input 7. ADC/LPCOMP reference input 1.
11	P0.07	Digital I/O	General purpose I/O pin.
12	VDD	Power	Power supply.
13	VSS	Power	Ground (0 V)[1].
14 to 22	P0.08 to P0.16	Digital I/O	General purpose I/O pin.
23	SWDIO/nRESET	Digital I/O	System reset (active low). Hardware debug and flash programming I/O.
24	SWDCLK	Digital input	Hardware debug and flash programming I/O.
25 to 28	P0.17 to P0.20	Digital I/O	General purpose I/O pin.
29	DEC2	Power	Power supply decoupling.
30	VDD_PA	Power output	Power supply output (+1.6 V) for on-chip RF power amp.
31	ANT1	RF	Differential antenna connection (TX and RX).
32	ANT2	RF	Differential antenna connection (TX and RX).
33, 34	VSS	Power	Ground (0 V).
35, 36	AVDD	Power	Analog power supply (Radio).
37	XC1	Analog input	Connection for 16/32 MHz crystal or external 16 MHz clock reference.
38	XC2	Analog output	Connection for 16/32 MHz crystal.
39	DEC1	Power	Power supply decoupling.

Pin	Pin name	Pin function	Description
40 to 44	P0.21 to P0.25	Digital I/O	General purpose I/O pin.
45	P0.26 AIN0 XL2	Digital I/O Analog input Analog output	General purpose I/O pin. ADC/LPCOMP input 0. Connection for 32.768 kHz crystal.
46	P0.27 AIN1 XL1	Digital I/O Analog input Analog input	General purpose I/O pin. ADC/LPCOMP input 1. Connection for 32.768 kHz crystal or external 32.768 kHz clock reference.
47, 48	P0.28 and P0.29	Digital I/O	General purpose I/O pin.

1. The exposed center pad of the QFN48 package must be connected to ground for proper device operation.

Table 1 *Pin functions QFN48 packet*

3 System blocks

The chip contains system-level features common to all nRF51 Series devices including clock control, power and reset, interrupt system, Programmable Peripheral Interconnect (PPI), watchdog, and GPIO.

System blocks which have a register interface and/or interrupt vector assigned are instantiated in the device address space. The instances of system blocks, their associated ID (for those with interrupt vectors), and base addresses are found in ***Table 15*** on page 28. Detailed functional descriptions, configuration options, and register interfaces can be found in the *nRF51 Series Reference Manual*.

3.1 CPU

The ARM® Cortex™-M0 CPU has a 16 bit instruction set with 32 bit extensions (Thumb-2® technology) that delivers high-density code with a small-memory-footprint. By using a single-cycle 32 bit multiplier, a 3-stage pipeline, and a Nested Vector Interrupt Controller (NVIC), the ARM Cortex-M0 CPU makes program execution simple and highly efficient.

The ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM Cortex-M processor series is implemented and available for M0 CPU. Code is forward compatible with ARM Cortex M3 based devices.

3.2 Memory

All memory and registers are found in the same address space as shown in the Device Memory Map, see ***Figure 3***. Devices in the nRF51 Series use flash based memory in the code, FICR, and UICR regions. The RAM region is SRAM.

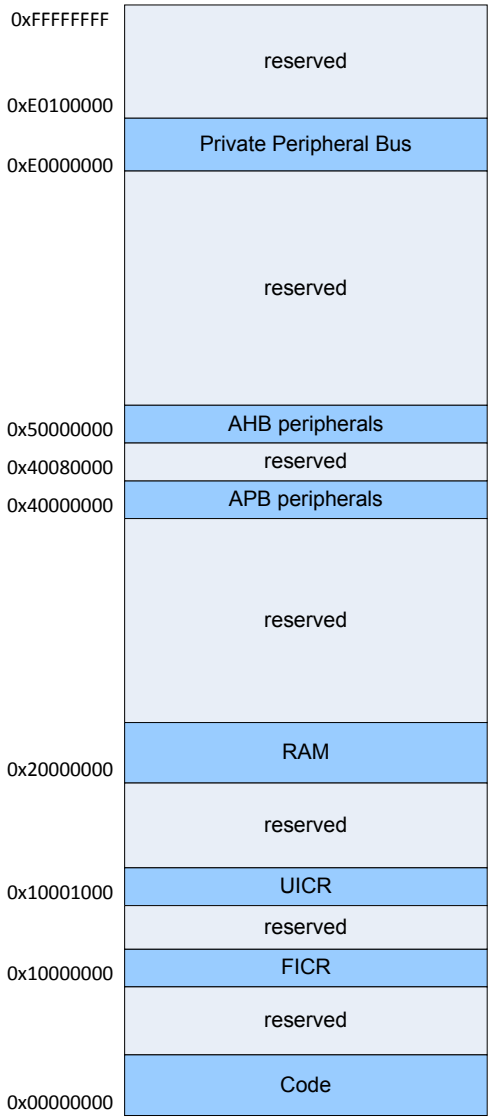

Figure 3 *Memory Map*

The embedded flash memory for program and static data can be programmed using In Application Programming (IAP) routines from RAM through the SWD interface, or in-system from a program executing from code area. The Non-Volatile Memory Controller (NVMC) is used for program/erase operations. Regions of flash memory can be protected from read, write, and erase by the Memory Protection Unit (MPU). A User Information Configuration Register (UICR) contains the lock byte for enabling readback protection to secure the IP, while individual block protection is controlled using registers which can only be cleared on chip reset.

3.2.1 Code organization

Chip variant	Code size	Page size	No of pages
nRF51824-QFAA	256 kB	1024 byte	256

Table 2 *Code organization*

3.2.2 RAM organization

RAM is divided into blocks for separate power management which is controlled by the POWER System Block. Each block is divided into two 4 kByte RAM sections with separate RAM AHB slaves.
Please see the *nRF51 Series Reference Manual* for more information.

Chip variant	RAM size	Block	Size
nRF51824-QFAA	16 kB	Block0 Block1	8 kB 8 kB

Table 3 *RAM organization*

How to organize the use of the RAM

For the best performance we recommend the following use of the RAM AHB slaves (Note that the Crypto consists of CCM, ECB, and AAR modules):

- If the Radio and Crypto buffers together are larger in size than one RAM section, the buffers should be separated so the memory used by the Radio is in one RAM section while the memory used by the Crypto is in another RAM section.
- The sections used by CODE should not be combined with sections used by the Radio, Crypto, or SPI.
- The Stack and Heap should be placed at the top section and should not be combined with sections used by the Radio, Crypto, or SPI.

Table 4 shows how memory allocated to different functions can be distributed between RAM sections for parallel access.

RAM Blocks/Sections		Radio buffers	Crypto buffers	SPIS buffers	CPU Stack/Heap	CODE	Global variables
Block0	RAM0	x	x				x
	RAM1					x	x
Block1	RAM2			x			x
	RAM3				x	x	x

Table 4 *RAM parallel access*

3.3 Memory Protection Unit (MPU)

The memory protection unit can be configured to protect all flash memory on the device from readback, or to protect blocks of flash from over-write or erase.

Chip variant	Flash block size	Number of protectable Flash blocks
nRF51824-QFAA	4 kB	64

Table 5 *MPU flash blocks*

3.4 Power management (POWER)

3.4.1 Power supply

nRF51824 supports two different power supply alternatives:

- Internal LDO setup
- DC/DC converter setup

See ***Table 17*** on page 30 for the voltage range on the different alternatives. See ***Chapter 11 "Reference circuitry"*** on page 64 for details on the schematic used for the different power supply alternatives.

3.4.1.1 Internal LDO setup

In internal LDO mode the DC/DC converter is bypassed (disabled) and the system power is generated directly from the supply voltage VDD. This mode could be used as the only option or in combination with the DC/DC converter setup. See ***Section 3.4.1.2 "DC/DC converter setup"*** for more details.

3.4.1.2 DC/DC converter setup

The nRF51 DC/DC buck converter transforms battery voltage to lower internal voltage with minimal power loss. The converted voltage is then available for the linear regulator input. The DC/DC converter can be disabled when the supply voltage drops to the lower limit of the voltage range so the LDO can be used for low supply voltages. When enabled, the DC/DC converter operation is automatically suspended between radio events when only the low current regulator is needed internally.

This feature is particularly useful for applications using battery technologies with nominal cell voltages higher than the minimum supply voltage with DC/DC enabled. The reduction in supply voltage level from a high voltage to a low voltage reduces the peak power drain from the battery. Used with a 3 V coin-cell battery, the peak current drawn from the battery is reduced by approximately 25%.

3.4.2 Power management

The power management system is highly flexible with functional blocks such as the CPU, Radio Transceiver, and peripherals having separate power state control in addition to the global System ON and OFF modes. In System OFF mode, RAM can be retained and the device state can be changed to System ON through Reset, GPIO DETECT signal, or LPCOMP ANADETECT signal. When in System ON mode, all functional blocks will independently be in IDLE or RUN mode depending on needed functionality.

Power management features:

- Supervisor HW to manage
  - Power on reset
  - Brownout reset
  - Power fail comparator
- System ON/OFF modes
- Pin wake-up from System OFF
  - Reset
  - GPIO DETECT signal
  - LPCOMP ANADETECT signal
- Functional block RUN/IDLE modes
- RAM retention in System OFF mode (8 kB blocks)

3.4.2.1 System OFF mode

In system OFF mode the chip is in the deepest power saving mode. The system's core functionality is powered down and all ongoing tasks are terminated. The only functionality that can be set up to be responsive is the Pin wake-up mechanism.

One or more blocks of RAM can be retained while in System OFF mode.

3.4.2.2 System ON mode

In system ON mode the system is fully operational and the CPU and selected peripherals can be brought into a state where they are functional and more or less responsive depending on the sub-power mode selected.

There are two sub-power modes:

- Low power
- Constant latency

Low Power

In Low Power mode the automatic power management system is optimized to save power. This is done by keeping as much as possible of the system powered down. The cost of this is that you will have varying CPU wakeup latency and PPI task response.

The CPU wakeup latency will be affected by the startup time of the 1V7 regulator. The PPI task response will vary depending on the resources required by the peripheral where the task originated.

The resources that could be involved are:

- 1V7 with the startup time $\mathbf{t_{1V7}}$
- 1V2 with the startup time $\mathbf{t_{1V2}}$
- One of the following clock sources
  - RC16 with the startup time $\mathbf{t_{START,RC16}}$
  - XO16M/XO32M with the startup time the clock management system $\mathbf{t_{XO}}$[1]

Constant Latency

In Constant Latency mode the system is optimized for keeping the CPU latency and the PPI task response constant and at a minimum. This is secured by forcing a set of base resources on while in sleep mode. The cost is that the system will have higher power consumption.

The following resources are kept active while in sleep mode:

- 1V7 regulator with the standby current of I_{1V7}
- 1V2 regulator. Here the current consumption is specified in combination with the clock source.
- One of the following clock sources:
  - RC16 with the standby current of $I_{1V2RC16}$
  - XO16M with the standby current of $I_{1V2XO16}$
  - XO32M with the standby current of $I_{1V2XO32}$

1. For the clock source XO16M and XO32M we assume that the crystal is already running (standby). This will give an increase of the power consumption in sleep mode given by $\mathbf{I_{STBY,X16M}}$ / $\mathbf{I_{STBY,X32M}}$.

3.5 Programmable Peripheral Interconnect (PPI)

The Programmable Peripheral Interconnect (PPI) enables peripherals to interact autonomously with each other using tasks and events independent of the CPU. The PPI allows precise synchronization between peripherals when real-time application constraints exist and eliminates the need for CPU activity to implement behavior which can be predefined using PPI.

Instance	Channel	Number of channels	Number of groups
PPI	0 - 15	16	4

Table 6 *PPI properties*

The PPI system has in addition to the fully programmable peripheral interconnections, a set of channels where the event (EEP) and task (TEP) endpoints are set in hardware. These fixed channels can be individually enabled, disabled, or added to PPI channel groups in the same way as ordinary PPI channels. See the *nRF51 Series Reference Manual* for more information.

Instance	Channel	Number of channels	Number of groups
PPI	20 - 31	12	4

Table 7 *Pre-programmed PPI channels*

3.6 Clock management (CLOCK)

The advanced clock management system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to modules based upon a module's individual requirements. This prevents large clock trees from being active and drawing power when system modules needing this clock reference are not active.

If an application enables a module that needs a clock reference without the corresponding oscillator running, the clock management system will automatically enable the RC oscillator option and provide the clock. When the module goes back to idle, the clock management will automatically set the oscillator to idle. To avoid delays involved in starting a given oscillator, or if a specific oscillator is required, the application can override the automatic oscillator management so it keeps oscillators active when no system modules require the clock reference.

Clocks are only available in System ON mode and can be generated by the sources listed in ***Table 8***.

Clock	Source	Frequency options
High Frequency Clock (HFCLK)[1]	External Crystal (XOSC)	16/32 MHz[2]
	External clock reference[3]	16 MHz
	Internal RC Oscillator (RCOSC)	16 MHz
Low Frequency Clock (LFCLK)	External Crystal (XOSC)	32.768 kHz
	External clock reference[3]	32.768 kHz
	Synthesized from HFCLK	32.768 kHz
	Internal RC Oscillator (RCOSC)	32.768 kHz

1. External Crystal must be used for Radio operation.
2. The HFCLK will be 16 MHz for both the 16 and 32 MHz crystal option.
3. See the *nRF51 Series Reference Manual* for more details on external clock reference.

Table 8 *Clock properties*

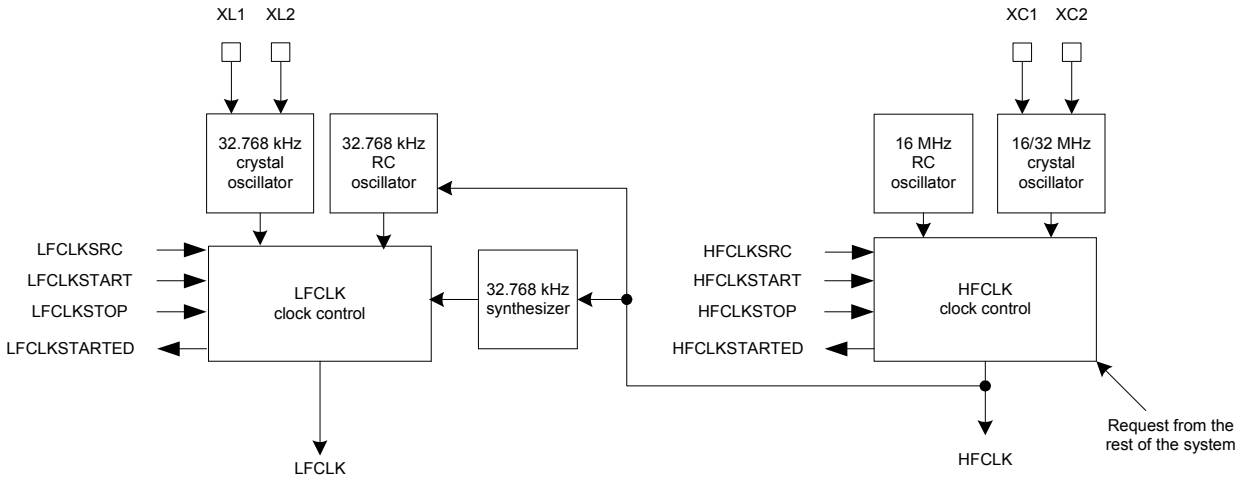

Figure 4 *Clock management*

3.6.1 16/32 MHz crystal oscillator

The crystal oscillator can be controlled either by a 16 MHz or a 32 MHz external crystal. However, the system clock is always 16 MHz, see the *nRF51 Series Reference Manual* for more details. The crystal oscillator is designed for use with an AT-cut quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet. ***Figure 5*** shows how the crystal is connected to the 16/32 MHz crystal oscillator.

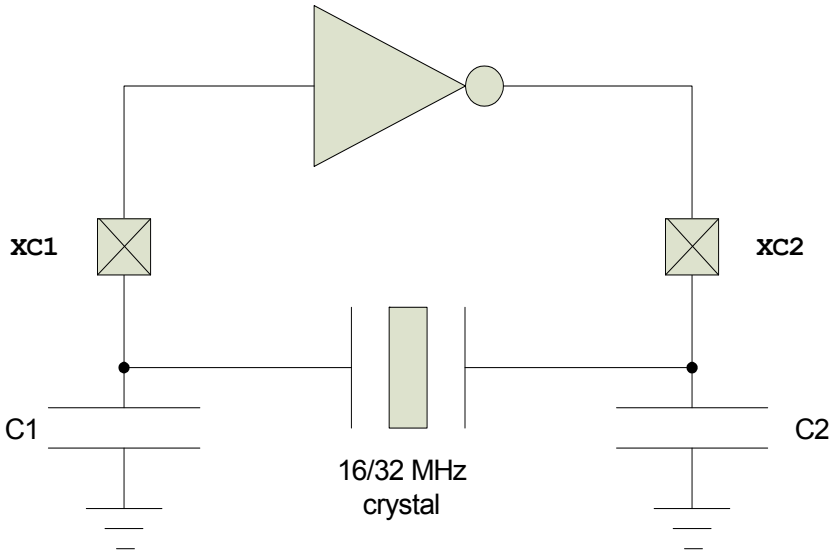

Figure 5 *Circuit diagram of the 16/32 MHz crystal oscillator*

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C\_pcb1 + C\_pin$$

$$C2' = C2 + C\_pcb2 + C\_pin$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. C_pcb1 and C_pcb2 are stray capacitances on the PCB. C_pin is the pin input capacitance on the XC1 and XC2 pins, see ***Table 18*** on page 32 (16 MHz) and ***Table 19*** on page 33 (32 MHz). The load capacitors C1 and C2 should have the same value. See ***Chapter 11 "Reference circuitry"*** on page 64 for the capacitance value used for C_pcb1 and C_pcb2 in reference circuitry.

For reliable operation, the crystal load capacitance, shunt capacitance, equivalent series resistance ($R_{S,X16M}$/$R_{S,X32M}$), and drive level must comply with the specifications in ***Table 18*** on page 32 (16 MHz) and ***Table 19*** on page 33 (32 MHz). It is recommended to use a crystal with lower than maximum $R_{S,X16M}$/$R_{S,X32M}$ if the load capacitance and/or shunt capacitance is high. This will give faster startup and lower current consumption. A low load capacitance will reduce both startup time and current consumption.

3.6.2 32.768 kHz crystal oscillator

The 32.768 kHz crystal oscillator is designed for use with a quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet. ***Figure 6*** shows how the crystal is connected to the 32.768 kHz crystal oscillator.

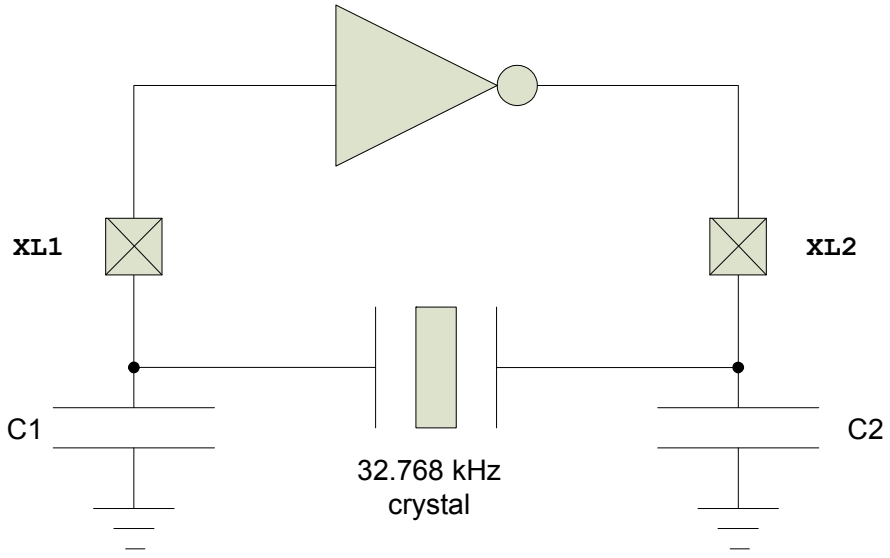

Figure 6 *Circuit diagram of the 32.768 kHz crystal oscillator*

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C\_pcb1 + C\_pin$$

$$C2' = C2 + C\_pcb2 + C\_pin$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. C_pcb1 and C_pcb2 are stray capacitances on the PCB. C_pin is the pin input capacitance on the XC1 and XC2 pins, see ***Section 8.1.5 "32.768 kHz crystal oscillator (32k XOSC)"*** on page 34. The load capacitors C1 and C2 should have the same value. See ***Chapter 11 "Reference circuitry"*** on page 64 for the capacitance value used for C_pcb1 and C_pcb2 in reference circuitry.

3.6.3 32.768 kHz RC oscillator

The 32.768 kHz RC low frequency oscillator may be used as an alternative to the 32.768 kHz crystal oscillator. It has a frequency accuracy of less than ± 250 ppm in a stable temperature environment or when calibration is periodically performed in changing temperature environments. The 32.768 kHz RC oscillator does not require external components.

3.6.4 Synthesized 32.768 kHz clock

The low frequency clock can be synthesized from the high frequency clock. This saves the cost of a crystal but increases average power consumption as the high frequency clock source will have to be active.

3.7 GPIO

The general purpose I/O is organized as one port with up to 32 I/Os (dependent on package) enabling access and control of up to 32 pins through one port. Each GPIO can be accessed individually with the following user configurable features:

- Input/output direction
- Output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on all pins
- All pins can be used by the PPI task/event system. The maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels.
- All pins can be individually configured to carry serial interface or quadrature demodulator signals.

3.8 Debugger support

The two pin Serial Wire Debug (SWD) interface provided as a part of the Debug Access Port (DAP) offers a flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints and single stepping are part of this support.

4 Peripheral blocks

Peripheral blocks which have a register interface and/or interrupt vector assigned are instantiated, one or more times, in the device address space. The instances, associated ID (for those with interrupt vectors), and base address of features are found in ***Table 15*** on page 28**.** Detailed functional descriptions, configuration options, and register interfaces can be found in the *nRF51 Series Reference Manual*.

4.1 2.4 GHz radio (RADIO)

The nRF51824 2.4 GHz RF transceiver is designed and optimized to operate in the worldwide ISM frequency band at 2.400 to 2.4835 GHz. Radio modulation modes and configurable packet structure enable interoperability with *Bluetooth*® low energy (BLE), ANT™, Enhanced ShockBurst™, and other 2.4 GHz protocol implementations.

The transceiver receives and transmits data directly to and from system memory for flexible and efficient packet data management. The nRF51824 transceiver has the following features:

- General modulation features
  - GFSK modulation
  - Data whitening
  - On-air data rates
    - 250 kbps
    - 1 Mbps BLE
    - 2 Mbps
- Transmitter with programmable output power of +4 dBm to -20 dBm, in 4 dB steps
- Transmitter whisper mode -30 dBm
- RSSI function (1 dB resolution)
- Receiver with integrated channel filters achieving maximum sensitivity
  - -96 dBm at 250 kbps
  - -93 dBm at 1 Mbps BLE
  - -85 dBm at 2 Mbps
- RF Synthesizer
  - 1 MHz frequency programming resolution
  - 1 MHz non-overlapping channel spacing at 250 kbps
  - 2 MHz non-overlapping channel spacing at 2 Mbps
  - Works with low-cost ± 60 ppm 16 MHz crystal oscillators
- Baseband controller
  - EasyDMA RX and TX packet transfer directly to and from RAM
  - Dynamic payload length
  - On-the-fly packet assembly/disassembly and AES CCM payload encryption
  - 8 bit, 16 bit, and 24 bit CRC check (programmable polynomial and initial value)

Note: EasyDMA is an integrated DMA implementation requiring no configuration to take advantage of flexible data management and avoids copying operations to and from RAM.

4.2 Timer/counters (TIMER)

The timer/counter runs on the high-frequency clock source (HFCLK) and includes a 4 bit ($1/2^X$) prescaler that can divide the HFCLK.

The TIMER will start requesting the 1 MHz mode of the HFCLK for values of the prescaler that gives f_{TIMER} less or equal to 1 MHz. If the timer module is the only one requesting the HFCLK, the system will automatically switch to using the 1 MHz mode resulting in a decrease in the current consumption. See the parameters $I_{1v2XO16,1M}$, $I_{1v2XO32,1M}$, $I_{1v2RC16,1M}$ in ***Table 28*** on page 39 and $I_{TIMER0/1/2,1M}$ in ***Table 48*** on page 52.

The task/event and interrupt features make it possible to use the PPI system for timing and counting tasks between any system peripheral including any GPIO of the device. The PPI system also enables the TIMER task/event features to generate periodic output and PWM signals to any GPIO. The number of input/outputs used at the same time is limited by the number of GPIOTE channels.

Instance	Bit-width	Capture/Compare registers
TIMER0	8/16/24/32	4
TIMER1	8/16	4
TIMER2	8/16	4

Table 9 *Timer/counter properties*

4.3 Real Time Counter (RTC)

The Real Time Counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK). The RTC features a 24 bit COUNTER, 12 bit (1/X) prescaler, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

Instance	Capture/Compare registers
RTC0	3
RTC1	4

Table 10 *RTC properties*

4.4 AES Electronic Codebook Mode Encryption (ECB)

The ECB encryption block supports 128 bit AES block encryption. It can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption. ECB encryption uses EasyDMA to access system RAM for in-place operations on cleartext and ciphertext during encryption.

4.5 AES CCM Mode Encryption (CCM)

Cipher Block Chaining - Message Authentication Code (CCM) Mode is an authenticated encryption algorithm designed to provide both authentication and confidentiality during data transfer. CCM combines counter mode encryption and CBC-MAC authentication.

Note: The CCM terminology "Message Authentication Code (MAC)" is called the "Message Integrity Check (MIC)" in *Bluetooth* terminology and this document and the *nRF51 Series Reference Manual* are consistent with *Bluetooth* terminology.

The CCM block generates an encrypted keystream, applies it to the input data using the XOR operation, and generates the 4 byte MIC field in one operation. The CCM and radio can be configured to work synchronously, as described in the *nRF51 Series Reference Manual*. The CCM will encrypt in time for transmission and decrypt after receiving bytes into memory from the Radio. All operations can complete within the packet RX or TX time.

CCM on this device is implemented according to *Bluetooth* requirements and the algorithm as defined in IETF RFC3610, and depends on the AES-128 block cipher. A description of the CCM algorithm can also be found in the NIST Special Publication 800-38C. The *Bluetooth* Core Specification v4.0 describes the configuration of counter mode blocks and encryption blocks to implement compliant encryption for BLE.

The CCM block uses EasyDMA to load key, counter mode blocks (including the nonce required), and to read/write plain text and cipher text.

4.6 Accelerated Address Resolver (AAR)

Accelerated Address Resolver is a cryptographic support function to implement the "Resolvable Private Address Resolution Procedure" described in the *Bluetooth Core Specification* v4.1. "Resolvable Private Address Generation" should be achieved using ECB and is not supported by AAR. The procedure allows two devices that share a secret key to generate and resolve a hash based on their device address.

The AAR block enables real-time address resolution on incoming packets when configured according to the description in the *nRF51 Series Reference Manual*. This allows real-time packet filtering (whitelisting) using a list of known shared secrets (Identity Resolving Keys (IRK) in *Bluetooth*).

The following table outlines the properties of the AAR.

Instance	Number of IRKs supported for simultaneous resolution
AAR	8

***Table 11** AAR properties*

4.7 Random Number Generator (RNG)

The Random Number Generator (RNG) generates true non-deterministic random numbers derived from thermal noise that are suitable for cryptographic purposes. The RNG does not require a seed value.

4.8 Watchdog Timer (WDT)

A countdown watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up. The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU.