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nRF52832 Product Specification v1.4

Key features

- 2.4 GHz transceiver
  - -96 dBm sensitivity in *Bluetooth*® low energy mode
  - Supported data rates: 1 Mbps, 2 Mbps *Bluetooth*® low energy mode
  - -20 to +4 dBm TX power, configurable in 4 dB steps
  - On-chip balun (single-ended RF)
  - 5.3 mA peak current in TX (0 dBm)
  - 5.4 mA peak current in RX
  - RSSI (1 dB resolution)
- ARM® Cortex®-M4 32-bit processor with FPU, 64 MHz
  - 215 EEMBC CoreMark® score running from flash memory
  - 58 µA/MHz running from flash memory
  - 51.6 µA/MHz running from RAM
  - Data watchpoint and trace (DWT), embedded trace macrocell (ETM), and instrumentation trace macrocell (ITM)
  - Serial wire debug (SWD)
  - Trace port
- Flexible power management
  - 1.7 V–3.6 V supply voltage range
  - Fully automatic LDO and DC/DC regulator system
  - Fast wake-up using 64 MHz internal oscillator
  - 0.3 µA at 3 V in System OFF mode
  - 0.7 µA at 3 V in System OFF mode with full 64 kB RAM retention
  - 1.9 µA at 3 V in System ON mode, no RAM retention, wake on RTC
- Memory
  - 512 kB flash/64 kB RAM
  - 256 kB flash/32 kB RAM
- Nordic SoftDevice ready
- Support for concurrent multi-protocol
- Type 2 near field communication (NFC-A) tag with wakeup-on-field and touch-to-pair capabilities
- 12-bit, 200 ksps ADC - 8 configurable channels with programmable gain
- 64 level comparator
- 15 level low power comparator with wakeup from System OFF mode
- Temperature sensor
- 32 general purpose I/O pins
- 3x 4-channel pulse width modulator (PWM) unit with EasyDMA
- Digital microphone interface (PDM)
- 5x 32-bit timer with counter mode
- Up to 3x SPI master/slave with EasyDMA
- Up to 2x I2C compatible 2-wire master/slave
- I2S with EasyDMA
- UART (CTS/RTS) with EasyDMA
- Programmable peripheral interconnect (PPI)
- Quadrature decoder (QDEC)
- AES HW encryption with EasyDMA
- Autonomous peripheral operation without CPU intervention using PPI and EasyDMA
- 3x real-time counter (RTC)
- Single crystal operation
- Package variants
  - QFN48 package, 6 × 6 mm
  - WLCSP package, 3.0 × 3.2 mm

Applications

- Internet of Things (IoT)
  - Home automation
  - Sensor networks
  - Building automation
  - Industrial
  - Retail
- Personal area networks
  - Health/fitness sensor and monitor devices
  - Medical devices
  - Key fobs and wrist watches
- Interactive entertainment devices
  - Remote controls
  - Gaming controllers
- Beacons
- A4WP wireless chargers and devices
- Remote control toys
- Computer peripherals and I/O devices
  - Mouse
  - Keyboard
  - Multi-touch trackpad
  - Gaming

2017-10-10

Contents

1 Revision history

Date	Version	Description
October 2017	1.4	The following content has been added or updated: • *Recommended operating conditions* on page 20: Added WLCSP light sensitivity information. • *FICR — Factory information configuration registers* on page 43: Added registers PARTNO, HWREVISION and PRODUCTIONREVISION. • *UICR — User information configuration registers* on page 54: Changed width of PSELRESETn port fields. • *SPIM*: Polarity in SPI mode table corrected. • *COMP — Comparator* on page 392: Documentation structure improvements/changes. • Liability disclaimer updated: Directive 2011/65/EU (RoHS 2).
February 2017	1.3	The following content has been added or updated: • *RADIO — 2.4 GHz Radio* on page 205: Introduced 2 Mbps Bluetooth® low energy mode. • *FICR — Factory information configuration registers* on page 43: Updated INFO.PACKAGE register (new package added). • *UARTE*: Corrected the pin configuration table. • *PPI — Programmable peripheral interconnect* on page 168: Timing information corrected. • Updated the liability disclaimer.
September 2016	1.2	Updated the following: • Power and clock management, *Current consumption: Ultra-low power* on page 77. • Power, *Current consumption, sleep* on page 99
July 2016	1.1	Added documentation for nRF52832 CIAA WLCSP. Added or updated the following content: • Cover: Added *Key features*. • *Pin assignments* on page 13: Added *WLCSP ball assignments*. Moved *GPIO usage restrictions* here from *GPIO/Notes on usage and restrictions*. • *Absolute maximum ratings* on page 19: Added environmental information for WLCSP to the table. • *Memory* on page 23: Added QFAB and CIAA information to the table. • *FICR — Factory information configuration registers* on page 43: Updated INFO.PACKAGE register. • *UICR — User information configuration registers* on page 54: Updated APPROTECT register. • *Debug and trace* on page 72: Updated *DAP - Debug access port*. • *POWER — Power supply* on page 78: Updated *Pin reset*. • *CLOCK — Clock control* on page 101: Updated information on external 32 kHz clock support. • *GPIO — General purpose input/output* on page 111: Added *GPIO located near the RADIO*. • *RADIO — 2.4 GHz Radio* on page 205: Updated Figure 29 and *Interframe spacing*. • *CCM*: Updated SCRATCHPTR register. • *SPIM*: Updated *Master mode pin configuration*. • *UARTE*: Added RXDRDY and TXDRDY events. • *NFCT*: Updated *Electrical specifications*. • *PWM — Pulse width modulation* on page 495: Updated SEQ[1].REFRESH register. • *Mechanical specifications* on page 540: Added *WLCSP package*. • *Ordering information* on page 542: Updated with CIAA and QFAB information. • *Reference circuitry* on page 545: QFAB information added. CIAA WLCSP schematics added.
February 2016	1.0	First release.

2 About this document

This product specification is organized into chapters based on the modules and peripherals that are available in this IC.

The peripheral descriptions are divided into separate sections that include the following information:

- A detailed functional description of the peripheral
- Register configuration for the peripheral
- Electrical specification tables, containing performance data which apply for the operating conditions described in *Recommended operating conditions* on page 20.

2.1 Document naming and status

Nordic uses three distinct names for this document, which are reflecting the maturity and the status of the document and its content.

Table 1: Defined document names

Document name	Description
Objective Product Specification (OPS)	Applies to document versions up to 0.7.
Preliminary Product Specification (PPS)	This product specification contains target specifications for product development. Applies to document versions 0.7 and up to 1.0.
Product Specification (PS)	This product specification contains preliminary data. Supplementary data may be published from Nordic Semiconductor ASA later. Applies to document versions 1.0 and higher. This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

2.2 Peripheral naming and abbreviations

Every peripheral has a unique capitalized name or an abbreviation of its name, e.g. TIMER, used for identification and reference. This name is used in chapter headings and references, and it will appear in the ARM® Cortex® Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer to identify the peripheral.

The peripheral instance name, which is different from the peripheral name, is constructed using the peripheral name followed by a numbered postfix, starting with 0, for example, TIMER0. A postfix is normally only used if a peripheral can be instantiated more than once. The peripheral instance name is also used in the CMSIS to identify the peripheral instance.

2.3 Register tables

Individual registers are described using register tables. These tables are built up of two sections. The first three colored rows describe the position and size of the different fields in the register. The following rows describe the fields in more detail.

2.3.1 Fields and values

The **Id (Field Id)** row specifies the bits that belong to the different fields in the register. If a field has enumerated values, then every value will be identified with a unique value id in the **Value Id** column.

A blank space means that the field is reserved and read as undefined, and it also must be written as `0` to secure forward compatibility. If a register is divided into more than one field, a unique field name is specified for each field in the **Field** column. The **Value Id** may be omitted in the single-bit bit fields when values can be substituted with a Boolean type enumerator range, e.g. true/false, disable(d)/enable(d), on/off, and so on.

Values are usually provided as decimal or hexadecimal. Hexadecimal values have a `0x` prefix, decimal values have no prefix.

The **Value** column can be populated in the following ways:

- Individual enumerated values, for example 1, 3, 9.
- Range of values, e.g. [0..4], indicating all values from and including 0 and 4.
- Implicit values. If no values are indicated in the **Value** column, all bit combinations are supported, or alternatively the field's translation and limitations are described in the text instead.

If two or more fields are closely related, the **Value Id**, **Value**, and **Description** may be omitted for all but the first field. Subsequent fields will indicate inheritance with '..'.

A feature marked **Deprecated** should not be used for new designs.

2.4 Registers

Table 2: Register Overview

Register	Offset	Description
DUMMY	0x514	Example of a register controlling a dummy feature

2.4.1 DUMMY

Address offset: 0x514

Example of a register controlling a dummy feature

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id								D	D	D	D						C	C	C								B							A	A
Reset 0x00050002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														**Description**	
A	RW	FIELD_A																																Example of a field with several enumerated values	
			Disabled	0																														The example feature is disabled	
			NormalMode	1																														The example feature is enabled in normal mode	
			ExtendedMode	2																														The example feature is enabled along with extra functionality	
B	RW	FIELD_B																																Example of a deprecated field	Deprecated
			Disabled	0																														The override feature is disabled	
			Enabled	1																														The override feature is enabled	
C	RW	FIELD_C																																Example of a field with a valid range of values	
			ValidRange	[2..7]																														Example of allowed values for this field	
D	RW	FIELD_D																																Example of a field with no restriction on the values	

3 Block diagram

This block diagram illustrates the overall system. Arrows with white heads indicate signals that share physical pins with other signals.

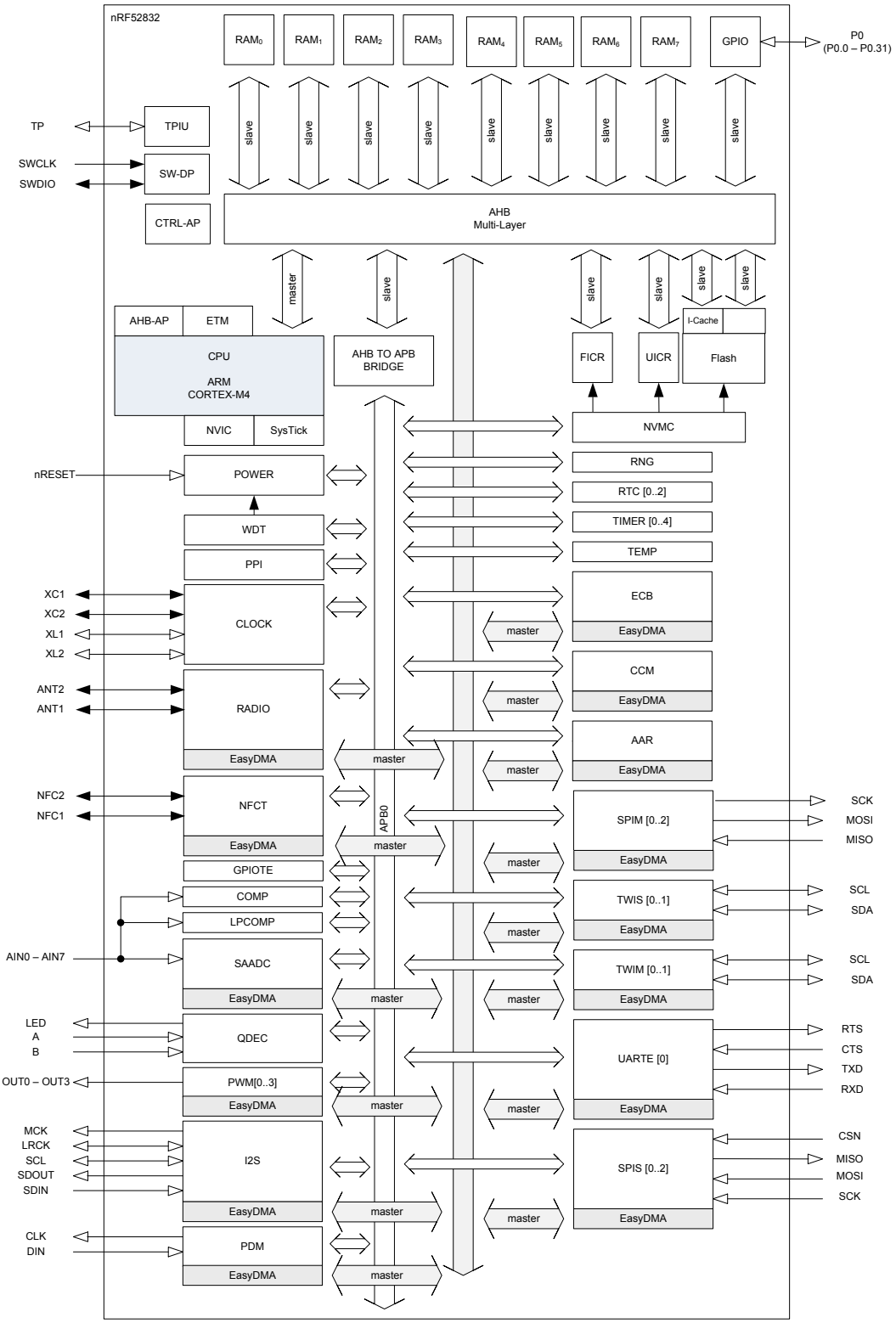

Figure 1: Block diagram

4 Pin assignments

Here we cover the pin assignments for each variant of the chip.

4.1 QFN48 pin assignments

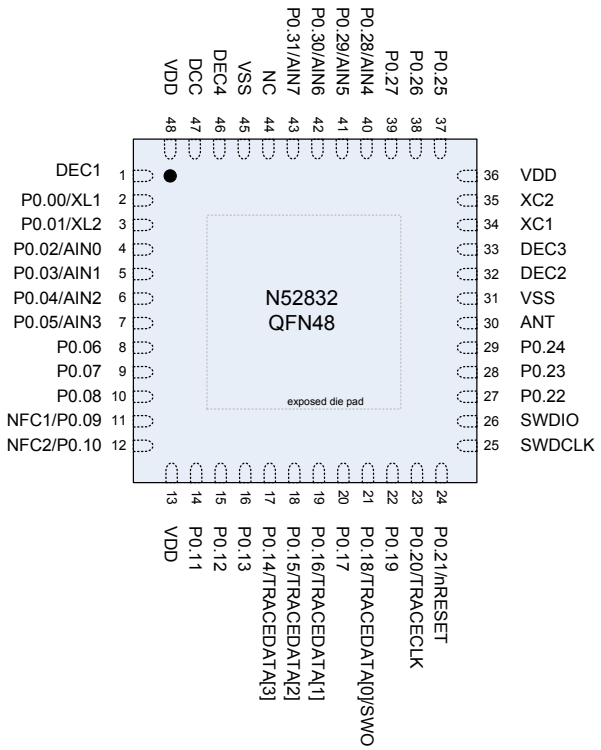

Figure 2: QFN48 pin assignments, top view

Table 3: QFN48 pin assignments

Pin	Name	Type	Description
Left Side of chip			
1	DEC1	Power	0.9 V regulator digital supply decoupling
2	P0.00	Digital I/O	General purpose I/O
	XL1	Analog input	Connection for 32.768 kHz crystal (LFXO)
3	P0.01	Digital I/O	General purpose I/O
	XL2	Analog input	Connection for 32.768 kHz crystal (LFXO)
4	P0.02	Digital I/O	General purpose I/O
	AIN0	Analog input	SAADC/COMP/LPCOMP input
5	P0.03	Digital I/O	General purpose I/O
	AIN1	Analog input	SAADC/COMP/LPCOMP input
6	P0.04	Digital I/O	General purpose I/O
	AIN2	Analog input	SAADC/COMP/LPCOMP input
7	P0.05	Digital I/O	General purpose I/O
	AIN3	Analog input	SAADC/COMP/LPCOMP input
8	P0.06	Digital I/O	General purpose I/O
9	P0.07	Digital I/O	General purpose I/O

Pin	Name	Type	Description
10	P0.08	Digital I/O	General purpose I/O
11	NFC1	NFC input	NFC antenna connection
	P0.09	Digital I/O	General purpose I/O[1]
12	NFC2	NFC input	NFC antenna connection
	P0.10	Digital I/O	General purpose I/O[1]
Bottom side of chip			
13	VDD	Power	Power supply
14	P0.11	Digital I/O	General purpose I/O
15	P0.12	Digital I/O	General purpose I/O
16	P0.13	Digital I/O	General purpose I/O
17	P0.14	Digital I/O	General purpose I/O
	TRACEDATA[3]		Trace port output
18	P0.15	Digital I/O	General purpose I/O
	TRACEDATA[2]		Trace port output
19	P0.16	Digital I/O	General purpose I/O
	TRACEDATA[1]		Trace port output
20	P0.17	Digital I/O	General purpose I/O
21	P0.18	Digital I/O	General purpose I/O
	TRACEDATA[0] / SWO		Single wire output Trace port output
22	P0.19	Digital I/O	General purpose I/O
23	P0.20	Digital I/O	General purpose I/O
	TRACECLK		Trace port clock output
24	P0.21	Digital I/O	General purpose I/O
	nRESET		Configurable as pin reset
Right Side of chip			
25	SWDCLK	Digital input	Serial wire debug clock input for debug and programming
26	SWDIO	Digital I/O	Serial wire debug I/O for debug and programming
27	P0.22	Digital I/O	General purpose I/O[2]
28	P0.23	Digital I/O	General purpose I/O[2]
29	P0.24	Digital I/O	General purpose I/O[2]
30	ANT	RF	Single-ended radio antenna connection
31	VSS	Power	Ground (Radio supply)
32	DEC2	Power	1.3 V regulator supply decoupling (Radio supply)
33	DEC3	Power	Power supply decoupling
34	XC1	Analog input	Connection for 32 MHz crystal
35	XC2	Analog input	Connection for 32 MHz crystal
36	VDD	Power	Power supply
Top side of chip			
37	P0.25	Digital I/O	General purpose I/O[2]
38	P0.26	Digital I/O	General purpose I/O[2]
39	P0.27	Digital I/O	General purpose I/O[2]
40	P0.28	Digital I/O	General purpose I/O[2]
	AIN4	Analog input	SAADC/COMP/LPCOMP input
41	P0.29	Digital I/O	General purpose I/O[2]
	AIN5	Analog input	SAADC/COMP/LPCOMP input
42	P0.30	Digital I/O	General purpose I/O[2]
	AIN6	Analog input	SAADC/COMP/LPCOMP input
43	P0.31	Digital I/O	General purpose I/O pin[2]
	AIN7	Analog input	SAADC/COMP/LPCOMP input

Pin	Name	Type	Description
44	NC		No connect Leave unconnected
45	VSS	Power	Ground
46	DEC4	Power	1.3 V regulator supply decoupling Input from DC/DC regulator Output from 1.3 V LDO
47	DCC	Power	DC/DC regulator output
48	VDD	Power	Power supply
Bottom of chip			
Die pad	VSS	Power	Ground pad Exposed die pad must be connected to ground (VSS) for proper device operation.

4.2 WLCSP ball assignments

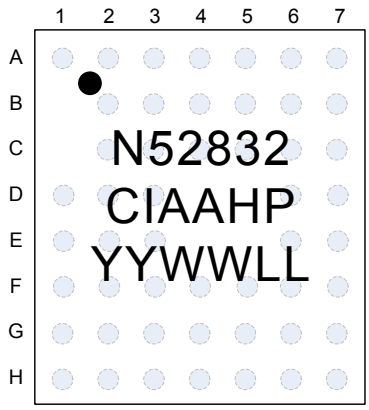

Figure 3: WLCSP ball assignments, top view

Table 4: WLCSP ball assignments

Ball	Name		Description
A1	XC2	Analog input	Connection for 32 MHz crystal
A2	DEC2	Power	1.3 V regulator supply decoupling (Radio supply)
A3	P0.28	Digital I/O	General purpose I/O[3]
	AIN4	Analog input	SAADC/COMP/LPCOMP input
A4	P0.29	Digital I/O	General purpose I/O[3]
	AIN5	Analog input	SAADC/COMP/LPCOMP input
A5	P0.30	Digital I/O	General purpose I/O[3]
	AIN6	Analog input	SAADC/COMP/LPCOMP input
A6	DEC4	Power	1.3 V regulator supply decoupling Input from DC/DC converter. Output from 1.3 V LDO
A7	VDD	Power	Power supply
B2	XC1	Analog input	Connection for 32 MHz crystal
B3	P0.25	Digital I/O	General purpose I/O[3]

[1] See *GPIO located near the radio* on page 17 for more information.
[2] See *NFC antenna pins* on page 17 for more information.

Ball	Name		Description
B4	P0.27	Digital I/O	General purpose I/O[3]
B5	P0.31	Digital I/O	General purpose I/O[3]
	AIN7	Analog input	SAADC/COMP/LPCOMP input
B6	DCC	Power	DC/DC converter output
B7	DEC1	Power	0.9 V regulator digital supply decoupling
C2	DEC3	Power	Power supply decoupling
C3	NC	N/A	Not connected
C4	VSS	Power	Ground
C5	VSS	Power	Ground
C6	P0.02	Digital I/O	General purpose I/O
	AIN0	Analog input	SAADC/COMP/LPCOMP input
C7	P0.01	Digital I/O	General purpose I/O
	XL2	Analog input	Connection for 32.768 kHz crystal (LFXO)
D1	ANT	RF	Single-ended radio antenna connection
D2	VSS_PA	Power	Ground (Radio supply)
D3	P0.26	Digital I/O	General purpose I/O [3]
D6	P0.03	Digital I/O	General purpose I/O
	AIN1	Analog input	SAADC/COMP/LPCOMP input
D7	P0.00	Digital I/O	General purpose I/O
	XL1	Analog input	Connection for 32.768 kHz crystal (LFXO)
E1	P0.24	Digital I/O	General purpose I/O[3]
E2	P0.23	Digital I/O	General purpose I/O[3]
E3	VSS	Power	Ground
E6	P0.04	Digital I/O	General purpose I/O
	AIN2	Analog input	SAADC/COMP/LPCOMP input
E7	P0.05	Digital I/O	General purpose I/O
	AIN3	Analog input	SAADC/COMP/LPCOMP input
F1	SWDCLK	Digital input	Serial wire debug clock input for debug and programming
F2	P0.22	Digital I/O	General purpose I/O[3]
F3	P0.19	Digital I/O	General purpose I/O
F4	P0.11	Digital I/O	General purpose I/O
F5	VSS	Power	Ground
F6	P0.07	Digital I/O	General purpose I/O
F7	P0.06	Digital I/O	General purpose I/O
G1	SWDIO	Digital I/O	Serial wire debug I/O for debug and programming
G2	P0.20	Digital I/O	General purpose I/O
	TRACECLK		Trace port clock output
G3	P0.17	Digital I/O	General purpose I/O
G4	P0.13	Digital I/O	General purpose I/O
G5	NFC2	NFC input	NFC antenna connection
	P0.10	Digital I/O	General purpose I/O[4]
G6	NFC1	NFC input	NFC antenna connection
	P0.09	Digital I/O	General purpose I/O[4]
G7	P0.08	Digital I/O	General purpose I/O
H1	P0.21	Digital I/O	General purpose I/O
	nRESET		Configurable as pin reset
H2	P0.18	Digital I/O	General purpose I/O
	TRACEDATA[0]		Trace port output
H3	P0.16	Digital I/O	General purpose I/O
	TRACEDATA[1]		Trace port output
H4	P0.15	Digital I/O	General purpose I/O

Ball	Name		Description
	TRACEDATA[2]		Trace port output
H5	P0.14	Digital I/O	General purpose I/O
	TRACEDATA[3]		Trace port output
H6	P0.12	Digital I/O	General purpose I/O
H7	VDD	Power	Power supply

4.3 GPIO usage restrictions

4.3.1 GPIO located near the radio

Radio performance parameters, such as sensitivity, may be affected by high frequency digital I/O with large sink/source current close to the Radio power supply and antenna pins.

Table 5: GPIO recommended usage for QFN48 package on page 17 and *Table 6: GPIO recommended usage for WLCSP package* on page 17 identify some GPIO that have recommended usage guidelines to maximize radio performance in an application.

Table 5: GPIO recommended usage for QFN48 package

Pin	GPIO	Recommended usage
27	P0.22	Low drive, low frequency I/O only.
28	P0.23	
29	P0.24	
37	P0.25	
38	P0.26	
39	P0.27	
40	P0.28	
41	P0.29	
42	P0.30	
43	P0.31	

Table 6: GPIO recommended usage for WLCSP package

Pin	GPIO	Recommended usage
F2	P0.22	Low drive, low frequency I/O only.
E2	P0.23	
E1	P0.24	
B3	P0.25	
D3	P0.26	
B4	P0.27	
A3	P0.28	
A4	P0.29	
A5	P0.30	
B5	P0.31	

4.3.2 NFC antenna pins

Two physical pins can be configured either as NFC antenna pins (factory default), or as GPIOs, as shown below.

Table 7: GPIO pins used by NFC

NFC pad name	GPIO
NFC1	P0.09
NFC2	P0.10

When configured as NFC antenna pins, the GPIOs on those pins will automatically be set to DISABLE state and a protection circuit will be enabled preventing the chip from being damaged in the presence of a strong NFC field. The protection circuit will short the two pins together if voltage difference exceeds approximately 2 V.

[3] See *GPIO located near the radio* on page 17 for more information.
[4] See *NFC antenna pins* on page 17 for more information.

For information on how to configure these pins as normal GPIOs, see *NFCT — Near field communication tag* on page 416 and *UICR — User information configuration registers* on page 54. Note that the device will not be protected against strong NFC field damage if the pins are configured as GPIO and an NFC antenna is connected to the device. The pins will always be configured as NFC pins during power-on reset until the configuration is set according to the UICR register.

These two pins will have some limitations when configured as GPIO. The pin capacitance will be higher on these pins, and there is some current leakage between the two pins if they are driven to different logical values. To avoid leakage between the pins when configured as GPIO, these GPIOs should always be at the same logical value whenever entering one of the device power saving modes. See *Electrical specification*.

5 Absolute maximum ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

Table 8: Absolute maximum ratings

	Min.	Max.	Unit
Supply voltages			
VDD	-0.3	+3.9	V
VSS		0	V
I/O pin voltage			
$V_{I/O}$, VDD ≤3.6 V	-0.3	VDD + 0.3 V	V
$V_{I/O}$, VDD >3.6 V	-0.3	3.9 V	V
NFC antenna pin current			
$I_{NFC1/2}$		80	mA
Radio			
RF input level		10	dBm
Environmental QFN48, 6×6 mm package			
Storage temperature	-40	+125	°C
MSL (moisture sensitivity level)		2	
ESD HBM (human body model)		4	kV
ESD CDM (charged device model)		1000	V
Environmental WLCSP, 3.0×3.2 mm package			
Storage temperature	-40	+125	°C
MSL		1	
ESD HBM		2	kV
ESD CDM		500	V
Flash memory			
Endurance	10 000		Write/erase cycles
Retention	10 years at 40°C		

6 Recommended operating conditions

The operating conditions are the physical parameters that the chip can operate within.

Table 9: Recommended operating conditions

Symbol	Parameter	Notes	Min.	Nom.	Max.	Units
VDD	Supply voltage, independent of DCDC enable		1.7	3.0	3.6	V
t_{R_VDD}	Supply rise time (0 V to 1.7 V)				60	ms
TA	Operating temperature		-40	25	85	°C

Important: The on-chip power-on reset circuitry may not function properly for rise times longer than the specified maximum.

6.1 WLCSP light sensitivity

All WLCSP package variants are sensitive to visible and close-range infrared light. This means that a final product design must shield the chip properly, either by final product encapsulation or by shielding/coating of the WLCSP device.

7 CPU

The ARM® Cortex®-M4 processor with floating-point unit (FPU) has a 32-bit instruction set (Thumb®-2 technology) that implements a superset of 16 and 32-bit instructions to maximize code density and performance.

This processor implements several features that enable energy-efficient arithmetic and high-performance signal processing including:

- Digital signal processing (DSP) instructions
- Single-cycle multiply and accumulate (MAC) instructions
- Hardware divide
- 8 and 16-bit single instruction multiple data (SIMD) instructions
- Single-precision floating-point unit (FPU)

The ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM Cortex processor series is implemented and available for the M4 CPU.

Real-time execution is highly deterministic in thread mode, to and from sleep modes, and when handling events at configurable priority levels via the Nested Vectored Interrupt Controller (NVIC).

Executing code from flash will have a wait state penalty on the nRF52 Series. An instruction cache can be enabled to minimize flash wait states when fetching instructions. For more information on cache, see *Cache* on page 30. The section *Electrical specification* on page 21 shows CPU performance parameters including wait states in different modes, CPU current and efficiency, and processing power and efficiency based on the CoreMark® benchmark.

7.1 Floating point interrupt

The floating point unit (FPU) may generate exceptions when used due to e.g. overflow or underflow. These exceptions will trigger the FPU interrupt (see *Instantiation* on page 24). To clear the IRQ line when an exception has occurred, the relevant exception bit within the FPSCR register needs to be cleared. For more information about the FPSCR or other FPU registers, see *Cortex-M4 Devices Generic User Guide*.

7.2 Electrical specification

7.2.1 CPU performance

The CPU clock speed is 64 MHz. Current and efficiency data is taken when in System ON and the CPU is executing the CoreMark™ benchmark. It includes power regulator and clock base currents. All other blocks are IDLE.

Symbol	Description	Min.	Typ.	Max.	Units
W_{FLASH}	CPU wait states, running from flash, cache disabled	0		2	
$W_{FLASHCACHE}$	CPU wait states, running from flash, cache enabled	0		3	
W_{RAM}	CPU wait states, running from RAM			0	
$I_{DDFLASHCACHE}$	CPU current, running from flash, cache enabled, LDO		7.4		mA
$I_{DDFLASHCACHEDCDC}$	CPU current, running from flash, cache enabled, DCDC 3V		3.7		mA
$I_{DDFLASH}$	CPU current, running from flash, cache disabled, LDO		8.0		mA
$I_{DDFLASHDCDC}$	CPU current, running from flash, cache disabled, DCDC 3V		3.9		mA
I_{DDRAM}	CPU current, running from RAM, LDO		6.7		mA
$I_{DDRAMDCDC}$	CPU current, running from RAM, DCDC 3V		3.3		mA
$I_{DDFLASH/MHz}$	CPU efficiency, running from flash, cache enabled, LDO		125		µA/MHz
$I_{DDFLASHDCDC/MHz}$	CPU efficiency, running from flash, cache enabled, DCDC 3V		58		µA/MHz

Symbol	Description	Min.	Typ.	Max.	Units
CM_{FLASH}	CoreMark[5], running from flash, cache enabled		215		CoreM
$CM_{FLASH/MHz}$	CoreMark per MHz, running from flash, cache enabled		3.36		CoreM/MHz
$CM_{FLASH/mA}$	CoreMark per mA, running from flash, cache enabled, DCDC 3V		58		CoreM/mA

7.3 CPU and support module configuration

The ARM® Cortex®-M4 processor has a number of CPU options and support modules implemented on the device.

Option / Module	Description	Implemented
Core options		
NVIC	Nested Vector Interrupt Controller	37 vectors
PRIORITIES	Priority bits	3
WIC	Wakeup Interrupt Controller	NO
Endianness	Memory system endianness	Little endian
Bit Banding	Bit banded memory	NO
DWT	Data Watchpoint and Trace	YES
SysTick	System tick timer	YES
Modules		
MPU	Memory protection unit	YES
FPU	Floating point unit	YES
DAP	Debug Access Port	YES
ETM	Embedded Trace Macrocell	YES
ITM	Instrumentation Trace Macrocell	YES
TPIU	Trace Port Interface Unit	YES
ETB	Embedded Trace Buffer	NO
FPB	Flash Patch and Breakpoint Unit	YES
HTM	AHB Trace Macrocell	NO

[5] Using IAR v6.50.1.4452 with flags --endian=little --cpu=Cortex-M4 -e --fpu=VFPv4_sp –Ohs --no_size_constraints

8 Memory

The nRF52832 contains flash and RAM that can be used for code and data storage.

The amount of RAM and flash will vary depending on variant, see *Table 10: Memory variants* on page 23.

Table 10: Memory variants

Device name	RAM	Flash	Comments
nRF52832-QFAA	64 kB	512 kB	
nRF52832-QFAB	32 kB	256 kB	
nRF52832-CIAA	64 kB	512 kB	

The CPU and the EasyDMA can access memory via the AHB multilayer interconnect. The CPU is also able to access peripherals via the AHB multilayer interconnect, as illustrated in *Figure 4: Memory layout* on page 23.

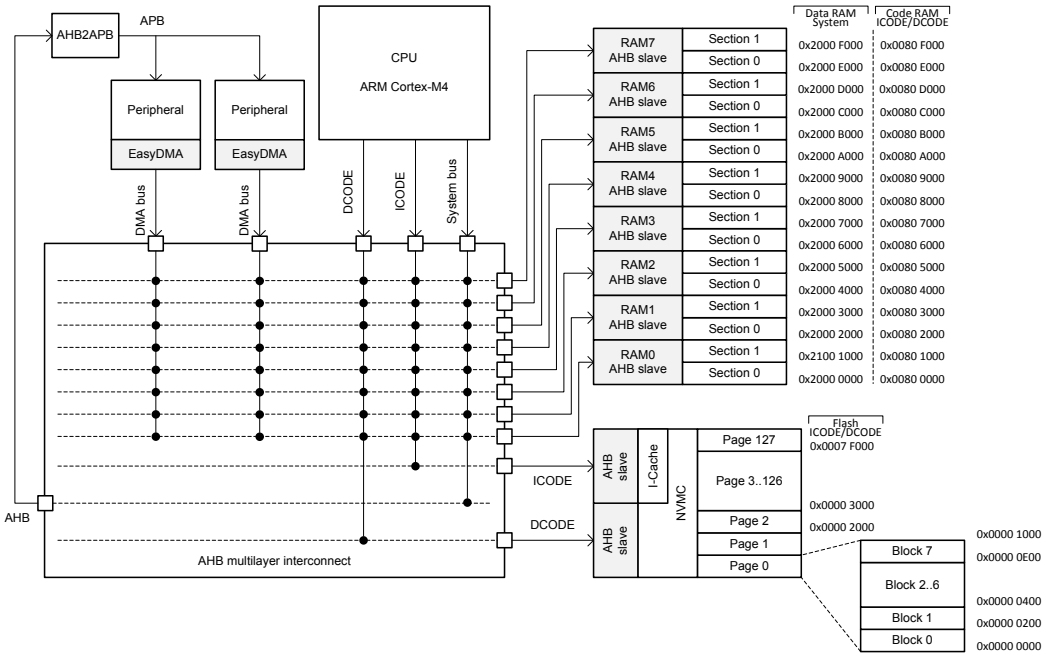

Figure 4: Memory layout

See *AHB multilayer* on page 26 and *EasyDMA* on page 27 for more information about the AHB multilayer interconnect and the EasyDMA.

The same physical RAM is mapped to both the Data RAM region and the Code RAM region. It is up to the application to partition the RAM within these regions so that one does not corrupt the other.

8.1 RAM - Random access memory

The RAM interface is divided into multiple RAM AHB slaves.

Each RAM AHB slave is connected to two 4-kilobyte RAM sections, see Section 0 and Section 1 in *Figure 4: Memory layout* on page 23.

Each of the RAM sections have separate power control for System ON and System OFF mode operation, which is configured via RAM register (see the *POWER — Power supply* on page 78).

8.2 Flash - Non-volatile memory

The Flash can be read an unlimited number of times by the CPU, but it has restrictions on the number of times it can be written and erased and also on how it can be written.

Writing to Flash is managed by the Non-volatile memory controller (NVMC), see *NVMC — Non-volatile memory controller* on page 29.

The Flash is divided into multiple pages that can be accessed by the CPU via both the ICODE and DCODE buses as shown in, *Figure 4: Memory layout* on page 23. Each page is divided into 8 blocks.

8.3 Memory map

The complete memory map is shown in *Figure 5: Memory map* on page 24. As described in *Memory* on page 23, Code RAM and the Data RAM are the same physical RAM.

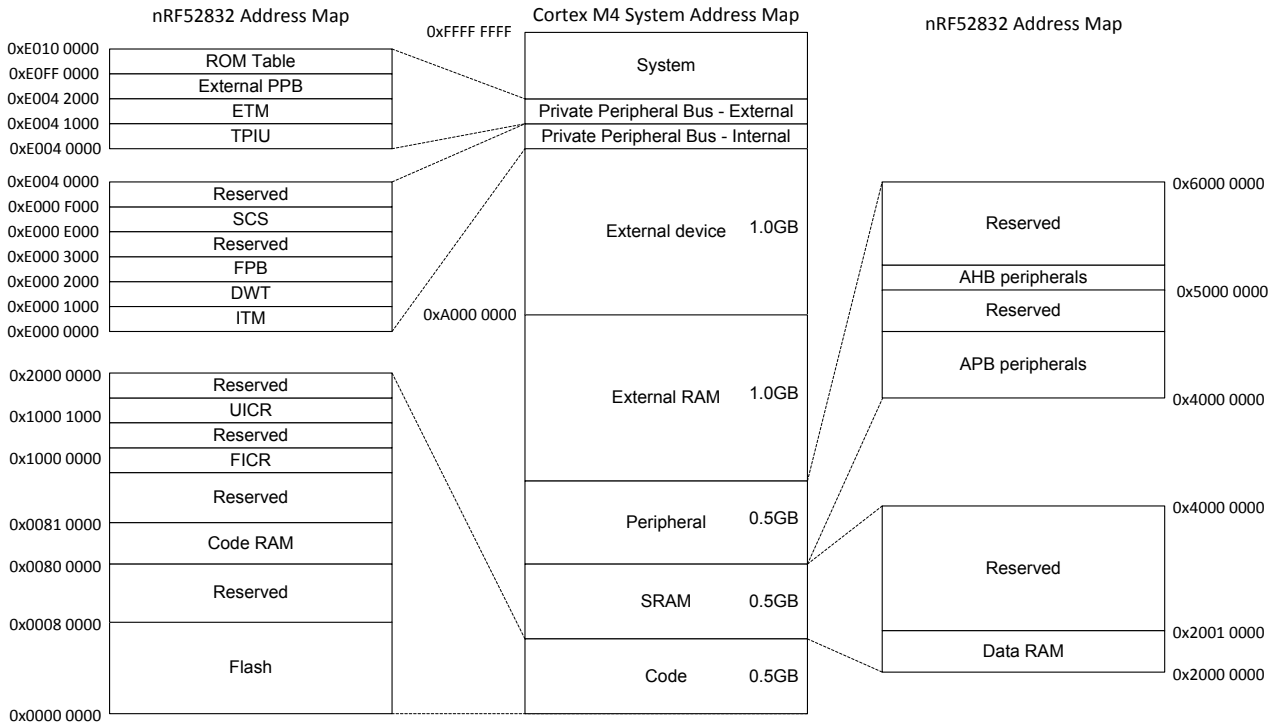

Figure 5: Memory map

8.4 Instantiation

Table 11: Instantiation table

ID	Base Address	Peripheral	Instance	Description	
0	0x40000000	CLOCK	CLOCK	Clock control	
0	0x40000000	POWER	POWER	Power control	
0	0x40000000	BPROT	BPROT	Block Protect	
1	0x40001000	RADIO	RADIO	2.4 GHz radio	
2	0x40002000	UARTE	UARTE0	Universal Asynchronous Receiver/Transmitter with EasyDMA	
2	0x40002000	UART	UART0	Universal Asynchronous Receiver/Transmitter	Deprecated
3	0x40003000	SPIM	SPIM0	SPI master 0	
3	0x40003000	SPIS	SPIS0	SPI slave 0	
3	0x40003000	TWIM	TWIM0	Two-wire interface master 0	
3	0x40003000	TWI	TWI0	Two-wire interface master 0	Deprecated
3	0x40003000	SPI	SPI0	SPI master 0	Deprecated

ID	Base Address	Peripheral	Instance	Description	
3	0x40003000	TWIS	TWIS0	Two-wire interface slave 0	
4	0x40004000	SPIM	SPIM1	SPI master 1	
4	0x40004000	TWI	TWI1	Two-wire interface master 1	Deprecated
4	0x40004000	SPIS	SPIS1	SPI slave 1	
4	0x40004000	TWIS	TWIS1	Two-wire interface slave 1	
4	0x40004000	TWIM	TWIM1	Two-wire interface master 1	
4	0x40004000	SPI	SPI1	SPI master 1	Deprecated
5	0x40005000	NFCT	NFCT	Near Field Communication Tag	
6	0x40006000	GPIOTE	GPIOTE	GPIO Tasks and Events	
7	0x40007000	SAADC	SAADC	Analog to digital converter	
8	0x40008000	TIMER	TIMER0	Timer 0	
9	0x40009000	TIMER	TIMER1	Timer 1	
10	0x4000A000	TIMER	TIMER2	Timer 2	
11	0x4000B000	RTC	RTC0	Real-time counter 0	
12	0x4000C000	TEMP	TEMP	Temperature sensor	
13	0x4000D000	RNG	RNG	Random number generator	
14	0x4000E000	ECB	ECB	AES Electronic Code Book (ECB) mode block encryption	
15	0x4000F000	CCM	CCM	AES CCM Mode Encryption	
15	0x4000F000	AAR	AAR	Acelerated Address Resolver	
16	0x40010000	WDT	WDT	Watchdog timer	
17	0x40011000	RTC	RTC1	Real-time counter 1	
18	0x40012000	QDEC	QDEC	Quadrature decoder	
19	0x40013000	LPCOMP	LPCOMP	Low power comparator	
19	0x40013000	COMP	COMP	General purpose comparator	
20	0x40014000	SWI	SWI0	Software interrupt 0	
20	0x40014000	EGU	EGU0	Event Generator Unit 0	
21	0x40015000	EGU	EGU1	Event Generator Unit 1	
21	0x40015000	SWI	SWI1	Software interrupt 1	
22	0x40016000	SWI	SWI2	Software interrupt 2	
22	0x40016000	EGU	EGU2	Event Generator Unit 2	
23	0x40017000	SWI	SWI3	Software interrupt 3	
23	0x40017000	EGU	EGU3	Event Generator Unit 3	
24	0x40018000	EGU	EGU4	Event Generator Unit 4	
24	0x40018000	SWI	SWI4	Software interrupt 4	
25	0x40019000	SWI	SWI5	Software interrupt 5	
25	0x40019000	EGU	EGU5	Event Generator Unit 5	
26	0x4001A000	TIMER	TIMER3	Timer 3	
27	0x4001B000	TIMER	TIMER4	Timer 4	
28	0x4001C000	PWM	PWM0	Pulse Width Modulation Unit 0	
29	0x4001D000	PDM	PDM	Pulse Density Modulation (Digital Microphone Interface)	
30	0x4001E000	NVMC	NVMC	Non-Volatile Memory Controller	
31	0x4001F000	PPI	PPI	Programmable Peripheral Interconnect	
32	0x40020000	MWU	MWU	Memory Watch Unit	
33	0x40021000	PWM	PWM1	Pulse Width Modulation Unit 1	
34	0x40022000	PWM	PWM2	Pulse Width Modulation Unit 2	
35	0x40023000	SPI	SPI2	SPI master 2	Deprecated
35	0x40023000	SPIS	SPIS2	SPI slave 2	
35	0x40023000	SPIM	SPIM2	SPI master 2	
36	0x40024000	RTC	RTC2	Real-time counter 2	
37	0x40025000	I2S	I2S	Inter-IC Sound Interface	
38	0x40026000	FPU	FPU	FPU interrupt	
0	0x50000000	GPIO	GPIO	General purpose input and output	Deprecated
0	0x50000000	GPIO	P0	General purpose input and output	
N/A	0x10000000	FICR	FICR	Factory Information Configuration	
N/A	0x10001000	UICR	UICR	User Information Configuration	