Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

nRF52840 Objective Product Specification v0.5.1

Key features

- *Bluetooth*® 5, IEEE 802.15.4-2006, 2.4 GHz transceiver
  - -95 dBm sensitivity in 1 Mbps *Bluetooth*® low energy (BLE) mode
  - -103 dBm sensitivity in 125 kbps BLE mode (long range)
  - +8 dBm TX power (down to -20 dBm in 4 dB steps)
  - On-air compatible with nRF52, nRF51, nRF24L and nRF24AP Series
  - Supported data rates:
    - Bluetooth 5: 2 Mbps, 1 Mbps, 500 kbps, 125 kbps
    - IEEE 802.15.4-2006: 250 kbps
    - Proprietary 2.4 GHz: 2 Mbps, 1 Mbps
  - Single-ended antenna output (on-chip balun)
  - 4.9 mA peak current in TX (0 dBm)
  - 4.8 mA peak current in RX
  - RSSI (1 dB resolution)
- ARM® Cortex®-M4 32-bit processor with FPU, 64 MHz
  - 212 EEMBC CoreMark® score running from flash memory
  - 56 µA/MHz running from flash memory
  - Watchpoint and trace debug modules (DWT, ETM and ITM)
  - Serial wire debug (SWD)
- Flexible power management
  - Supply voltage range 1.7 V to 5.5 V
  - On-chip DC/DC and LDO regulators with automated low current modes
  - Regulated supply for external components from 1.8 V to 3.3 V
  - Automated peripheral power management
  - Fast wake-up using 64 MHz internal oscillator
  - 0.4 µA at 3 V in OFF mode, no RAM retention
  - 1.3 µA at 3 V in ON mode, no RAM retention, wake on RTC
- Memory
  - 1 MB flash/256 kB RAM
- HW accelerated security
  - ARM® TrustZone® Cryptocell 310 cryptographic accelerator
  - 128 bit AES/ECB/CCM/AAR co-processor (on-the-fly packet encryption)
- Advanced on-chip interfaces
  - USB 2.0 full speed (12 Mbps) controller
  - QSPI 32 MHz interface
  - High speed 32 MHz SPI
  - Type 2 near field communication (NFC-A) tag with wake-on field
    - Touch-to-pair support
  - Programmable peripheral interconnect (PPI)
  - 48 general purpose I/O pins
  - EasyDMA automated data transfer without CPU processing on peripherals
- Nordic SoftDevice ready and with support for concurrent multi-protocol
- 12-bit, 200 ksps ADC - 8 configurable channels with programmable gain
- 64 level comparator
- 15 level low-power comparator with wake-up from System OFF mode
- Temperature sensor
- 4x 4-channel pulse width modulator (PWM) units with EasyDMA
- Audio peripherals: I2S, digital microphone interface (PDM)
- 5x 32-bit timers with counter mode
- Up to 4x SPI masters/3x SPI slaves with EasyDMA
- Up to 2x I2C compatible 2-wire masters/slaves
- 2x UART (CTS/RTS) with EasyDMA
- Quadrature decoder (QDEC)
- 3x real-time counters (RTC)
- Package variants
  - AQFN73 package, 7 × 7 mm

Applications

- Advanced computer peripherals and I/O devices
  - Mouse
  - Keyboard
  - Multi-touch trackpad
- Advanced wearables
  - Health/fitness sensor and monitor devices
  - Wireless payment enabled devices
- Internet of things (IoT)
  - Smart home sensors and controllers
  - Industrial IoT sensors and controllers
- Interactive entertainment devices
  - Remote controls
  - Gaming controllers

2017-07-06

Contents

1 Revision history

Date	Version	Description

July 2017	0.5.1	The following content is changed in this version:
		• *Pin assignments* on page 13: Added description for trace pins
		• *CPU* on page 18: Improved SysTick timer description
		• *Memory* on page 20: Memory map figure updated
		• *AHB multilayer* on page 25: Added SPIM3 and updated RAMPRI registers
		• *EasyDMA* on page 26: Miscellaneous documentation improvements
		• *UICR — User information configuration registers* on page 44: Improved APPROTECT description and added DEBUGCTRL register
		• *SPIM — Serial peripheral interface master with EasyDMA* on page 340: Fixed error in mode table and changed the base address of SPIM3
		• *Debug and trace* on page 62: Added r_pull parameter for CTRL-AP, in addition to miscellaneous documentation improvements
		• *POWER — Power supply* on page 66:
		  • Added clarifications for supplying external circuitry
		  • Improved register descriptions
		  • Removed deprecated RAMON and RAMONB registers
		  • Removed pin reset from CTRL-AP feature
		  • Improved description of POFCON
		• *CLOCK — Clock control* on page 141:
		  • Added HFXO debounce functionality
		  • Changed LFRC accuracy to +- 500 ppm
		  • Improved description in TRACECONFIG register
		• *RADIO — 2.4 GHz Radio* on page 249:
		  • Removed 9 dBm output power option
		  • Updated TX sequence figure
		  • Improved TIFS description
		  • Added PHYEND event
		  • Added PDUSTAT register
		  • Removed 250 kbit/s Nordic proprietary mode
		  • Changed to using term bps instead of sps for data rate in electrical specifications
		• *SAADC — Successive approximation analog-to-digital converter* on page 418: Updated VDD/5 input specification
		• *COMP — Comparator* on page 453: REFSEL AREF value changed
		• *PWM — Pulse width modulation* on page 558: Changed width of DECODER.LOAD field
		• *PDM — Pulse density modulation interface* on page 499: Fixed error in electrical specification units
		• *I2S — Inter-IC sound interface* on page 508: PSEL registers PORT field updated
		• *Reference circuitry* on page 688: Reference schematics updated and erroneous sentence for VDD/VDDH connection removed
		• *Block diagram* on page 12: Miscellaneous improvements

December 2016	0.5	First release

2 About this document

This product specification is organized into chapters based on the modules and peripherals that are available in this IC.

The peripheral descriptions are divided into separate sections that include the following information:

- A detailed functional description of the peripheral
- Register configuration for the peripheral
- Electrical specification tables, containing performance data which apply for the operating conditions described in *Recommended operating conditions* on page 17.

2.1 Document naming and status

Nordic uses three distinct names for this document, which are reflecting the maturity and the status of the document and its content.

Table 1: Defined document names

Document name	Description
Objective Product Specification (OPS)	Applies to document versions up to 0.7.
Preliminary Product Specification (PPS)	This product specification contains target specifications for product development. Applies to document versions 0.7 and up to 1.0.
Product Specification (PS)	This product specification contains preliminary data. Supplementary data may be published from Nordic Semiconductor ASA later. Applies to document versions 1.0 and higher. This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

2.2 Peripheral naming and abbreviations

Every peripheral has a unique capitalized name or an abbreviation of its name, e.g. TIMER, used for identification and reference. This name is used in chapter headings and references, and it will appear in the ARM® Cortex® Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer to identify the peripheral.

The peripheral instance name, which is different from the peripheral name, is constructed using the peripheral name followed by a numbered postfix, starting with 0, for example, TIMER0. A postfix is normally only used if a peripheral can be instantiated more than once. The peripheral instance name is also used in the CMSIS to identify the peripheral instance.

2.3 Register tables

Individual registers are described using register tables. These tables are built up of two sections. The first three colored rows describe the position and size of the different fields in the register. The following rows describe the fields in more detail.

2.3.1 Fields and values

The **Id (Field Id)** row specifies the bits that belong to the different fields in the register. If a field has enumerated values, then every value will be identified with a unique value id in the **Value Id** column.

A blank space means that the field is reserved and read as undefined, and it also must be written as `0` to secure forward compatibility. If a register is divided into more than one field, a unique field name is specified for each field in the **Field** column. The **Value Id** may be omitted in the single-bit bit fields when values can be substituted with a Boolean type enumerator range, e.g. true/false, disable(d)/enable(d), on/off, and so on.

Values are usually provided as decimal or hexadecimal. Hexadecimal values have a `0x` prefix, decimal values have no prefix.

The **Value** column can be populated in the following ways:

- Individual enumerated values, for example 1, 3, 9.
- Range of values, e.g. [0..4], indicating all values from and including 0 and 4.
- Implicit values. If no values are indicated in the **Value** column, all bit combinations are supported, or alternatively the field's translation and limitations are described in the text instead.

If two or more fields are closely related, the **Value Id**, **Value**, and **Description** may be omitted for all but the first field. Subsequent fields will indicate inheritance with '..'.

A feature marked **Deprecated** should not be used for new designs.

2.4 Registers

Table 2: Register Overview

Register	Offset	Description
DUMMY	0x514	Example of a register controlling a dummy feature

2.4.1 DUMMY

Address offset: 0x514

Example of a register controlling a dummy feature

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id								D	D	D	D						C	C	C								B							A	A
Reset 0x00050002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														**Description**	
A	RW	FIELD_A																																Example of a field with several enumerated values	
			Disabled	0																														The example feature is disabled	
			NormalMode	1																														The example feature is enabled in normal mode	
			ExtendedMode	2																														The example feature is enabled along with extra functionality	
B	RW	FIELD_B																																Example of a deprecated field	Deprecated
			Disabled	0																														The override feature is disabled	
			Enabled	1																														The override feature is enabled	
C	RW	FIELD_C																																Example of a field with a valid range of values	
			ValidRange	[2..7]																														Example of allowed values for this field	
D	RW	FIELD_D																																Example of a field with no restriction on the values	

3 Block diagram

This block diagram illustrates the overall system. Arrows with white heads indicate signals that share physical pins with other signals.

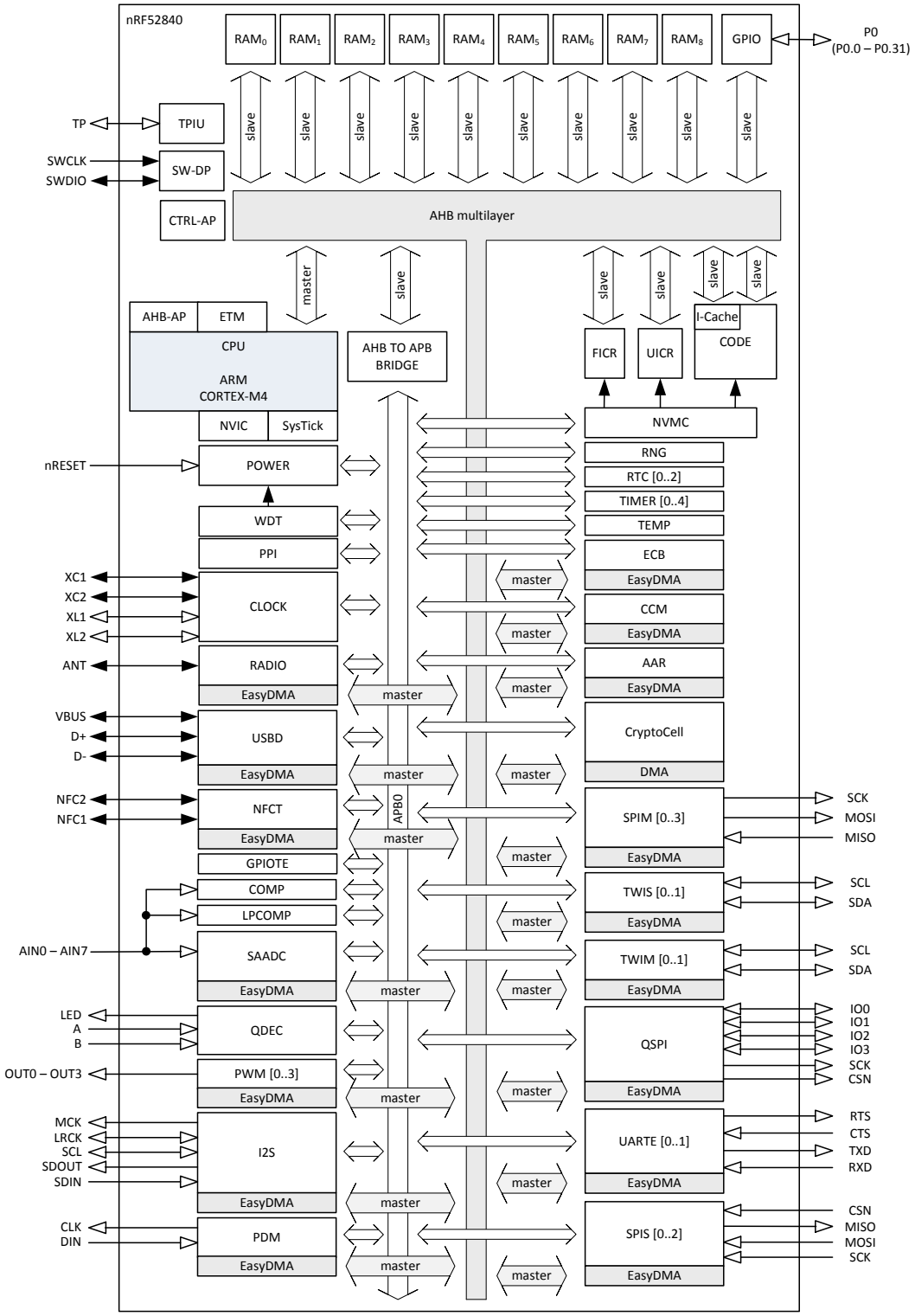

Figure 1: Block diagram

4 Pin assignments

This section describes the pin assignment and the pin functions.

This device provides flexibility when it comes to routing and configuration of the GPIO pins. However, some pins have recommendations for how the pin should be configured or what it should be used for. See *Table 3: QIAA pin assignments* on page 13 for more information about this.

4.1 QIAA pin assignments

This section describes the pin assignment and the pin functions.

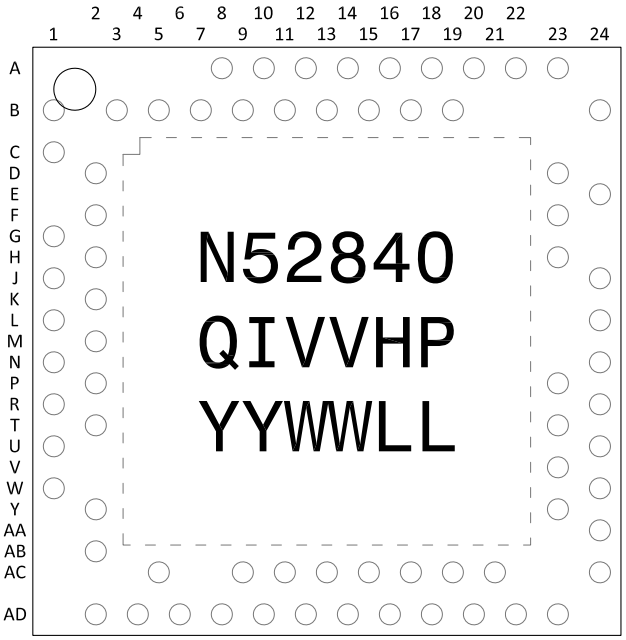

Figure 2: QIAA pin assignments, top view

Table 3: QIAA pin assignments

Pin	Name	Function	Description	Recommended usage
A8	P0.31	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
	AIN7	Analog input	Analog input	
A10	P0.29	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
	AIN5	Analog input	Analog input	
A12	P0.02	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
	AIN0	Analog input	Analog input	
A14	P1.15	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
A16	P1.13	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
A18	DEC2	Power	1.3 V regulator supply decoupling (Radio supply)	
A20	P1.10	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
A22	VDD	Power	Power supply	
A23	XC2	Analog input	Connection for 32 MHz crystal.	
B1	VDD	Power	Power supply	
B3	DCC	Power	DC/DC converter output	

Pin	Name	Function	Description	Recommended usage
B5	DEC4	Power	1.3 V regulator supply decoupling	
B7	VSS	Power	Ground	
B9	P0.30	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
	AIN6	Analog input	Analog input	
B11	P0.28	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
	AIN4	Analog input	Analog input	
B13	P0.03	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
	AIN1	Analog input	Analog input	
B15	P1.14	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
B17	P1.12	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
B19	P0.11	Digital I/O	General purpose I/O pin.	Standard drive, low frequency I/O only.
	TRACEDATA2	Trace data	Trace buffer TRACEDATA[2].	
B24	XC1	Analog input	Connection for 32 MHz crystal	
C1	DEC1	Power	1.1 V regulator supply decoupling	
D2	P0.00	Digital I/O	General purpose I/O	
	XL1	Analog input	Connection for 32.768 kHz crystal	
D23	DEC3	Power	Power supply, decoupling	
E24	DEC6	Power	1.3 V regulator supply decoupling (Radio supply)	
F2	P0.01	Digital I/O	General purpose I/O	
	XL2	Analog input	Connection for 32.768 kHz crystal	
F23	VSS_PA	Power	Ground (Radio supply)	
G1	P0.26	Digital I/O	General purpose I/O	
H2	P0.27	Digital I/O	General purpose I/O	
H23	ANT	RF	Single-ended radio antenna connection	See *Reference circuitry* on page 688 for guidelines on how to ensure good RF performance.
J1	P0.04	Digital I/O	General purpose I/O	
	AIN2	Analog input	Analog input	
J24	P0.10	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
	NFC2	NFC input	NFC antenna connection	
K2	P0.05	Digital I/O	General purpose I/O	
	AIN3	Analog input	Analog input	
L1	P0.06	Digital I/O	General purpose I/O	
L24	P0.09	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
	NFC1	NFC input	NFC antenna connection	
M2	P0.07	Digital I/O	General purpose I/O pin	
	TRACECLK	Trace clock	Trace buffer clock	
N1	P0.08	Digital I/O	General purpose I/O	
N24	DEC5	Power	1.3 V regulator supply decoupling (flash supply)	
P2	P1.08	Digital I/O	General purpose I/O	
P23	P1.07	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
R1	P1.09	Digital I/O	General purpose I/O pin.	
	TRACEDATA3	Trace data	Trace buffer TRACEDATA[3].	
R24	P1.06	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
T2	P0.11	Digital I/O	General purpose I/O	
T23	P1.05	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
U1	P0.12	Digital I/O	General purpose I/O pin.	
	TRACEDATA1	Trace data	Trace buffer TRACEDATA[1].	

Pin	Name	Function	Description	Recommended usage
U24	P1.04	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
V23	P1.03	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
W1	VDD	Power	Power supply	
W24	P1.02	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
Y2	VDDH	Power	High voltage power supply	
Y23	P1.01	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
AA24	SWDCLK	Debug	Serial wire debug clock input for debug and programming	
AB2	DCCH	Power	DC/DC converter output	
AC5	DECUSB	Power	Decoupling for USB 3.3 V	
AC9	P0.14	Digital I/O	General purpose I/O	
AC11	P0.16	Digital I/O	General purpose I/O	
AC13	P0.18 nRESET	Digital I/O	General purpose I/O Configurable as system RESET	QSPI/CSN
AC15	P0.19	Digital I/O	General purpose I/O	QSPI/SCK
AC17	P0.21	Digital I/O	General purpose I/O	QSPI
AC19	P0.23	Digital I/O	General purpose I/O	QSPI
AC21	P0.25	Digital I/O	General purpose I/O	
AC24	SWDIO	Debug	Debug serial data	
AD2	VBUS	Power	5 V input for USB 3.3 V regulator	
AD4	D-	Digital I/O	USB D-	USB
AD6	D+	Digital I/O	USB D+	USB
AD8	P0.13	Digital I/O	General purpose I/O	
AD10	P0.15	Digital I/O	General purpose I/O	
AD12	P0.17	Digital I/O	General purpose I/O	
AD14	VDD	Power	Power supply	
AD16	P0.20	Digital I/O	General purpose I/O	
AD18	P0.22	Digital I/O	General purpose I/O	QSPI
AD20	P0.24	Digital I/O	General purpose I/O	
AD22	P1.00 TRACEDATA0	Digital I/O Trace data	General purpose I/O pin. Trace buffer TRACEDATA[0]. Serial wire output (SWO).	QSPI
AD23	VDD	Power	Flash supply pad	
Bottom of chip				
Die pad	VSS	Power	Ground pad. Exposed die pad must be connected to ground (VSS) for proper device operation.	

Important: For more information on Standard drive, see *GPIO — General purpose input/output* on page 154. Low frequency I/O is signals with a frequency up to 10 kHz.

5 Absolute maximum ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

Table 4: Absolute maximum ratings

	Note	Min.	Max.	Unit
Supply voltages				
VDD		-0.3	+3.9	V
VDDH		-0.3	+5.8	V
VBUS		-0.3	+5.8	V
VSS			0	V
I/O pin voltage				
$V_{I/O}$, VDD ≤3.6 V		-0.3	VDD + 0.3 V	V
$V_{I/O}$, VDD >3.6 V		-0.3	3.9 V	V
NFC antenna pin current				
$I_{NFC1/2}$			80	mA
Radio				
RF input level			10	dBm
Environmental (AQFN package)				
Storage temperature		-40	+125	°C
MSL	Moisture Sensitivity Level		2	
ESD HBM	Human Body Model		4	kV
ESD CDM_{QF}	Charged Device Model (AQFN73, 7×7 mm package)		750	V
Flash memory				
Endurance		10 000		Write/erase cycles
Retention		10 years at 40°C		

6 Recommended operating conditions

The operating conditions are the physical parameters that the chip can operate within.

Table 5: Recommended operating conditions

Symbol	Parameter	Notes	Min.	Nom.	Max.	Units
VDD	VDD supply voltage, independent of DCDC enable		1.7	3.0	3.6	V
VDD_{POR}	VDD supply voltage needed during power-on reset		1.75			V
VDDH	VDDH supply voltage, independent of DCDC enable		2.5	3.7	5.5	V
VBUS	VBUS USB supply voltage		4.35	5	5.5	V
t_{R_VDD}	Supply rise time (0 V to 1.7 V)				60	ms
t_{R_VDDH}	Supply rise time (0 V to 3.7 V)				100	ms
TA	Operating temperature		-40	25	85	°C

Important: The on-chip power-on reset circuitry may not function properly for rise times longer than the specified maximum.

7 CPU

The ARM® Cortex®-M4 processor with floating-point unit (FPU) has a 32-bit instruction set (Thumb®-2 technology) that implements a superset of 16 and 32-bit instructions to maximize code density and performance.

This processor implements several features that enable energy-efficient arithmetic and high-performance signal processing, including:

- Digital signal processing (DSP) instructions
- Single-cycle multiply and accumulate (MAC) instructions
- Hardware divide
- 8- and 16-bit single instruction multiple data (SIMD) instructions
- Single-precision floating-point unit (FPU)

The ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM Cortex processor series is implemented and available for the M4 CPU.

Real-time execution is highly deterministic in thread mode, to and from sleep modes, and when handling events at configurable priority levels via the nested vectored interrupt controller (NVIC).

Executing code from flash will have a wait state penalty on the nRF52 series. An instruction cache can be enabled to minimize flash wait states when fetching instructions. For more information on cache, see *Cache* on page 29. The section *Electrical specification* on page 18 shows CPU performance parameters including wait states in different modes, CPU current and efficiency, and processing power and efficiency based on the CoreMark® benchmark.

The ARM System Timer (SysTick) is present on nRF52840. The SysTick's clock will only tick when the CPU is running or when the system is in debug interface mode.

7.1 Floating point interrupt

The floating point unit (FPU) may generate exceptions when used due to e.g. overflow or underflow, which in turn will trigger the FPU interrupt.

See *Instantiation* on page 23 for more information about the exceptions triggering the FPU interrupt.

To clear the IRQ (interrupt request) line when an exception has occurred, the relevant exception bit within the floating-point status and control register (FPSCR) needs to be cleared. For more information about the FPSCR or other FPU registers, see *Cortex-M4 Devices Generic User Guide*.

7.2 Electrical specification

7.2.1 CPU performance

The CPU clock speed is 64 MHz. Current and efficiency data is taken when in System ON and the CPU is executing the CoreMark™ benchmark. It includes power regulator and clock base currents. All other blocks are IDLE.

Symbol	Description	Min.	Typ.	Max.	Units
W_{FLASH}	CPU wait states, running CoreMark from flash, cache disabled			2	
$W_{FLASHCACHE}$	CPU wait states, running CoreMark from flash, cache enabled			3	
W_{RAM}	CPU wait states, running CoreMark from RAM			0	
$I_{DDFLASHCACHE}$	CPU current, running CoreMark from flash, cache enabled, LDO		6.5		mA
$I_{DDFLASHCACHEDCDC}$	CPU current, running CoreMark from flash, cache enabled, DCDC 3V		3.6		mA
$I_{DDFLASH}$	CPU current, running CoreMark from flash, cache disabled, LDO				mA

Symbol	Description	Min.	Typ.	Max.	Units
$I_{DDFLASHDCDC}$	CPU current, running CoreMark from flash, cache disabled, DCDC 3V				mA
I_{DDRAM}	CPU current, running CoreMark from RAM, LDO				mA
$I_{DDRAMDCDC}$	CPU current, running CoreMark from RAM, DCDC 3V				mA
$I_{DDFLASH/MHz}$	CPU efficiency, running CoreMark from flash, cache enabled, LDO		102		µA/MHz
$I_{DDFLASHDCDC/MHz}$	CPU efficiency, running CoreMark from flash, cache enabled, DCDC 3V		56		µA/MHz
CM_{FLASH}	CoreMark, running CoreMark from flash, cache enabled		212		CoreM
$CM_{FLASH/MHz}$	CoreMark per MHz, running CoreMark from flash, cache enabled		3.3		CoreM/MHz
$CM_{FLASH/mA}$	CoreMark per mA, running CoreMark from flash, cache enabled, DCDC 3V		59		CoreM/mA

7.3 CPU and support module configuration

The ARM® Cortex®-M4 processor has a number of CPU options and support modules implemented on the device.

Option / Module	Description	Implemented
Core options		
NVIC	Nested vector interrupt controller	37 vectors
PRIORITIES	Priority bits	3
WIC	Wakeup interrupt controller	NO
Endianness	Memory system endianness	Little endian
Bit-banding	Bit banded memory	NO
DWT	Data watchpoint and trace	YES
SysTick	System tick timer	YES
Modules		
MPU	Memory protection unit	YES
FPU	Floating-point unit	YES
DAP	Debug access port	YES
ETM	Embedded trace macrocell	YES
ITM	Instrumentation trace macrocell	YES
TPIU	Trace port interface unit	YES
ETB	Embedded trace buffer	NO
FPB	Flash patch and breakpoint unit	YES
HTM	AMBA™ AHB trace macrocell	NO

8 Memory

The nRF52840 contains 1 MB of flash and 256 kB of RAM that can be used for code and data storage.

The CPU and the peripherals having EasyDMA can access memory via the AHB multilayer interconnect.

The CPU is also able to access peripherals via the AHB multilayer interconnect, as illustrated in *Figure 3: Memory layout* on page 20.

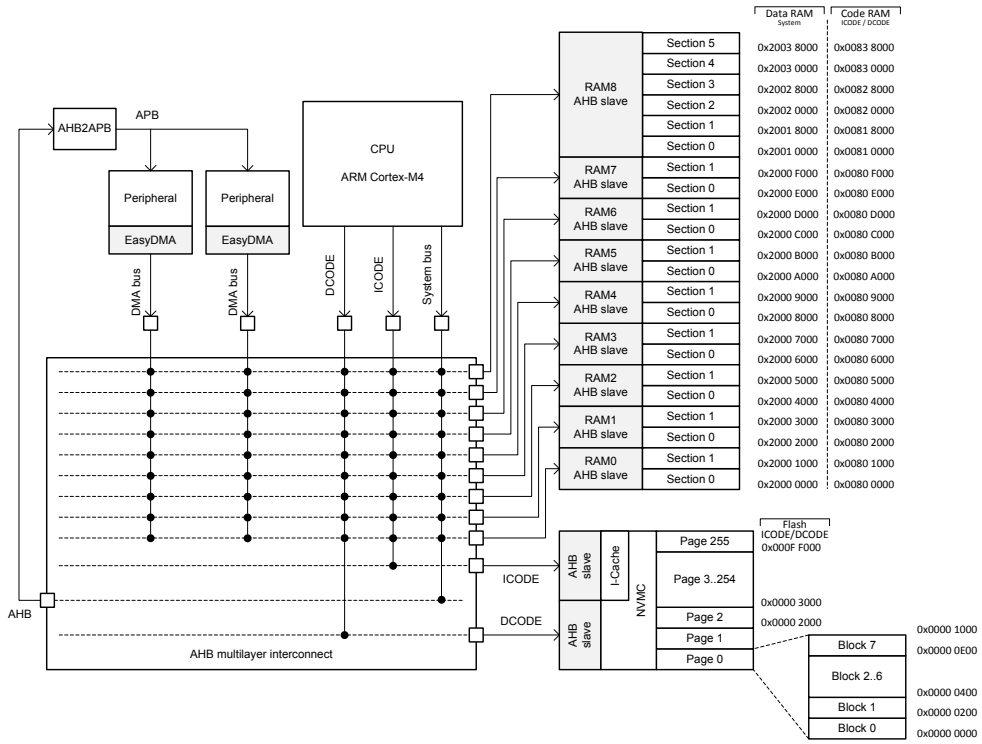

Figure 3: Memory layout

See *AHB multilayer* on page 25 and *EasyDMA* on page 26 for more information about the AHB multilayer interconnect and the EasyDMA.

The same physical RAM is mapped to both the Data RAM region and the Code RAM region. It is up to the application to partition the RAM within these regions so that one does not corrupt the other.

8.1 RAM - Random access memory

The RAM interface is divided into 9 RAM AHB slaves.

RAM AHB slave 0-7 is connected to 2x4 kB RAM sections each and RAM AHB slave 8 is connected to 6x32 kB sections, as shown in *Figure 3: Memory layout* on page 20.

Each of the RAM sections have separate power control for System ON and System OFF mode operation, which is configured via RAM register (see the *POWER — Power supply* on page 66).

8.2 Flash - Non-volatile memory

The flash can be read an unlimited number of times by the CPU, but it has restrictions on the number of times it can be written and erased and also on how it can be written.

Writing to flash is managed by the non-volatile memory controller (NVMC), see *NVMC — Non-volatile memory controller* on page 28.

The flash is divided into 256x4 kB pages that can be accessed by the CPU via both the ICODE and DCODE buses as shown in *Figure 3: Memory layout* on page 20. Each page is divided into 8 blocks.

8.3 Memory map

The complete memory map is shown in *Figure 4: Memory map* on page 22. As described in *Memory* on page 20, Code RAM and the Data RAM are the same physical RAM.

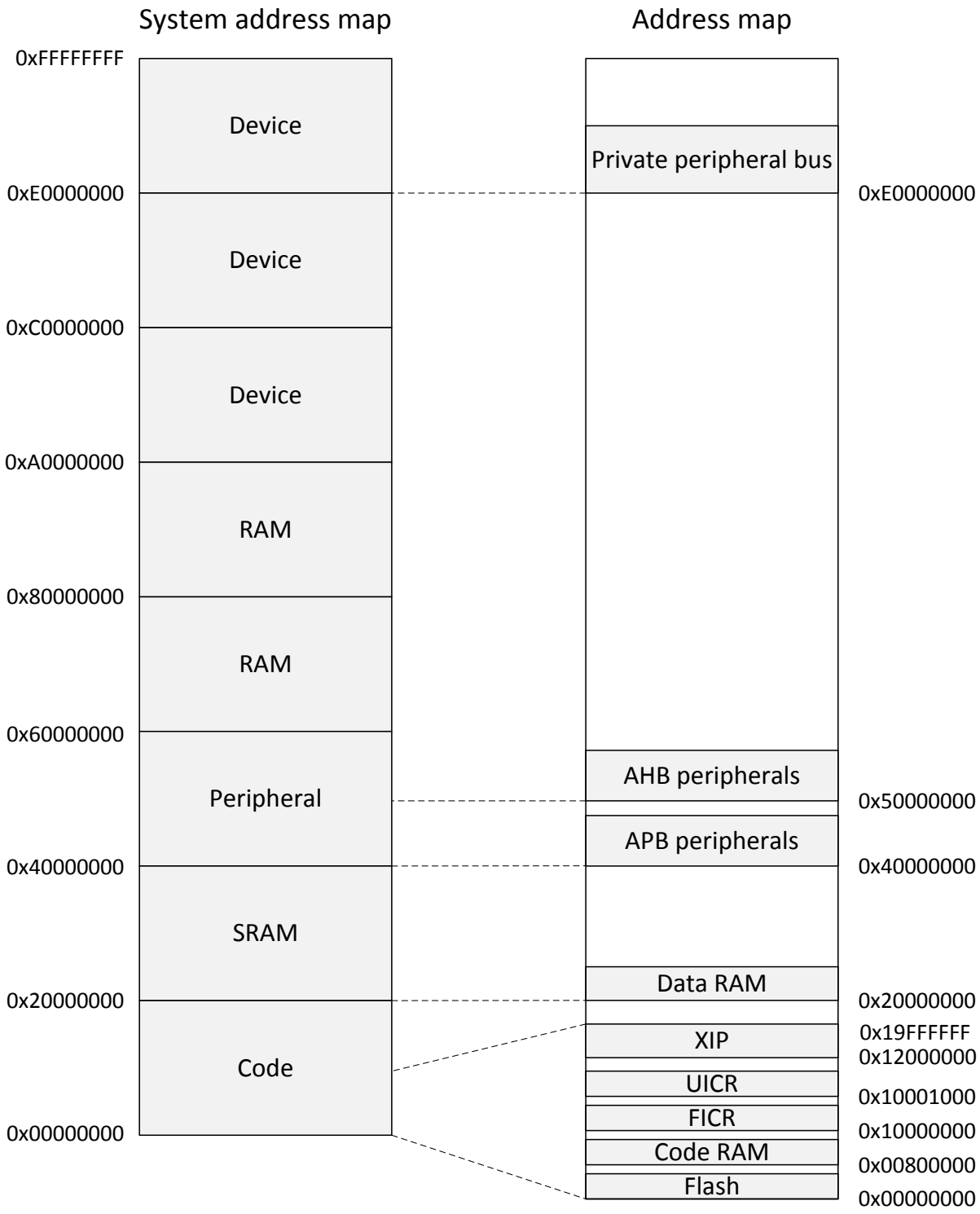

Figure 4: Memory map

8.4 Instantiation

Table 6: Instantiation table

ID	Base Address	Peripheral	Instance	Description	
0	0x40000000	CLOCK	CLOCK	Clock control	
0	0x40000000	POWER	POWER	Power control	
1	0x40001000	RADIO	RADIO	2.4 GHz radio	
2	0x40002000	UARTE	UARTE0	Universal asynchronous receiver/transmitter with EasyDMA, unit 0	
2	0x40002000	UART	UART0	Universal asynchronous receiver/transmitter	Deprecated
3	0x40003000	TWIM	TWIM0	Two-wire interface master 0	
3	0x40003000	SPIS	SPIS0	SPI slave 0	
3	0x40003000	SPIM	SPIM0	SPI master 0	
3	0x40003000	SPI	SPI0	SPI master 0	Deprecated
3	0x40003000	TWIS	TWIS0	Two-wire interface slave 0	
3	0x40003000	TWI	TWI0	Two-wire interface master 0	Deprecated
4	0x40004000	TWIS	TWIS1	Two-wire interface slave 1	
4	0x40004000	SPIS	SPIS1	SPI slave 1	
4	0x40004000	SPIM	SPIM1	SPI master 1	
4	0x40004000	TWI	TWI1	Two-wire interface master 1	Deprecated
4	0x40004000	TWIM	TWIM1	Two-wire interface master 1	
4	0x40004000	SPI	SPI1	SPI master 1	Deprecated
5	0x40005000	NFCT	NFCT	Near field communication tag	
6	0x40006000	GPIOTE	GPIOTE	GPIO tasks and events	
7	0x40007000	SAADC	SAADC	Analog to digital converter	
8	0x40008000	TIMER	TIMER0	Timer 0	
9	0x40009000	TIMER	TIMER1	Timer 1	
10	0x4000A000	TIMER	TIMER2	Timer 2	
11	0x4000B000	RTC	RTC0	Real-time counter 0	
12	0x4000C000	TEMP	TEMP	Temperature sensor	
13	0x4000D000	RNG	RNG	Random number generator	
14	0x4000E000	ECB	ECB	AES electronic code book (ECB) mode block encryption	
15	0x4000F000	AAR	AAR	Accelerated address resolver	
15	0x4000F000	CCM	CCM	AES counter with CBC-MAC (CCM) mode block encryption	
16	0x40010000	WDT	WDT	Watchdog timer	
17	0x40011000	RTC	RTC1	Real-time counter 1	
18	0x40012000	QDEC	QDEC	Quadrature decoder	
19	0x40013000	LPCOMP	LPCOMP	Low power comparator	
19	0x40013000	COMP	COMP	General purpose comparator	
20	0x40014000	EGU	EGU0	Event generator unit 0	
20	0x40014000	SWI	SWI0	Software interrupt 0	
21	0x40015000	EGU	EGU1	Event generator unit 1	
21	0x40015000	SWI	SWI1	Software interrupt 1	
22	0x40016000	EGU	EGU2	Event generator unit 2	
22	0x40016000	SWI	SWI2	Software interrupt 2	
23	0x40017000	EGU	EGU3	Event generator unit 3	
23	0x40017000	SWI	SWI3	Software interrupt 3	
24	0x40018000	SWI	SWI4	Software interrupt 4	
24	0x40018000	EGU	EGU4	Event generator unit 4	
25	0x40019000	SWI	SWI5	Software interrupt 5	
25	0x40019000	EGU	EGU5	Event generator unit 5	
26	0x4001A000	TIMER	TIMER3	Timer 3	
27	0x4001B000	TIMER	TIMER4	Timer 4	
28	0x4001C000	PWM	PWM0	Pulse width modulation unit 0	
29	0x4001D000	PDM	PDM	Pulse Density modulation (digital microphone) interface	
30	0x4001E000	ACL	ACL	Access control lists	
30	0x4001E000	NVMC	NVMC	Non-volatile memory controller	

ID	Base Address	Peripheral	Instance	Description	
31	0x4001F000	PPI	PPI	Programmable peripheral interconnect	
32	0x40020000	MWU	MWU	Memory watch unit	
33	0x40021000	PWM	PWM1	Pulse width modulation unit 1	
34	0x40022000	PWM	PWM2	Pulse width modulation unit 2	
35	0x40023000	SPIM	SPIM2	SPI master 2	
35	0x40023000	SPIS	SPIS2	SPI slave 2	
35	0x40023000	SPI	SPI2	SPI master 2	Deprecated
36	0x40024000	RTC	RTC2	Real-time counter 2	
37	0x40025000	I2S	I2S	Inter-IC sound interface	
38	0x40026000	FPU	FPU	FPU interrupt	
39	0x40027000	USBD	USBD	Universal serial bus device	
40	0x40028000	UARTE	UARTE1	Universal asynchronous receiver/transmitter with EasyDMA, unit 1	
41	0x40029000	QSPI	QSPI	External memory interface	
45	0x4002D000	PWM	PWM3	Pulse width modulation unit 3	
47	0x4002F000	SPIM	SPIM3	SPI master 3	
0	0x50000000	GPIO	GPIO	General purpose input and output	Deprecated
0	0x50000000	GPIO	P0	General purpose input and output, port 0	
0	0x50000300	GPIO	P1	General purpose input and output, port 1	
42	0x5002A000	CRYPTOCELL	CRYPTOCELL	CryptoCell subsystem control interface	
N/A	0x10000000	FICR	FICR	Factory information configuration	
N/A	0x10001000	UICR	UICR	User information configuration	

9 AHB multilayer

AHB multilayer enables parallel access paths between multiple masters and slaves in a system. Access is resolved using priorities.

Each bus master is connected to the slave devices using an interconnection matrix. The bus masters are assigned priorities. Priorities are used to resolve access when two (or more) bus masters request access to the same slave device. The following applies:

- If two (or more) bus masters request access to the same slave device, the master with the highest priority is granted the access first.
- Bus masters with lower priority are stalled until the higher priority master has completed its transaction.
- If the higher priority master pauses at any point during its transaction, the lower priority master in queue is temporarily granted access to the slave device until the higher priority master resumes its activity.
- Bus masters that have the same priority are mutually exclusive, thus cannot be used concurrently.

Below is a list of bus masters in the system and their priorities.

Table 7: AHB bus masters (listed in priority order, highest to lowest)

Bus master name	Description
CPU	
CTRL-AP	
USB	
CRYPTOCELL	
SPIM1/SPIS1/TWIM1/TWIS1	Same priority and mutually exclusive
RADIO	
CCM/ECB/AAR	Same priority and mutually exclusive
SAADC	
UARTE0	
SPIM0/SPIS0/TWIM0/TWIS0	Same priority and mutually exclusive
SPIM2/SPIS2	Same priority and mutually exclusive
NFCT	
I2S	
PDM	
PWM0	
PWM1	
PWM2	
QSPI	
PWM3	
UARTE1	
SPIM3	

Defined bus masters are the CPU and the peripherals with implemented EasyDMA, and the available slaves are RAM AHB slaves. How the bus masters and slaves are connected using the interconnection matrix is illustrated in *Memory* on page 20.