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nRF905

Single chip 433/868/915MHz Transceiver

Product Specification

Key Features

- True single chip GFSK transceiver in a small 32 pin package (32L QFN 5x5mm)
- ShockBurst™ mode for low power operation
- Power supply range 1.9 to 3.6 V
- Multi channel operation – ETSI/FCC Compatible
- Channel switching time <650µs
- Extremely low cost Bill of Material (BOM)
- No external SAW filter
- Adjustable output power up to 10dBm
- Carrier detect for "listen before transmit" protocols
- Data Ready signal when a valid data packet is received or transmitted
- Address Match for detection of incoming packet
- Automatic retransmission of data packet
- Automatic CRC and preamble generation
- Low supply current (TX), typical 9mA @ -10dBm output power
- Low supply current (RX), typical 12.5mA

Applications

- Wireless data communication
- Alarm and security system
- Home automation
- Remote control
- Surveillance
- Automotive
- Telemetry
- Keyless entry
- Toys

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Objective product specification	This product specification contains target specifications for product development.
Preliminary product specification	This product specification contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
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Writing conventions

This product specification follows a set of typographic rules that makes the document consistent and easy to read. The following writing conventions are used:

- Commands, bit state conditions, and register names are written in *Courier*.
- Pin names and pin signal conditions are written in *Courier bold*.
- Cross references are [underlined and highlighted in blue](#).

Revision history

Date	Version	Description
June 2006	1.4	
April 2008	1.5	<ul style="list-style-type: none">• Restructured layout in the new template• Updated package information• Added moisture sensitivity level to the absolute maximum ratings

Attention!

Observe precaution for handling
Electrostatic Sensitive Device.



Datasheet order code: 051005nRF905

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1 Introduction

nRF905 is a single chip radio transceiver for the 433/868/915MHz ISM band. The transceiver consists of a fully integrated frequency synthesizer, receiver chain with demodulator, a power amplifier, a crystal oscillator and, a modulator. The ShockBurst™ feature automatically handles preamble and CRC. You can easily configure the nRF905 through the SPI. Current consumption is very low, in transmit only 9mA at an output power of -10dBm, and in receive mode 12.5mA. Built-in power down modes makes power saving easily realizable.

2 Quick reference data

Parameter	Value	Unit
Minimum supply voltage	1.9	V
Maximum transmit output power	10	dBm
Data rate	50	kbps
Supply current in transmit @ -10dBm output power	9	mA
Supply current in receive mode	12.5	mA
Temperature range	-40 to +85	°C
Typical sensitivity	-100	dBm
Supply current in power down mode	2.5	μA

Table 1. nRF905 quick reference data.

3 Block Diagram

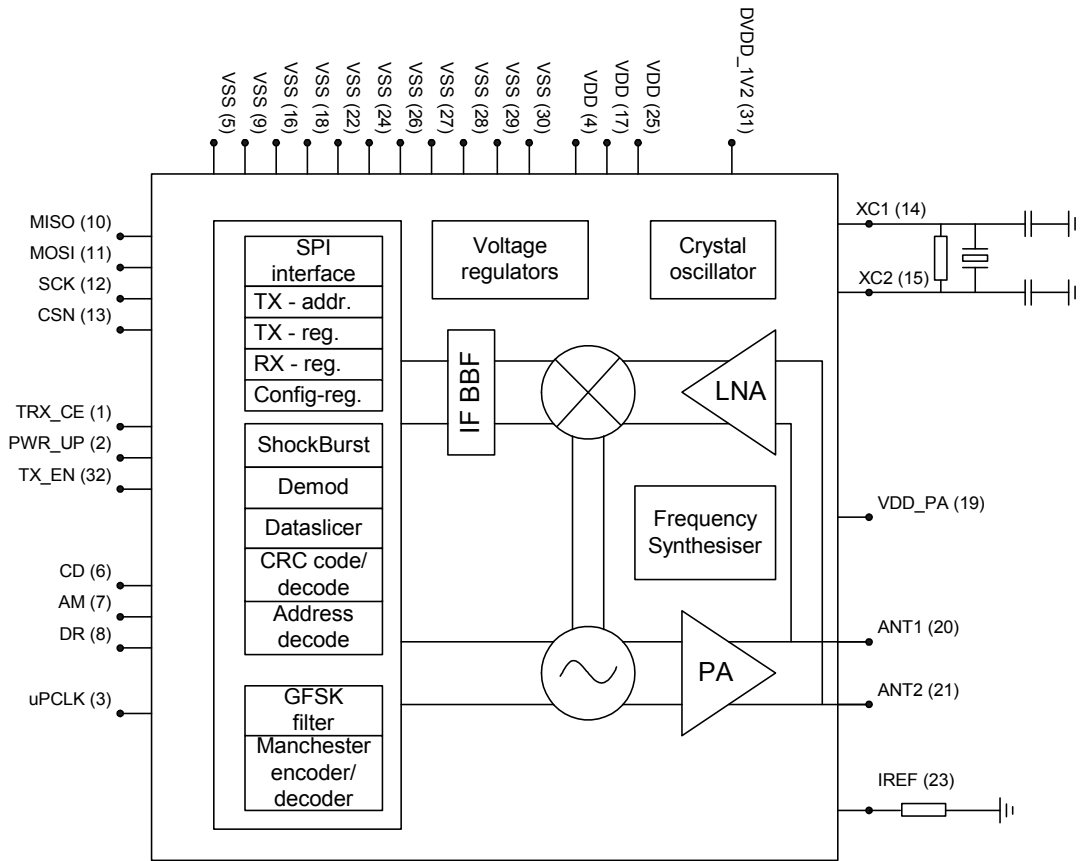


Figure 1. nRF905 with external components.

4 Absolute maximum ratings

Operating conditions	Minimum	Maximum	Units
Supply voltages			
VDD	-0.3	+3.6	V
VSS		0	V
Input voltage			
V_I	-0.3	VDD +0.3	V
Output voltage			
V_O	-0.3	VDD +0.3	V
Total power dissipation			
$P_D (T_A=85^\circ\text{C})$		200	mW
Temperatures			
Operating temperature	-40	+85	$^\circ\text{C}$
Storage temperature	-40	+125	$^\circ\text{C}$
Moisture sensitivity level			
		260	$^\circ\text{C}$

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Table 2. Absolute maximum ratings

5 Electrical Specifications

Conditions: VDD = +3V VSS = 0V, TEMP = -40°C to +85°C (typical +27°C)

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
VDD	Supply voltage		1.9		3.6	V
TEMP	Operating temperature		-40		85	°C

Table 3. Operating conditions

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
V _{IH}	HIGH level input voltage		0.7·VDD		VDD	V
V _{IL}	LOW level input voltage		VSS		0.3·VDD	V
C _i	Pin capacitance				5	pF
I _{iL}	Pin leakage current	a			±10	nA
V _{OH}	HIGH level output voltage (I _{OH} =-0.5mA)		VDD-0.3		VDD	V
V _{OL}	LOW level output voltage (I _{OL} =0.5mA)		VSS		0.3	V

a. Max value determined by design and characterization testing.

Table 4. Digital input/output

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
I _{stby_eclk}	Supply current in standby, uCLK enabled	a		100		μA
I _{stby_dclk}	Supply current in standby, uCLK disabled	b		12.5		μA
I _{PD}	Supply current in power down mode	c		2.5		μA
I _{SPI}	Supply current in SPI programming	d		20		μA

- a. Output frequency is 4MHz load of external clock pin is 5pF, Crystal is 4MHz.
- b. Crystal is 4MHz.
- c. Pin voltages are VSS or VDD.
- d. Chip in power down, SPI_SCK frequency is 1MHz.

Table 5. Electrical specifications

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
f_{OP}	Operating frequency	a	430		928	MHz
f_{XTAL}	Crystal frequency	b	4		20	MHz
Δf	Frequency deviation		± 42	± 50	± 58	kHz
BR	Data rate	c		50		kbps
f_{CH433}	Channel spacing for 433MHz band			100		kHz
$f_{CH868/915}$	Channel spacing for 868/915MHz band			200		kHz

- a. Operates in the 433, 868 and 915MHz ISM band.
b. The crystal frequency may be chosen from 5 different values (4, 8, 12, 16, and 20MHz).
c. Data is Manchester encoded before GFSK modulation.

Table 6. General RF conditions

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
P_{RF10}	Output power 10dBm setting	a	7	10	11	dBm
P_{RF6}	Output power 6dBm setting	a	3	6	9	dBm
P_{RF-2}	Output power -2dBm setting	a	-6	-2	2	dBm
P_{RF-10}	Output power -10dBm setting	a	-14	-10	-6	dBm
$P_{BW_{-16}}$	-16dBc bandwidth for modulated carrier	b		173		kHz
$P_{BW_{-24}}$	-24dBc bandwidth for modulated carrier	b		222		kHz
$P_{BW_{-32}}$	-32dBc bandwidth for modulated carrier	b		238		kHz
$P_{BW_{-36}}$	-36dBc bandwidth for modulated carrier	b		313		kHz
P_{RF1}	1 st adjacent channel transmit power	c		-27		dBc
P_{RF2}	2 nd adjacent channel transmit power	c		-54		dBc
$I_{TX10dBm}$	Supply current @ 10dBm output power			30		mA
$I_{TX-10dBm}$	Supply current @ -10dBm output power			9		mA

- a. Optimum load impedance, please see peripheral RF information.
b. Data is Manchester encoded before GFSK modulation.
c. Channel width and channel spacing is 200kHz.

Table 7. Transmitter operation

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
I_{RX}	Supply current in receive mode			12.5		mA
RX_{SENS}	Sensitivity at 0.1%BER			-100		dBm
RX_{MAX}	Maximum received signal		0			dBm
C/I_{CO}	C/I Co-channel	a		13		dB
C/I_{1ST}	1 st adjacent channel selectivity C/I 200kHz	a		-7		dB
C/I_{2ND}	2 nd adjacent channel selectivity C/I 400kHz	a		-16		dB
C/I_{+1M}	Blocking at +1MHz	a		-40		dB
C/I_{-1M}	Blocking at -1MHz	a		-50		dB
C/I_{-2M}	Blocking at -2MHz	a		-63		dB

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
C/I _{+5M}	Blocking at +5MHz	a		-70		dB
C/I _{-5M}	Blocking at -5MHz	a		-65		dB
C/I _{+10M}	Blocking at +10MHz	a		-69		dB
C/I _{-10M}	Blocking at -10MHz	a		-67		dB
C/I _{IM}	Image rejection	a		-36		dB

a. Channel Level +3dB over sensitivity, interfering signal a standard CW, image lies 2MHz above wanted.

Table 8. Receiver operation

6 Current Consumption

Mode	Crystal freq. (MHz)	Output clock Freq. (MHz)	Typical current
Power Down	16	OFF	2.5uA
Standby	4	OFF	12uA
Standby	8	OFF	25uA
Standby	12	OFF	27uA
Standby	16	OFF	32uA
Standby	20	OFF	46uA
Standby	4	0.5	110uA
Standby	8	0.5	125uA
Standby	12	0.5	130uA
Standby	16	0.5	135uA
Standby	20	0.5	150uA
Standby	4	1	130uA
Standby	8	1	145uA
Standby	12	1	150uA
Standby	16	1	155uA
Standby	20	1	170uA
Standby	4	2	170uA
Standby	8	2	185uA
Standby	12	2	190uA
Standby	16	2	195uA
Standby	20	2	210uA
Standby	4	4	260uA
Standby	8	4	275uA
Standby	12	4	280uA
Standby	16	4	285uA
Standby	20	4	300uA
Rx @ 433	16	OFF	12.2mA
Rx @ 868/915	16	OFF	12.8mA
Reduced Rx	16	OFF	10.5mA
Tx @ 10dBm	16	OFF	30mA
Tx @ 6dBm	16	OFF	20mA
Tx @ -2dBm	16	OFF	14mA
Tx @ -10dBm	16	OFF	9mA
Conditions: VDD = 3.0V, VSS = 0V, T _A = 27°C, Load capacitance of external clock = 13pF, Crystal load capacitance = 12pF			

Table 9. nRF905 current consumption

7 Pin information

7.1 Pin Assignment

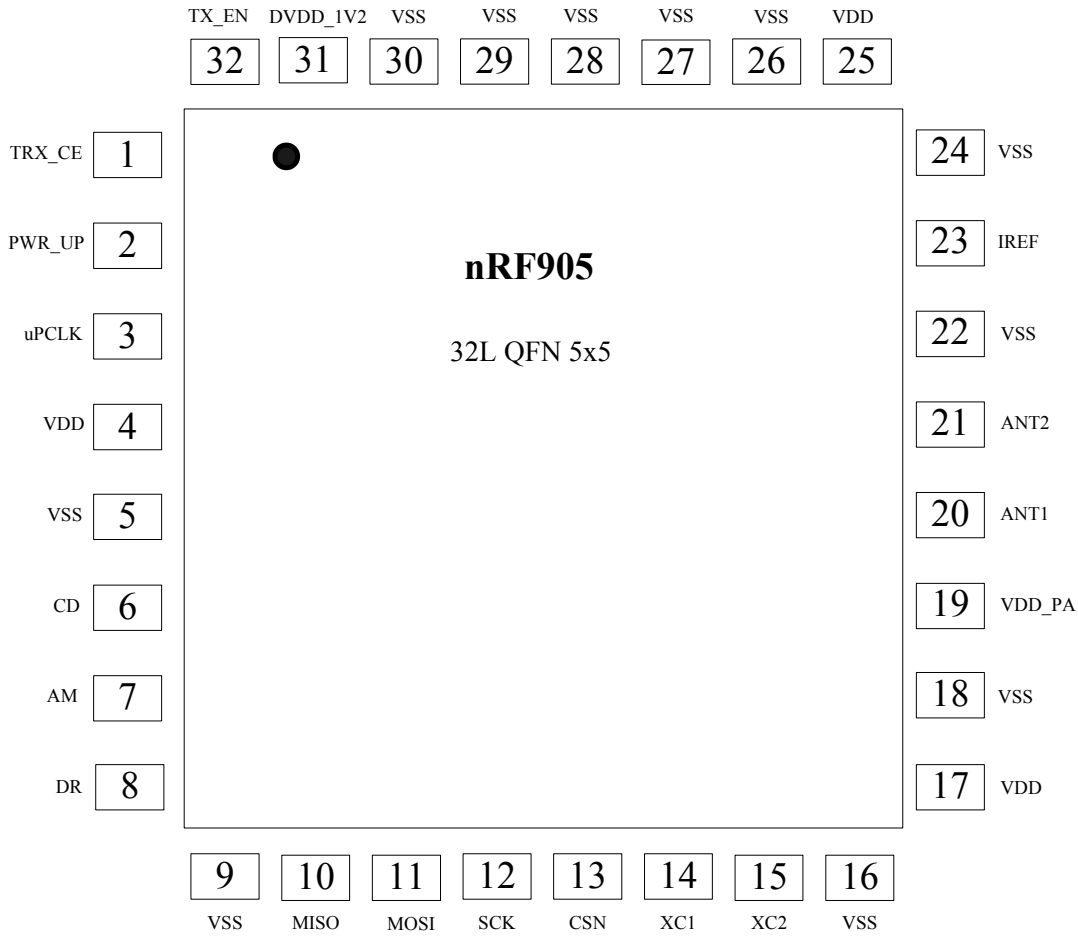


Figure 2. nRF905 pin assignment (top view) for a 32L QFN 5x5 package

7.2 Pin Functions

Pin	Name	Pin function	Description
1	TRX_CE	Digital input	Enables chip for receive and transmit
2	PWR_UP	Digital input	Power up chip
3	uPCLK	Clock output	Output clock, divided crystal oscillator full swing clock
4	VDD	Power	Power supply (+3V DC)
5	VSS	Power	Ground (0V)
6	CD	Digital output	Carrier Detect
7	AM	Digital output	Address Match
8	DR	Digital output	Receive and transmit Data Ready
9	VSS	Power	Ground (0V)
10	MISO	SPI - interface	SPI output
11	MOSI	SPI - interface	SPI input
12	SCK	SPI - Clock	SPI clock
13	CSN	SPI - enable	SPI enable, active low
14	XC1	Analog Input	Crystal pin 1/ External clock reference pin
15	XC2	Analog Output	Crystal pin 2
16	VSS	Power	Ground (0V)
17	VDD	Power	Power supply (+3V DC)
18	VSS	Power	Ground
19	VDD_PA	Power output	Positive supply (1.8V) to nRF905 power amplifier
20	ANT1	RF	Antenna interface 1
21	ANT2	RF	Antenna interface 2
22	VSS	Power	Ground (0V)
23	IREF	Analog Input	Reference current
24	VSS	Power	Ground (0V)
25	VDD	Power	Power supply (+3V DC)
26	VSS	Power	Ground (0V)
27	VSS	Power	Ground (0V)
28	VSS	Power	Ground (0V)
29	VSS	Power	Ground (0V)
30	VSS	Power	Ground (0V)
31	DVDD_1V2	Power	Low voltage positive digital supply output for decoupling
32	TX_EN	Digital input	TX_EN="1"TX mode, TX_EN="0"RX mode

Table 10. nRF905 pin function.

8 Modes of Operation

The nRF905 has two active (RX/TX) modes and two power saving modes:

8.1 Active Modes

- ShockBurst™ RX
- ShockBurst™ TX

8.2 Power Saving Modes

- Power down and SPI programming
- Standby and SPI programming

The nRF905 mode is decided by the settings of TRX_CE, TX_EN and PWR_UP.

PWR_UP	TRX_CE	TX_EN	Operating Mode
0	X	X	Power down and SPI programming
1	0	X	Standby and SPI programming
1	X	0	Read data from RX register
1	1	0	Radio Enabled - ShockBurst™ RX
1	1	1	Radio Enabled - ShockBurst™ TX

Table 11. nRF905 operational modes.

8.3 nRF ShockBurst™ Mode

The nRF905 uses the ShockBurst™ feature. ShockBurst™ makes it possible to use the high data rate offered by the nRF905 without the need of a costly, high-speed microcontroller (MCU) for data processing/clock recovery. By placing all high speed signal processing related to RF protocol on-chip, the nRF905 offers the application microcontroller a simple SPI, the data rate is decided by the interface speed the microcontroller sets up. By allowing the digital part of the application to run at low speed, while maximizing the data rate on the RF link, the nRF905 ShockBurst™ mode reduces the average current consumption in applications. In ShockBurst™ RX, Address Match (AM) and Data Ready (DR) notifies the MCU when a valid address and payload is received respectively. In ShockBurst™ TX, the nRF905 automatically generates preamble and CRC. Data Ready (DR) notifies the MCU that the transmission is completed. This means reduced memory demand in the MCU resulting in a low cost MCU, as well as reduced software development time.

8.4 Typical ShockBurst™ TX

1. When the application MCU has data for a remote node, the address of the receiving node (TX-address) and payload data (TX-payload) are clocked into nRF905 through the SPI. The application protocol or MCU sets the speed of the interface.
2. MCU sets TRX_CE and TX_EN high, this activates a nRF905 ShockBurst™ transmission.
3. nRF905 ShockBurst™ does the following:
 - ▶ Radio is automatically powered up.
 - ▶ Data packet is completed (preamble added, CRC calculated).
 - ▶ Data packet is transmitted (50kbps).
 - ▶ Data Ready is set high when transmission is completed.

4. If AUTO_RETRAN is set high, the nRF905 continuously retransmits the packet until TRX_CE is set low.
5. When TRX_CE is set low, the nRF905 finishes transmitting the outgoing packet and then sets itself into standby mode.

If TX_EN is set low while TRX_CE is kept high, the nRF905 finishes transmitting the outgoing packet and enters RX mode in the channel already programmed in the RF-CONFIG register.

The ShockBurst™ mode ensures that a transmitted packet that has started always finishes regardless of what TRX_EN and TX_EN are set to during transmission. The new mode is activated when the transmission is completed.

For test purposes such as antenna tuning and measuring output power it is possible to set the transmitter so that a constant carrier is produced. To do this, TRX_CE must be maintained high instead of being pulsed and Auto Retransmit should be switched off. After the burst of data is sent the device continues to send the unmodulated carrier.

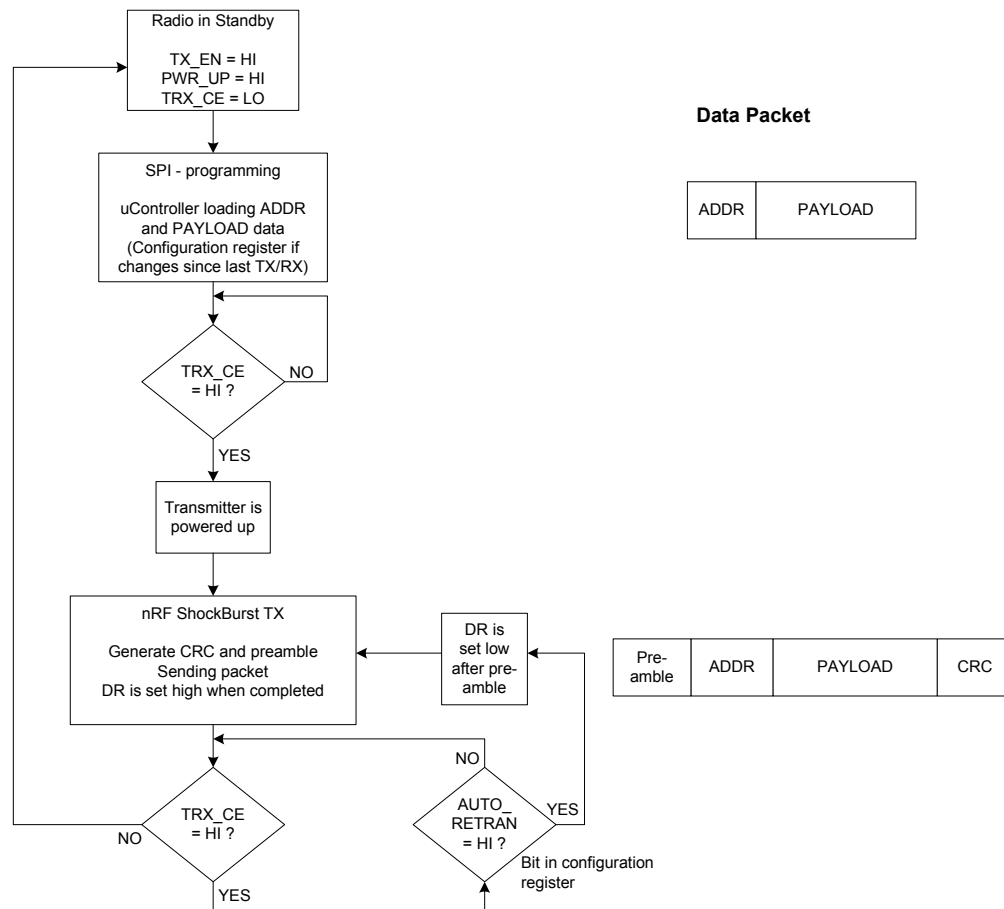


Figure 3. Flowchart ShockBurst™ transmit of nRF905.

Note: When DR is set high it can be set low again under the following conditions:

- If TX_EN is set low
- If PWR_UP is set low

8.5 Typical ShockBurst™ RX

1. ShockBurst™ RX is selected by setting TRX_CE high and TX_EN low.
2. After 650µs nRF905 is monitoring the air for incoming communication.
3. When the nRF905 senses a carrier at the receiving frequency, Carrier Detect (CD) pin is set high.
4. When a valid address is received, Address Match (AM) pin is set high.
5. When a valid packet has been received (correct CRC found), nRF905 removes the preamble, address and CRC bits, and the Data Ready (DR) pin is set high.
6. MCU sets the TRX_CE low to enter standby mode (low current mode).
7. MCU can clock out the payload data at a suitable rate through the SPI.
8. When all payload data is retrieved, nRF905 sets Data Ready (DR) and Address Match (AM) low again.
9. The chip is now ready for entering ShockBurst™ RX, ShockBurst™ TX or, power down mode.

If TX_EN is set high while TRX_CE is kept high, the nRF905 would enter ShockBurst™ TX and start a transmission according to the present contents in the SPI registers.

If TRX_CE or TX_EN is changed during an incoming packet, the nRF905 changes mode immediately and the packet is lost. However, if the MCU is sensing the Address Match (AM) pin, it knows when the chip is receiving an incoming packet and can therefore decide whether to wait for the Data Ready (DR) signal or enter a different mode.

To avoid spurious address matches it is recommended that the address length be 24 bits or higher in length. Small addresses such as 8 or 16 bits can often lead to statistical failures due to the address being repeated as part of the data packet. This can be avoided by using a longer address.

Each byte within the address should be unique. Repeating bytes within the address reduces the effectiveness of the address and increases its susceptibility to noise which increases the packet error rate. The address should also have several level shifts (that is, 10101100) reducing the statistical effect of noise and the packet error rate.

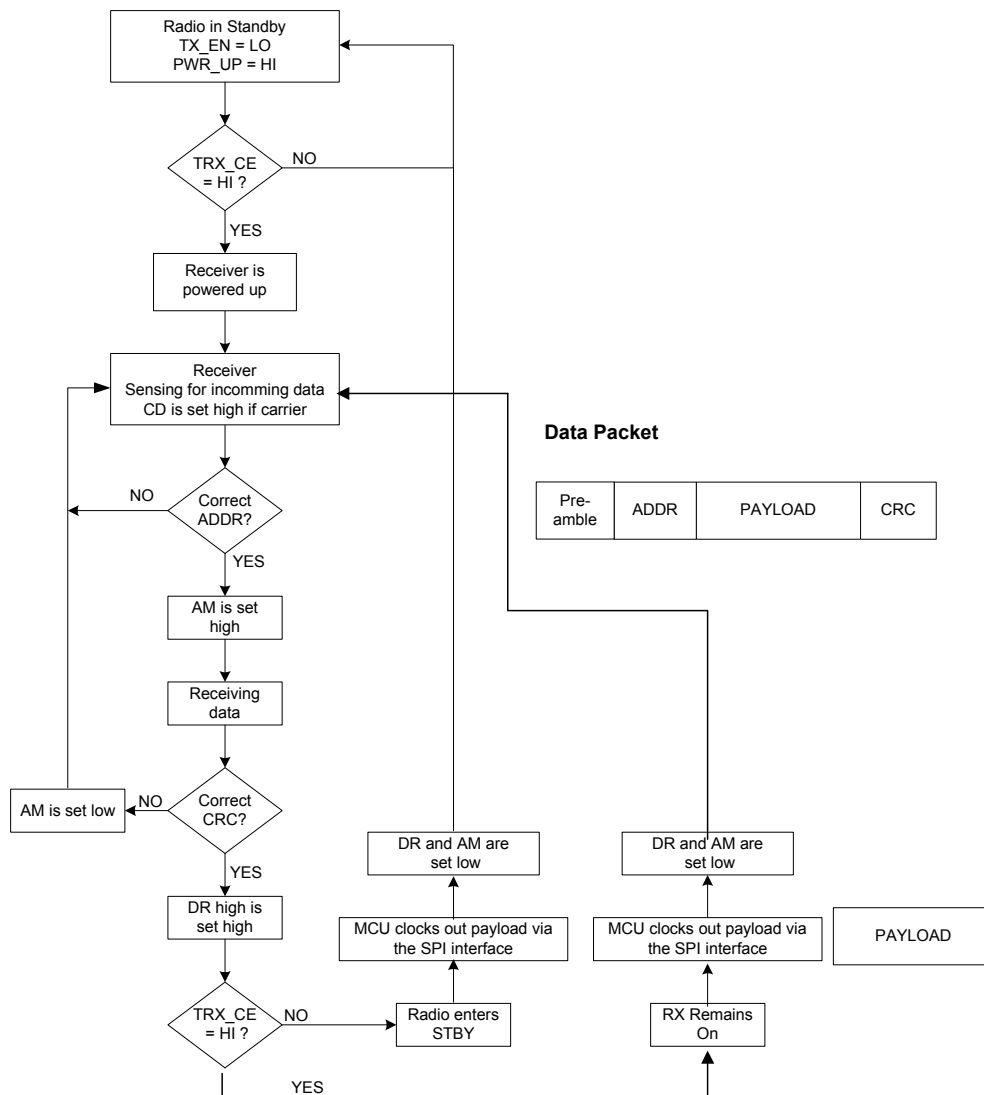


Figure 4. Flowchart ShockBurst™ receive of nRF905.

8.6 Power Down Mode

In power down the nRF905 is disabled with minimal current consumption, typically less than 2.5µA. When the device enters this mode it is not active which minimizes average current consumption and maximizes battery lifetime. The configuration word content is maintained during power down.

8.7 Standby Mode

Standby mode is used to minimize average current consumption while maintaining short start up times to ShockBurst™ RX and ShockBurst™ TX. In this mode part of the crystal oscillator is active. Current consumption is dependent on crystal frequency, Ex: $I_{DD} = 12\mu A @ 4MHz$ and $I_{DD} = 46\mu A @ 20MHz$. If the uP-clock (pin 3) of nRF905 is enabled, current consumption increases and is dependent on the load capacitance and frequency. The configuration word content is maintained during standby.

9 Device Configuration

All configuration of the nRF905 is through the SPI. The interface consists of five registers. A SPI instruction set is used to decide which operation shall be performed. The SPI can be activated in any mode however, we recommend that the chip is in standby or power down mode.

9.1 SPI Register Configuration

The SPI consists of five internal registers. A register readback mode is implemented to allow verification of the register contents.

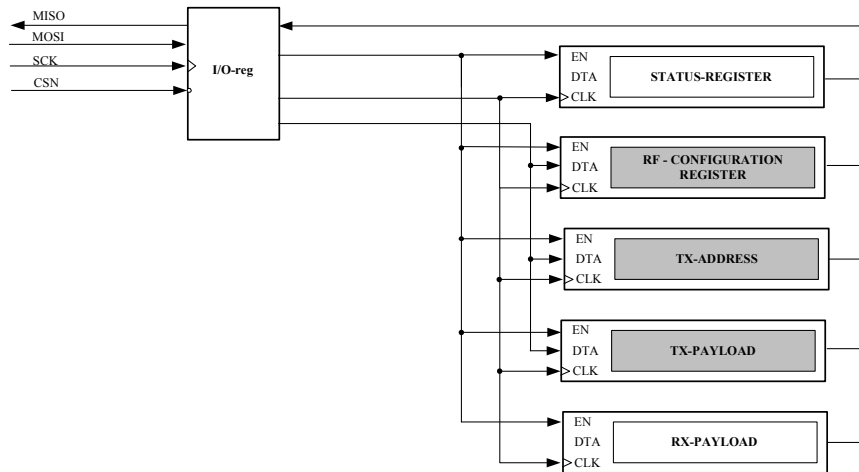


Figure 5. SPI – interface and the five internal registers.

Internal registers	Description
Status – Register	Register contains status of Data Ready (DR), Address Match (AM).
RF – Configuration Register	Register contains transceiver setup information such as frequency and output power ext.
TX – Address	Register contains address of target device. How many bytes used is set in the configuration register.
TX – Payload	Register containing the payload information to be sent in a Shock-Burst™ packet. How many bytes used is set in the configuration register.
RX – Payload	Register containing the payload information derived from a received valid ShockBurst™ packet. How many bytes used is set in the configuration register. Valid data in the RX-Payload register is indicated with a high Date Ready (DR) signal.

Table 12. Internal registers description

9.2 SPI Instruction Set

The available commands used on the SPI are shown below. Whenever CSN is set low the interface expects an instruction. Every new instruction must be started by a high to low transition on CSN.

Instruction set for the nRF905 SPI		
Instruction Name	Instruction Format	Operation
W_CONFIG (WC)	0000 AAAA	Write Configuration register. AAAA indicates which byte the write operation is to be started from. Number of bytes depends on start address AAAA.
R_CONFIG (RC)	0001 AAAA	Read Configuration register. AAAA indicates which byte the read operation is to be started from. Number of bytes depends on start address AAAA.
W_TX_PAYLOAD AD (WTP)	0010 0000	Write TX-payload: 1 – 32 bytes. A write operation always starts at byte 0.
R_TX_PAYLOAD AD (RTP)	0010 0001	Read TX-payload: 1 – 32 bytes. A read operation always starts at byte 0.
W_TX_ADDRESS SS (WTA)	0010 0010	Write TX-address: 1 – 4 bytes. A write operation always starts at byte 0.
R_TX_ADDRESS SS (RTA)	0010 0011	Read TX-address: 1 – 4 bytes. A read operation always starts at byte 0.
R_RX_PAYLOAD AD (RRP)	0010 0100	Read RX-payload: 1 – 32 bytes. A read operation always starts at byte 0.
CHANNEL_CONFIGURATION (CC)	1000 pphc cccc cccc	Special command for fast setting of CH_NO, HFREQ_PLL and PA_PWR in the CONFIGURATION REGISTER. CH_NO= cccccccc, HFREQ_PLL = h PA_PWR = pp
STATUS REGISTER	N.A.	The content of the status register (S[7:0]) is always read to MISO after a high to low transition on CSN as shown in Figure 6 . and Figure 7 .

Table 13. Instruction set for the nRF905 SPI.

A read or a write operation may operate on a single byte or on a set of succeeding bytes from a given start address defined by the instruction. When accessing succeeding bytes, you read or write the MSB of the byte with the smallest byte number first.

9.3 SPI Timing

The interface supports SPI mode 0. SPI operation and timing is given in [Figure 6](#), to [Figure 8](#), and in [Table 14](#). The device must be in one of the power saving modes for you to read or write to the configuration registers.

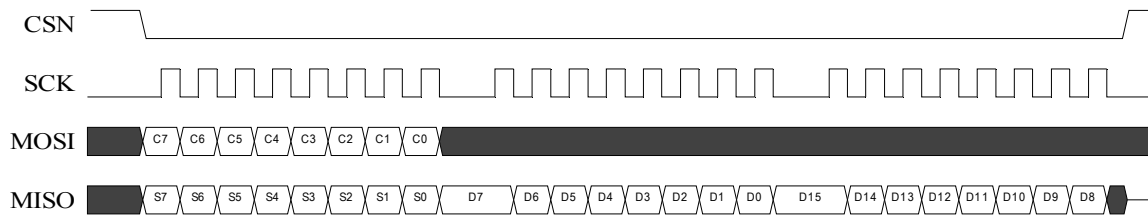


Figure 6. SPI read operation.

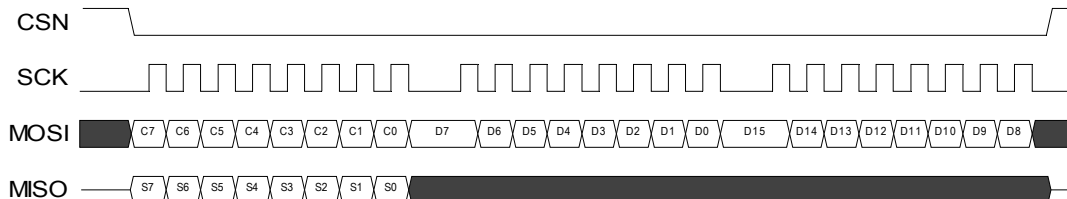


Figure 7. SPI write operation.

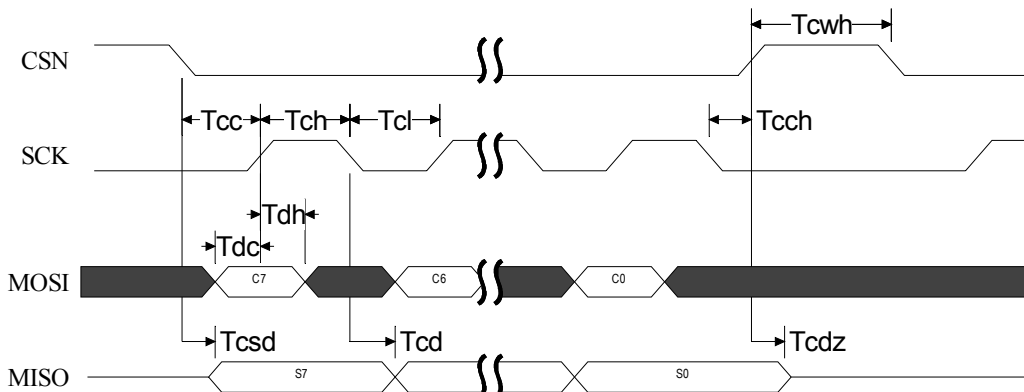


Figure 8. SPI NOP timing diagram.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Data to SCK Setup	Tdc	5		ns
SCK to Data Hold	Tdh	5		ns
CSN to Data Valid	Tcsd		45	ns
SCK to Data Valid	Tcd		45	ns
SCK Low Time	Tcl	40		ns
SCK High Time	Tch	40		ns
SCK Frequency	Tsck	DC	10	MHz
SCK Rise and Fall	Tr,Tf		100	ns
CSN to SCK Setup	Tcc	5		ns
SCK to CSN Hold	Tcch	5		ns
CSN Inactive time	Tcwh	500		ns
CSN to Output High Z	Tcdz		45	ns

Table 14. SPI timing parameters ($C_{load} = 10pF$)

9.4 RF – Configuration Register Description

Parameter	Bitwidth	Description
CH_NO	9	Sets center frequency together with HFREQ_PLL (default = 001101100 _b = 108 _d). $f_{RF} = (422.4 + CH_NO_d / 10) * (1 + HFREQ_PLL_d)$ MHz
HFREQ_PLL	1	Sets PLL in 433 or 868/915MHz mode (default = 0). '0' – Chip operating in 433MHz band '1' – Chip operating in 868 or 915 MHz band
PA_PWR	2	Output power (default = 00). '00' -10dBm '01' -2dBm '10' +6dBm '11' +10dBm
RX_RED_PWR	1	Reduces current in RX mode by 1.6mA. Sensitivity is reduced (default = 0). '0' – Normal operation '1' – Reduced power
AUTO_RETRAN	1	Retransmit contents in TX register if TRX_CE and TXEN are high (default = 0). '0' – No retransmission '1' – Retransmission of data packet
RX_AFW	3	RX-address width (default = 100). '001' – 1 byte RX address field width '100' – 4 byte RX address field width
TX_AFW	3	TX-address width (default = 100). '001' – 1 byte TX address field width '100' – 4 byte TX address field width
RX_PW	6	RX-payload width (default = 100000). '000001' – 1 byte RX payload field width '000010' – 2 byte RX payload field width . '100000' – 32 byte RX payload field width
TX_PW	6	TX-payload width (default = 100000). '000001' – 1 byte TX payload field width '000010' – 2 byte TX payload field width . '100000' – 32 byte TX payload field width
RX_ADDRESS	32	RX address identity. Used bytes depend on RX_AFW (default = E7E7E7E7 _h).
UP_CLK_FREQ	2	Output clock frequency (default = 11). '00' – 4MHz '01' – 2MHz '10' – 1MHz '11' – 500kHz
UP_CLK_EN	1	Output clock enable (default = 1). '0' – No external clock signal available '1' – External clock signal enabled

Parameter	Bitwidth	Description
XOF	3	Crystal oscillator frequency. Must be set according to external crystal resonant frequency (default = 100). '000' – 4MHz '001' – 8MHz '010' – 12MHz '011' – 16MHz '100' – 20MHz
CRC_EN	1	CRC – check enable (default = 1). '0' – Disable '1' – Enable
CRC_MODE	1	CRC – mode (default = 1). '0' – 8 CRC check bit '1' – 16 CRC check bit

Table 15. Configuration register description

9.5 Register Contents

RF-CONFIG_REGISTER (R/W)		
Byte #	Content bit[7:0], MSB = bit[7]	Init value
0	CH_NO[7:0]	0110_1100
1	bit[7:6] not used, AUTO_RETRAN, RX_RED_PWR, PA_PWR[1:0], HFREQ_PLL, CH_NO[8]	0000_0000
2	bit[7] not used, TX_AFW[2:0], bit[3] not used, RX_AFW[2:0]	0100_0100
3	bit[7:6] not used, RX_PW[5:0]	0010_0000
4	bit[7:6] not used, TX_PW[5:0]	0010_0000
5	RX_ADDRESS (device identity) byte 0	E7
6	RX_ADDRESS (device identity) byte 1	E7
7	RX_ADDRESS (device identity) byte 2	E7
8	RX_ADDRESS (device identity) byte 3	E7
9	CRC_MODE, CRC_EN, XOF[2:0], UP_CLK_EN, UP_CLK_FREQ[1:0]	1110_0111

Table 16. RF config register

TX_PAYLOAD (R/W)		
Byte #	Content bit[7:0], MSB = bit[7]	Init value
0	TX_PAYLOAD[7:0]	X
1	TX_PAYLOAD[15:8]	X
-	-	X
-	-	X
30	TX_PAYLOAD[247:240]	X
31	TX_PAYLOAD[255:248]	X

Table 17. TX payload register

TX_ADDRESS (R/W)		
Byte #	Content bit[7:0], MSB = bit[7]	Init value
0	TX_ADDRESS[7:0]	E7
1	TX_ADDRESS[15:8]	E7
2	TX_ADDRESS[23:16]	E7
3	TX_ADDRESS[31:24]	E7

Table 18. TX address register

RX_PAYLOAD (R)		
Byte #	Content bit[7:0], MSB = bit[7]	Init value
0	RX_PAYLOAD[7:0]	X
1	RX_PAYLOAD[15:8]	X
	-	X
	-	X
30	RX_PAYLOAD[247:240]	X
31	RX_PAYLOAD[255:248]	X

Table 19. RX payload register

STATUS_REGISTER (R)		
Byte #	Content bit[7:0], MSB = bit[7]	Init value
0	AM, bit [6] not used, DR, bit [0:4] not used	X

Table 20. Status register

The length of all registers is fixed. However, the bytes in TX_PAYLOAD, RX_PAYLOAD, TX_ADDRESS and RX_ADDRESS used in ShockBurst™ RX/TX are set in the configuration register. Register content is not lost when the device enters one of the power saving modes.