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nRF9E5

433/868/915MHz RF Transceiver with Embedded 8051 Compatible Microcontroller and 4 Input, 10 Bit ADC

Product Specification

Key Features

- nRF905 433/868/915MHz transceiver
- 8051 compatible microcontroller
- 4 input, 10bit 80ksps ADC
- Single 1.9V to 3.6V supply
- Small 32 pin QFN (5x5mm) package
- Extremely low cost Bill of Material (BOM)
- Internal VDD monitoring
- 2.5µA standby with wakeup on timer or external pin
- Adjustable output power up to 10dBm
- Channel switching time less than 650µs
- Low TX supply current, typical 9mA @-10dBm
- Low RX supply current typical 12.5mA peak
- Low MCU supply current, typically 1mA at 4MHz @3volt
- Suitable for frequency hopping
- Carrier Detect for “listen before transmit protocol”

Applications

- Sports and leisure equipment
- Alarm and security system
- Industrial sensors
- Remote control
- Surveillance
- Automotive
- Telemetry
- Keyless entry
- Toys

September 2011

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Data sheet status	
Objective product specification	This product specification contains target specifications for product development.
Preliminary product specification	This product specification contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
Product specification	This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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Writing conventions

This product specification follows a set of typographic rules that makes the document consistent and easy to read. The following writing conventions are used:

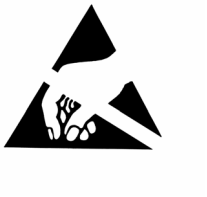
- Commands, bit state conditions, and register names are written in `Courier`.
- Pin names and pin signal conditions are written in **`Courier bold`**.
- Cross references are underlined and highlighted in blue.

Revision history

Date	Version	Description
June 2006	1.3	
April 2008	1.4	• Restructured layout in the new template • Updated package information • Added moisture sensitivity level to the absolute maximum ratings
April 2008	1.5	• Added layout example and application schematic for operation in the 433MHz and 868-915MHz ranges
September 2011	1.6	• Corrected the values in Table 85. on page 101

Attention!

Observe precaution for handling Electrostatic Sensitive Device.



Datasheet order code: 051005nRF9E5

Contents

1 Introduction

nRF9E5 is a true single chip system with fully integrated RF transceiver, 8051 compatible microcontroller and a 4 input 10bit 80ksps AD converter. The transceiver of the system supports all the features available in the nRF905 chip including ShockBurst™, which automatically handles preamble, address and CRC. The circuit has embedded voltage regulators, which provide maximum noise immunity and allow operation on a single 1.9V to 3.6V supply. nRF9E5 is compatible with FCC standard CFR47 part 15 and ETSI EN 300 220-1.

2 Quick reference data

Parameter	Value	Unit
Minimum supply voltage	1.9	V
Temperature range	-40 to +85	°C
Supply current in transmit @ -10dBm output power	9	mA
Supply current in receive mode	12.5	mA
Supply current for µ-controller 4MHz @ 3volt	1	mA
Supply current for ADC	0.9	mA
Maximum transmit output power	10	dBm
Data rate	50	kbps
Sensitivity	-100	dBm
Supply current in power down mode	2.5	µA

Table 1. nRF9E5 quick reference data.

3 Block diagram

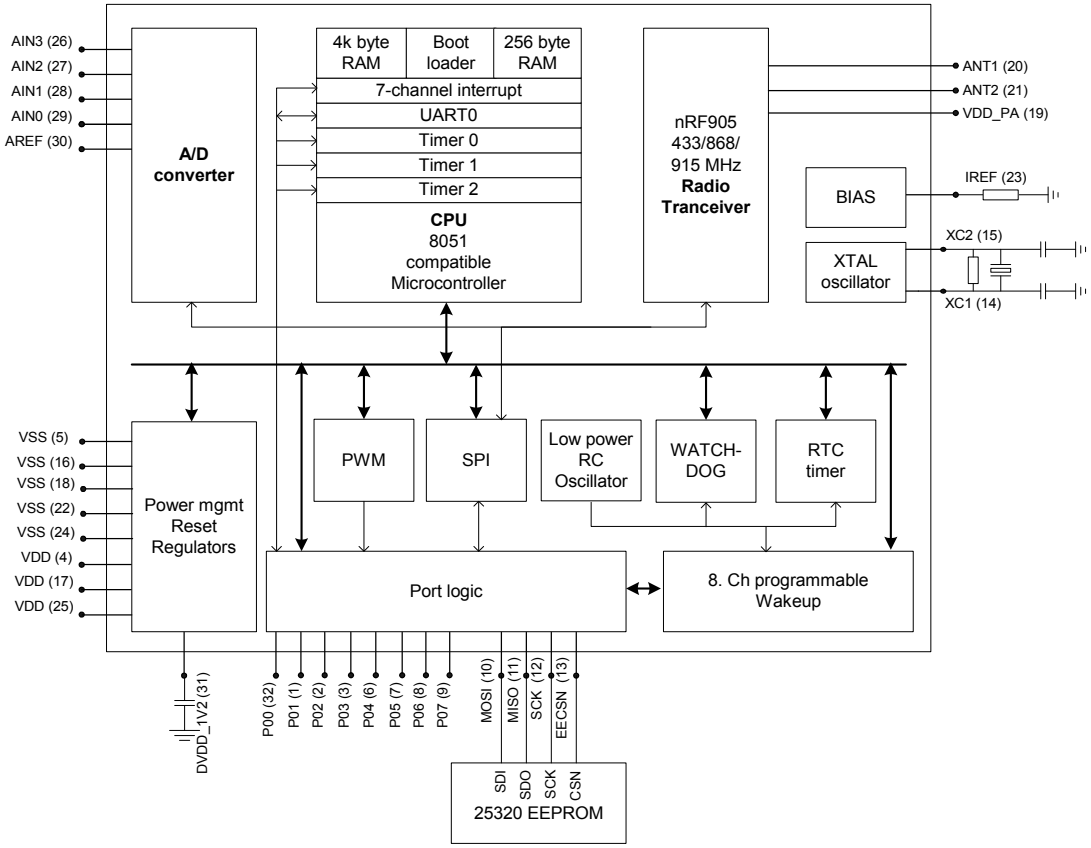


Figure 1. nRF9E5 block diagram

4 Architectural overview

This section gives you a brief overview of each of the blocks in Figure 1. on page 10.

4.1 Microcontroller

The nRF9E5 microcontroller is instruction set compatible with the industry standard 8051. Instruction timing is slightly different from the industry standard, typically each instruction uses from 4 to 20 clock cycles, compared with 12 to 48 for the standard. The interrupt controller is extended to support five additional interrupt sources; ADC, SPI, two for the radio and a wakeup function. There are also three timers that are 8052 compatible, plus some extensions, in the microcontroller core. An 8051 compatible UART that can use timer1 or timer2 for baud rate generation in the traditional asynchronous modes is included. The CPU is equipped with two data pointers to facilitate easier movement of data in the XRAM area, which is a common 8051 extension. The microcontroller clock is derived from the crystal oscillator.

4.1.1 Memory configuration

The microcontroller has a 256-byte data ram (8052 compatible, with the upper half only addressable by register indirect addressing). A small ROM of 512 bytes contains a bootstrap loader that is executed automatically after power on reset or if initiated by software later. The user program is normally loaded into a 4k byte RAM from an external serial EEPROM by the bootstrap loader. The 4k byte RAM may also (partially) be used for data storage in some applications.

Note: Optionally this 4k block of memory can be configured as 2k mask ROM and 2k RAM or 4k mask ROM.

4.1.2 Boot EEPROM/FLASH

The program code for the device must be loaded from an external non-volatile memory. The default boot loader expects this to be a “generic 25320” EEPROM with a SPI. These memories are available from several vendors with supply ranges down to 1.8V. The SPI uses the pins **MISO** (from EEPROM SDO), **SCK** (to EEPROM SCK), **MOSI** (to EEPROM SDI) and **EECSN** (to EEPROM CSN). When the boot is completed, the **MISO** (P1.2), **MOSI** (P1.1) and **SCK** (P1.0) pins may be used for other purposes such as other SPI devices or GPIO (General Purpose Input Output).

4.1.3 Register map

The SFRs (Special Function Registers) control several of the features of the nRF9E5. Most of the nRF9E5 SFRs are identical to the standard 8051 SFRs. However, there are additional SFRs that control features that are not available in the standard 8051.

The SFR map is shown in Table 2.. The registers with grey background are registers with industry standard 8051 behavior. Note that the function of P0, P1 and P2 are somewhat different from the “standard” even if the conventional addresses (0x80, 0x90 and 0xA0) are used.

	X000	X001	X010	X011	X100	X101	X110	X111
F8	EIP						HWREV	
F0	B							
E8	EIE							
E0	ACC							
D8	EICON							

	X000	X001	X010	X011	X100	X101	X110	X111
D0	PSW							
C8	T2CON		RCAP2L	RCAP2H	TL2	TH2		
C0								
B8	IP							CKLFCON
B0		RSTREAS	SPI_DATA	SPI_CTRL	SPICLK	TICK_DV	CK_CTRL	TEST_MODE
A8	IE	PWMCON	PWMDUTY	REGX_MSB	REGX_LSB	REGX_CTRL		
A0	P2							
98	SCON	SBUF						
90	P1	EXIF	MPAGE	P0_DRV	P0_DIR	P0_ALT	P1_DIR	P1_ALT
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	SPC_FNC
80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON

Table 2. SFR Register map.

4.2 PWM

The nRF9E5 has one programmable PWM (Pulse-Width Modulation) output, which is the alternate function of P0.7. The resolution of the PWM is software programmable to 6, 7 or 8 bits. The frequency of the PWM signal is programmable through a 6 bit prescaler from the crystal oscillator. The duty cycle is programmable between 0% and 100% through a one 8 bit register.

4.3 SPI

nRF9E5 features a simple single buffered SPI (Serial Programmable Interface) master. The 3 data lines of the SPI bus (**MISO**, **SCK** and **MOSI**) are multiplexed (by writing to register SPI_CTRL) between the GPIO pins (lower 3 bits of P1) and the RF transceiver and AD subsystems. The SPI hardware does not generate any chip select signal. You typically use GPIO bits (from port P0) to act as chip selects for one or more external SPI devices. The **EECSN** pin is a general purpose I/O dedicated as chip select for the boot EEPROM. When the SPI interfaces the RF transceiver, the chip selects are available in an internal GPIO port, P2.

4.4 Port logic

The device has 8 general purpose bi-directional pins (the P0 port). Additionally the 4 SPI data pins may be used as general purpose I/O (the P1). Most of the GPIO pins can be used for multiple purposes under program control. The alternate functions include two external interrupts, UART RXD and TXD, a SPI master port, three enable/count signals for the timers and the PWM output and a slow programmable timer. Each pin in the P0 port can be programmed for high sink or source current.

4.5 Power management

The nRF9E5 can be placed into several low power modes under program control, and the ADC and RF subsystems can be turned on or off under program control. The CPU stops, but all RAM's and registers maintain their values. The watchdog, RTC (Real Time Clock) wakeup timer and the GPIO wakeup function

are always active during power down. The current consumption is typically 2.5µA when running with the crystal oscillator off.

The device can exit the power down modes by an external pin, by an event on any of the P0 GPIO pins, by the wakeup timer if enabled or by a watchdog reset.

4.6 LF clock, RTC wakeup timer, GPIO wakeup and watchdog

The nRF9E5 contains an internal low frequency clock CKLF that is always on. When the crystal oscillator clocks the circuit, the CKLF is a 4kHz clock derived from the crystal oscillator. When no crystal oscillator clock is available, the CKLF is a low power RC oscillator that cannot be disabled, so it runs continuously as long as VDD is 1.8V. The RTC Wakeup timer, the GPIO wakeup and watchdog all run on the CKLF to ensure these vital functions works during all power down modes.

RTC Wakeup timer is a 24 bit programmable down counter and the Watchdog is a 16 bit programmable down counter. The resolution of the watchdog and wakeup timer is programmable (with prescaler TICK_DV) from approximately 300µs to approximately 80ms. By default the resolution is 1ms. The wakeup timer can be started and stopped by user software. The watchdog is disabled after a reset, but if activated it cannot be disabled again, except by another reset. An RTC Wakeup timer timeout also provides a programmable pulse (GTIMER) that can be an output on a GPIO pin.

The GPIO wakeup function lets the software enable wakeup on one or more pins from the P0 GPIO port. The edge sensitivity (rising, falling or both) and de-bouncing filter is individually programmable for each pin.

4.7 Crystal oscillator

The microcontroller, AD converter and transceiver run on the same crystal oscillator generated clock. A range of crystals frequencies from 4 to 20MHz may be utilized. For details, please see chapter 10.1 on page 26. The oscillator may be started and stopped as requested by software.

4.8 AD converter

The nRF9E5 AD converter has up to 10 bit dynamic range and linearity with a conversion rate of 80 ksps used at the Nyquist rate. The reference for the AD converter is software selectable between the **AREF** input and an internal 1.22V bandgap reference.

The converter has 5 inputs selectable by software. Selecting one of the inputs 0 to 3 converts the voltage on the respective **AIN0** to **AIN3** pin. Input 4 enables software to monitor the nRF9E5 supply voltage by converting an internal input that is VDD/3 with the 1.22V internal reference selected. The AD converter is typically used in a start/stop mode. The sampling time is then under software control. The converter is by default configured as 10 bits. For special requirements, the AD converter can be configured by software to perform 6, 8 or 12 bit conversions. The converter may also be used in differential mode with **AIN0** used as negative input and one of the other 3 external inputs used as noninverting input.

4.9 Radio transceiver

The transceiver part of the circuit has identical functionality to the nRF905 single chip RF transceiver. It is accessed through an internal parallel port and/or an internal SPI. You can program the data ready, carrier-detect and address match signals as interrupts to the microcontroller or polled through a GPIO port.

The nRF905 is a radio transceiver for the 433/868/915MHz ISM bands. The transceiver consists of a fully integrated frequency synthesizer, a power amplifier, a modulator and a receiver unit. Output power and frequency channels and other RF parameters are easily programmable by using the on-chip SPI. RF current consumption is only 9 mA in TX mode (output power -10dBm) and 12.5 mA in RX mode. For power saving the transceiver can be turned on/off under software control.

Note: This document should be read in conjunction with the nRF905 datasheet.

5 Absolute maximum ratings

Operating conditions	Minimum	Maximum	Units
Supply voltages			
VDD	-0.3	+3.6	V
VSS		0	V
Input voltage			
For analog pins, **AIN0** to **AIN3** and **AREF**:			
V_{IA}	-0.3	+2.0	V
For all other pins:			
V_I	-0.3	VDD +0.3	V
Output voltage			
V_O	-0.3	VDD +0.3	V
Total power dissipation			
P_D (T_A=85°C)		230	mW
Temperatures			
Operating temperature	-40	+85	°C
Storage temperature	-40	+125	°C
Moisture sensitivity level			
		260	°C

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Table 3. Absolute maximum ratings

6 Electrical specifications

Conditions: VDD = +3V, VSS = 0V, TEMP = -40ºC to +85ºC (typical +27ºC)

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
VDD	Supply voltage		1.9		3.6	V
TEMP	Operating temperature		-40		85	ºC

Table 4. Operating conditions

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
V_{IH}	HIGH level input voltage		0.7 VDD		VDD	V
V_{IL}	LOW level input voltage		VSS		0.3 VDD	V
Ci	Pin capacitance				5	pF
I_{IL}	Pin leakage current	a			±10	nA
V_{OH}	HIGH level output voltage (I_{OH}=-0.5mA)		VDD-0.3		VDD	V
V_{OL}	LOW level output voltage (I_{OL}=0.5mA)		VSS		0.3	V

a. Max value determined by design and characterization testing.

Table 5. Digital input/output

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
I_{PD}	Supply current in power down mode	a		2.5		µA

a. Pin voltages are VSS or VDD

Table 6. General electrical specification

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
I_{VDD_MCU}	Supply current @4MHz @3V			1		mA
I_{OL_HD}	High drive sink current for **P06**, **P04**, **P02** and **P00** @ VOL = 0.4V	a			10	mA
I_{OH_HD}	High drive source current for **P07**, **P05**, **P03** and **P01** @ VOH = VDD-0.4V	a			10	mA
f_{LP_OSC}	Low power RC oscillator frequency		1		5.5	KHz

a. Higher sink/source current is possible if increased voltage changes on ports are accepted

Table 7. General microcontroller conditions

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
f_{OP}	Operating frequency	a	430		928	MHz
f_{XTAL}	Crystal frequency	b	4		20	MHz
Δf	Frequency deviation		±42	±50	±58	kHz
BR	Data rate	c		50		kbps
f_{CH_433}	Channel spacing @ 433MHz			100		kHz
f_{CH_868}	Channel spacing @ 868 and 915MHz			200		kHz

a. Operates in the 433, 868 and 915MHz ISM band.
b. The crystal frequency may be chosen from 5 different values (4, 8, 12, 16, and 20MHz) which are specified in the configuration word. Please see Table 29. on page 45.
c. Data is Manchester-encoded before GFSK modulation.

Table 8. General RF conditions

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
P_{RF10}	Output power 10dBm setting	a	7	10	11	dBm
P_{RF6}	Output power 6dBm setting	a	3	6	9	dBm
P_{RF-2}	Output power –2dBm setting	a	-6	-2	2	dBm
P_{RF-10}	Output power -10dBm setting	a	-14	-10	-6	dBm
P_{BW_-16}	-16dBc bandwidth for modulated carrier	b		173		kHz
P_{BW_-24}	-24dBc bandwidth for modulated carrier	b		222		kHz
P_{BW_-32}	-32dBc bandwidth for modulated carrier	b		238		kHz
P_{BW_-36}	-36dBc bandwidth for modulated carrier	b		313		kHz
P_{RF1}	1^{st} adjacent channel transmit power	c		-27		dBc
P_{RF2}	2^{nd} adjacent channel transmit power	c		-54		dBc
$I_{TX10dBm}$	Supply current @ 10dBm output power			30		mA
$I_{TX-10dBm}$	Supply current @ -10dBm output power			9		mA

a. Optimum load impedance.
b. Data is Manchester-encoded before GFSK modulation.
c. Channel width and channel spacing is 200kHz.

Table 9. Transmitter operation

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
I_{RX}	Supply current in receive mode			12.5		mA
RX_{SENS}	Sensitivity at 0.1%BER			-100		dBm
RX_{MAX}	Maximum received signal		0			dBm
C/I_{CO}	C/I Co-channel	a		13		dB
C/I_{1ST}	1^{st} adjacent channel selectivity C/I 200kHz	a		-7		dB
C/I_{2ND}	2^{nd} adjacent channel selectivity C/I 400kHz	a		-16		dB
C/I_{+1M}	Blocking at +1MHz	a		-40		dB
C/I_{-1M}	Blocking at -1MHz	a		-50		dB
C/I_{-2M}	Blocking at -2MHz	a		-63		dB

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
C/I_{+5M}	Blocking at +5MHz	a		-70		dB
C/I_{-5M}	Blocking at -5MHz	a		-65		dB
C/I_{+10M}	Blocking at +10MHz	a		-69		dB
C/I_{-10M}	Blocking at -10MHz	a		-67		dB
C/I_{IM}	Image rejection	a		-36		dB

a. Channel Level +3dB over sensitivity, interfering signal a standard carrier wave, image 2MHz above wanted.

Table 10. Receiver operation

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
DNL	Differential Nonlinearity f_{IN} = 0.9991 kHz			±0.5		LSB
INL	Integral Nonlinearity f_{IN} = 0.9991 kHz			±0.75		LSB
SNR	Signal to Noise Ratio (DC input)			59		dBFS
V_{OS}	Midscale offset			± 1		%FS
ε_G	Gain Error			±1		%FS
SNR	Signal to Noise Ratio (without harmonics) f_{IN} = 10 kHz		53	58		dBFS
SFDR	Spurious Free Dynamic Range f_{IN} = 10 kHz			65		dB
V_{BG}	Internal reference		1.1	1.22	1.3	V
	Internal reference voltage drift			100		ppm/°C
V_{FS}	Reference voltage input (external ref)		0.8		1.5	V
F_S	Conversion rate	a			125	ksps
I_{ADC}	Supply current ADC operation			1		mA
t_{NPD}	Start up time from ADC Power down			15		µs

a. Conversion rate is dependant on resolution, Please see section 13.3 on page 39 .

Table 11. ADC operation

6.1 Current information for all operating modes

Mode	XO frequency	Typical current
Light power down	4MHz	0.45 mA
Moderate Power down	4MHz	100 uA
Standby mode	4MHz	12 uA
Deep Power Down	-	2.5 uA
MCU at 0.5MHz 3 volt	4MHz	0.55 mA [a]
MCU at 1MHz 3 volt	4MHz	0.60 mA [a]
MCU at 2MHz 3 volt	4MHz	0.70 mA [a]
MCU at 4MHz 3 volt	4MHz	0.90 mA [a]
MCU at 8Mhz 3 volt	8MHz	1.4 mA [a]
MCU at 12MHz 3 volt	12MHz	1.8 mA [a]
MCU at 16MHz 3 volt	16MHz	2.2 mA [a]
MCU at 20MHz 3 volt	20MHz	2.6 mA [a]
Rx at 433MHz	16MHz	12.2 mA
Rx at 868MHz/915MHz	16MHz	12.8 mA
Reduced Rx	16MHz	10.5 mA
Tx at 10dBm output power	16MHz	30 mA
Tx at 6dBm output power	16MHz	20 mA
Tx at -2dBm output power	16MHz	14 mA
Tx at -10dBm output power	16MHz	9 mA

a. Typical current given for medium MCU activity. Measured current may differ with higher or lower MCU activity or with other XO frequency than given in the table.

Table 12.Current information for all operating modes.

7 Pin information

7.1 Pin assignment

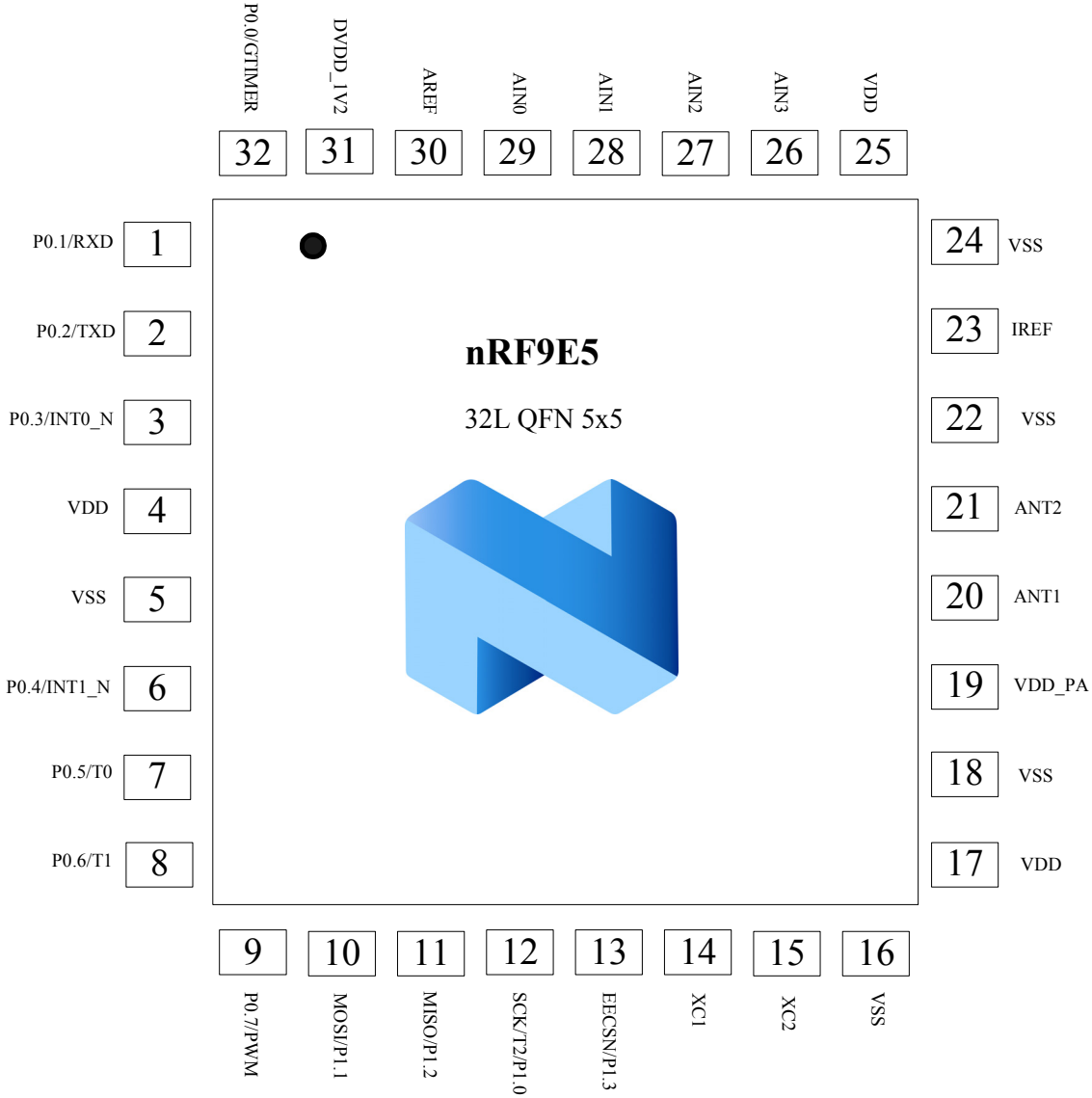


Figure 2. Pin assignment nRF9E5.

7.2 Pin function

Pin	Name	Pin function	Description
1	P01	Digital IN/OUT	uP Bi-directional digital pin
2	P02	Digital IN/OUT	uP Bi-directional digital pin
3	P03	Digital IN/OUT	uP Bi-directional digital pin
4	VDD	Power	Power supply (+3V DC)
5	VSS	Power	Ground (0V)
6	P04	Digital IN/OUT	uP Bi-directional digital pin
7	P05	Digital IN/OUT	uP Bi-directional digital pin
8	P06	Digital IN/OUT	uP Bi-directional digital pin
9	P07	Digital IN/OUT	uP Bi-directional digital pin
10	MOSI	SPI-Interface	SPI output
11	MISO	SPI-Interface	SPI input
12	SCK	SPI-clock	SPI clock
13	EECSN	SPI-enable	SPI enable, active low
14	XC1	Analog Input	Crystal Pin 1/ External clock reference pin
15	XC2	Analog Output	Crystal Pin 2
16	VSS	Power	Ground (0V)
17	VDD	Power	Power supply (+3V DC)
18	VSS	Power	Ground (0V)
19	VDD_PA	Power Output	Regulated positive supply (1.8V) to nRF905 power amplifier
20	ANT1	RF – port	Antenna interface 1
21	ANT2	RF – port	Antenna interface 2
22	VSS	Power	Ground (0V)
23	IREF	Analog Input	Reference current
24	VSS	Power	Ground (0V)
25	VDD	Power	Power supply (+3V DC)
26	AIN3	Analog Input	ADC Input 3
27	AIN2	Analog Input	ADC Input 2
28	AIN1	Analog Input	ADC Input 1
29	AIN0	Analog Input	ADC Input 0
30	AREF	Analog Input	ADC Reference Voltage
31	DVDD_1V2	Power Output	Low voltage positive digital supply output for de-coupling
32	P00	Digital IN/OUT	uP Bi-directional digital pin

Table 13. nRF9E5 pin function.

8 System clock

The microcontroller clock, CPU_CLK, is generated from the on-chip crystal oscillator. CPU_CLK frequency is configured in the RF configuration register (see chapter 14 on page 41) and can be set to 0.5, 1, 2 or 4MHz. CPU_CLK could in addition be set equal to the crystal oscillator frequency itself. The CPU_CLK generation is illustrated in Figure 3.

Note: It is important to always set XOF equal to the actual crystal selected for the application.

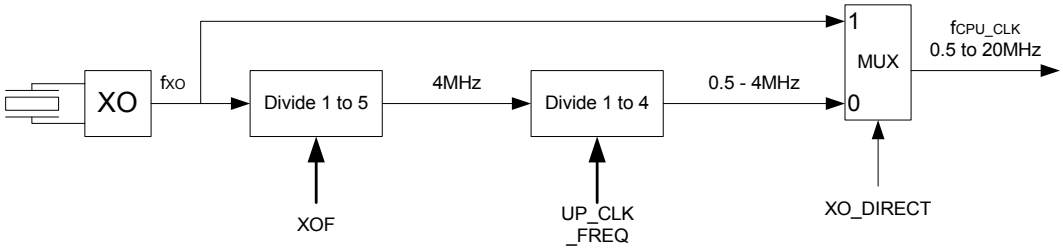


Figure 3. CPU_CLK generation in nRF9E5.

The SFR 0xBF, CKLFCON, has to correspond with XOF, UP_CLK_FREQ and XO_DIRECT. SFR 0xBF is described in Table 50. on page 58.

Default values of UP_CLK_FREQ and XO_DIRECT are '00' and '0' respectively. That is, the default CPU_CLK frequency is 4MHz.

The chip has an internal low frequency clock that is always active. This clock ensures proper operation of vital functions when the chip is in power down mode and the crystal oscillator is turned off, please see chapter 19 on page 58.

9 Digital I/O ports

The nRF9E5 has two I/O ports located at the default locations for P0 and P1 in standard 8051, but the ports are fully bi-directional CMOS and the direction of each pin is controlled by a _DIR and an _ALT bit for each bit as shown in the table below.

Pin	Default function	Alternate=1	SPI CTRL != 01
EECSN	P1.3		P1.3
MISO	SPI.datain		P1.2
SCK	SPI.clock	T2 (timer2 input)	P1.0
MOSI	SPI.dataout		P1.1
P00	P0.0	GTIMER	
P01	P0.1	RXD (UART)	
P02	P0.2	TXD (UART)	
P03	P0.3	INT0_N (interrupt)	
P04	P0.4	INT1_N (interrupt)	
P05	P0.5	T0 (timer0 input)	
P06	P0.6	T1 (timer1 input)	
P07	P0.7	PWM	

Table 14. Port functions.

9.1 I/O port behavior during RESET

During this period the internal reset is active (regardless of whether or not the clock is running), all the port pins related to P0 are configured as inputs, whereas the inputs related to P1 are configured as required for an SPI master. When program execution starts, all ports are still configured as during reset. The program needs to set the _ALT and/or the _DIR register for the pins that need another direction.

9.2 Port 0 (P0)

P0_ALT and P0_DIR control the P0 port function in that order of priority. If the alternate function for port P0.n is set (by P0_ALT.n = 1) the pin is input or output as required by the alternate function (UART, external interrupt, timer inputs or PWM output), except that the UART RXD direction depends on P0_DIR.1.

To use INT0_N or INT1_N as interrupts, the corresponding alternate function must be activated. P0_ALT.3 / P0_ALT.4. P0_ALT.5 / P0_ALT.6 can be set to use P0.5 / P0.6 as a timer 0 / 1 control. In that case the CPU samples these signals every 4 CPU clock periods. When the P0_ALT.n is not set, bit ‘n’ of the port is a GPIO function with the direction controlled by P0_DIR.n.

Pin	Data in P0_ALT.n,P0_DIR.n							
	10		11		00		01	
P00	GTIMER	Out	GTIMER	Out	P0.0	Out	P0.0	In
P01	RXD	Out	RXD	In	P0.1	Out	P0.1	In
P02	TXD	Out	TXD	Out	P0.2	Out	P0.2	In
P03	INT0_N	In	INT0_N	In	P0.3	Out	P0.3	In
P04	INT1_N	In	INT1_N	In	P0.4	Out	P0.4	In
P05	T0	In	T0	In	P0.5	Out	P0.5	In
P06	T1	In	T1	In	P0.6	Out	P0.6	In
P07	PWM	Out	PWM	Out	P0.7	Out	P0.7	In

Table 15. Port 0 (P0) functions.

Port 0 is controlled by SFR registers 0x80, 0x93, 0x94 and 0x95 listed in the table below.

Addr SFR (hex)	R/W	#bit	Init value (hex)	Name	Function
80	R/W	8	FF	P0	Port 0, pins P07 to P00
93	R/W	8	00	P0_DRV	High drive strength for each bit of Port 0 1: Enable, : Disable (See 9.2.1 for a description)
94	R/W	8	FF	P0_DIR	Direction for each bit of Port 0 0: Output, 1: Input Direction is overridden if alternate function is selected for a pin.
95	R/W	8	00	P0_ALT	Select alternate functions for each pin of P0, if corresponding bit in P0_ALT is set, as listed in Table 15. Port 0 (P0) functions.

Table 16. Port 0 control and data SFR registers.

9.2.1 High current drive capability

Odd numbered bits source high current when the corresponding bit in P0_DRV is set, where as even number bits sink high current when the corresponding bit in P0_DRV is set.

9.3 Port 1 (P1 or SPI port)

The P1 port consists of 4 pins, one of which is a hardwired input. The primary function of the P1 port (when SPI_CTRL is 01) is as a SPI master port. The pin **EECSN** is used as a chip select for the boot EEPROM, the GPIO bits in port P0 may be used as chip select(s) for other SPI devices.

P1_ALT.0 can be set to use **SCK** (P1.0) as a timer 2 control. In that case the CPU samples this signal every 4 CPU clock periods. **MOSI** (P1.1) is now a GPIO. When P0_ALT.0 is 0, also **SCK** (P1.0) is a GPIO.

MISO (P1.2) is always an input. That is P1_DIR.2 and P1_ALT.2 are ignored.

EECSN (P1.3) is always a GPIO. It is activated by the default boot loader after reset and should be connected to the CSN of the boot flash.

Pin	SPI_CTRL = 01		SPI_CTL != 01					
			P1 ALT.n= 1		P1 ALT.n = 0			
					P1 DIR.n = 0		P1 DIR.n = 1	
SCK	SPI.clock	Out	T2	In	P1.0	Out	P1.0	In
MOSI	SPI.dataout	Out	P1.1	I/O[a]	P1.1	Out	P1.1	In
MISO	SPI.datain	In	P1.2	In	P1.2	In	P1.2	In
EECSN	P1.3	Out	P1.3	I/O[a]	P1.3	Out	P1.3	In

a. P1.1 and P1.3 are under control of P1_DIR.1 and P1_DIR.3 even when P1_ALT.1 or P1_ALT.3 are 1, since there are no alternate functions for these pins.

Table 17. Port 1 (P1) functions.

Port 1 is controlled by SFR registers 0x90, 0x96 and 0x97, and only the 4 lower bits of the registers are used.

Addr SFR (hex)	R/W	#bit	Init value (hex)	Name	Function
90	R/W	4	F	P1	Port 1, pins **SPI_SCK**, **SPI_MOSI**, **SPI_MISO** and **SPI_CSN**
96	R/W	4	4	P1_DIR	Direction for each bit of Port 1 0: Output, 1: Input Direction is overridden if alternate function is selected for a pin, or if **SPI_CTRL**=01. **SPI_MISO** is always input.
97	R/W	4	0	P1_ALT	Select alternate functions for each pin of P1 if corresponding bit in P1_ALT is set, as listed in Table 17. Port 1 (P1) functions

Table 18. Port 1 control and data SFR registers.

P1 is by default configured as a SPI master port. In this case, it is then controlled by the three SFR registers 0xB2, 0xB3 and 0xB4 as shown in Table 40. on page 51