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With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

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N-Channel PowerTrench® **MOSFET**

60 V, 110 A, 2.7 m Ω

Features

- Typical $R_{DS(on)} = 2.2 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 80 \text{ A}$
- Typical $Q_{g(tot)} = 80 \text{ nC}$ at $V_{GS} = 10 \text{ V}$, $I_D = 80 \text{ A}$
- UIS Capability
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Industrial Motor Drive
- Industrial Power Supply
- Industrial Automation
- Battery Operated Tools
- Battery Protection
- Solar Inverters
- UPS and Energy Inverters
- Energy Storage
- Load Switch

ABSOLUTE MAXIMUM RATINGS ($T_J = 25$ °C, Unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	60	V
Gate-to-Source Voltage	V_{GS}	±20	V
Drain Current – Continuous ($T_C = 25^{\circ}C$) ($V_{GS} = 10$) (Note 1)	I _D	110	Α
Pulsed Drain Current (T _C = 25°C)		See Figure 4	
Single Pulse Avalanche Energy (Note 2)	E _{AS}	193	mJ
Power Dissipation	P_{D}	176	W
Derate Above 25°C		1.2	W/°C
Operating and Storage Temperature Range	T _J , T _{STG}	–55 to +175	°C
Thermal Resistance, Junction to Case	$R_{ heta JC}$	0.85	°C/W
Maximum Thermal Resistance, Junction to Ambient (Note 3)	$R_{ heta JA}$	43	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

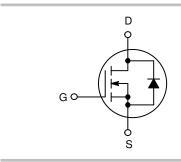
- 1. Current is limited by bondwire configuration.
- 2. Starting $T_J = 25$ °C, $L = 50 \mu H$, $I_{AS} = 88 A$, $V_{DD} = 60 V$ during inductor
- charging and $V_{DD} = 0$ V during time in avalanche.

 3. $R_{\theta,JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.



ON Semiconductor®

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D²PAK-3 TO-263 CASE 418AJ

MARKING DIAGRAM



NTBS2D7N06M7 = Specific Device Code = Assembly Location

= Year ww = Work Week = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity
NTBS2D7N06M7	NTBS2D7N	D ² PAK (TO-263)	330 mm	24 mm	800 Units

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
OFF CHARACT	TERISTICS				l	
BV _{DSS}	Drain-to-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60	_	-	V
I _{DSS}	Drain-to-Source Leakage Current	V _{DS} = 60 V, V _{GS} = 0 V, T _J = 25°C	-	_	1	μΑ
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 175°C (Note 4)	-	-	1	mA
I _{GSS}	Gate-to-Source Leakage Current	V _{GS} = ±20 V	-	_	±100	nA
ON CHARACTI	ERISTICS					
V _{GS(th)}	Gate-to-Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.0	3.2	4.0	V
R _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = 10 V, I _D = 80 A, T _J = 25°C	-	2.2	2.7	mΩ
		V _{GS} = 10 V, I _D = 80 A, T _J = 175°C (Note 4)		4.1	5.0	mΩ
YNAMIC CHA	ARACTERISTICS					
C _{iss}	Input Capacitance	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	6655	_	pF
C _{oss}	Output Capacitance		-	1745	-	pF
C _{rss}	Reverse Transfer Capacitance		-	57	-	pF
Rg	Gate Resistance	f = 1 MHz	-	2.2	-	Ω
Q _{g(tot)}	Total Gate Charge at 10 V	$V_{DD} = 30 \text{ V}, I_D = 80 \text{ A}, V_{GS} = 0 \text{ to } 10 \text{ V}$	-	80	110	nC
Q _{g(th)}	Threshold Gate Charge	$V_{DD} = 30 \text{ V}, I_D = 80 \text{ A}, V_{GS} = 0 \text{ to } 2 \text{ V}$	-	12	-	nC
Q_{gs}	Gate-to-Source Gate Charge	V _{DD} = 30 V, I _D = 80 A	-	35	-	nC
Q_{gd}	Gate-to-Drain "Miller" Charge	V _{DD} = 30 V, I _D = 80 A	-	10	_	nC
WITCHING CI	HARACTERISTICS					
t _(on)	Turn-On Time	V _{DD} = 30 V, I _D = 80 A,	-	_	115	ns
t _{d(on)}	Turn-On Delay	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	-	36	-	ns
t _r	Rise Time		-	52	-	ns
t _{d(off)}	Turn-Off Delay		-	36	-	ns
t _f	Fall Time		-	13	-	ns
t _{off}	Turn-Off Time		-	-	64	ns
PRAIN-SOUR	CE DIODE CHARACTERISTICS					
V_{SD}	Source-to-Drain Diode Voltage	V _{GS} = 0 V, I _{SD} = 80 A	-	-	1.25	V
		V _{GS} = 0 V, I _{SD} = 40 A	-	_	1.2	V
t _{rr}	Reverse–Recovery Time	$V_{DD} = 48 \text{ V, I}_F = 80 \text{ A,}$	-	78	102	ns
Q _{rr}	Reverse–Recovery Charge	$dI_{SD}/dt = 100 A/\mu s$	-	100	130	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 4. The maximum value is specified by design at $T_J = 175^{\circ}$ C. Product is not tested to this condition in production.

TYPICAL PERFORMANCE CHARACTERISTICS

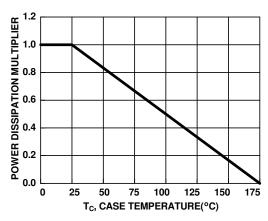


Figure 1. Normalized Power Dissipation vs.

Case Temperature

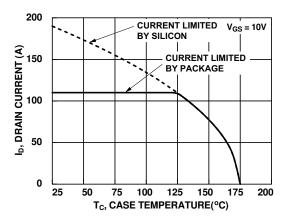


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

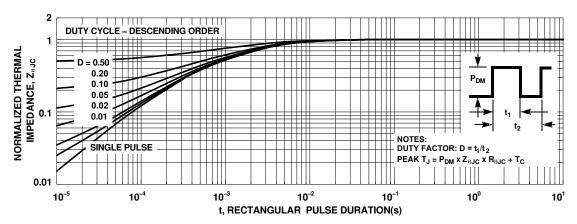


Figure 3. Normalized Maximum Transient Thermal Impedance

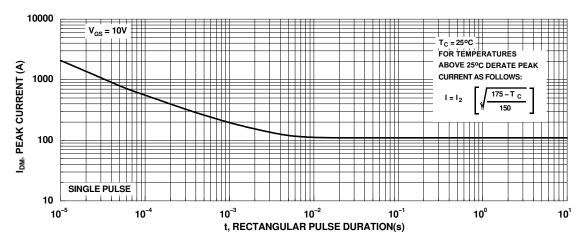


Figure 4. Peak Current Capability

TYPICAL PERFORMANCE CHARACTERISTICS

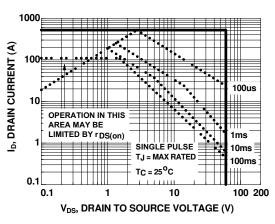
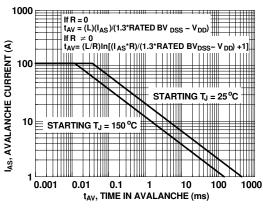


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

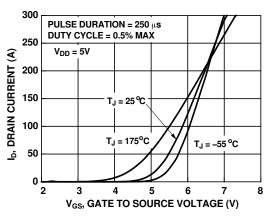


Figure 7. Transfer Characteristics

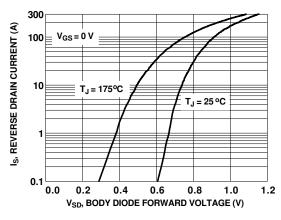


Figure 8. Forward Diode Characteristics

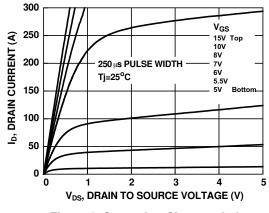


Figure 9. Saturation Characteristics

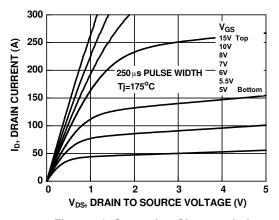


Figure 10. Saturation Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS

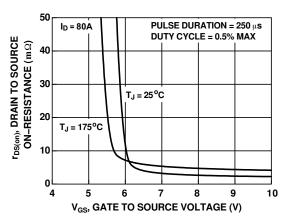


Figure 11. R_{DS(on)} vs. Gate Voltage

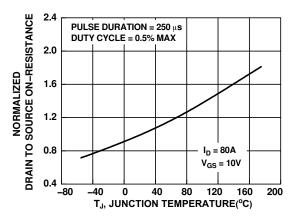


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

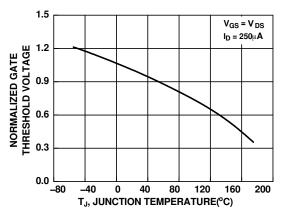


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

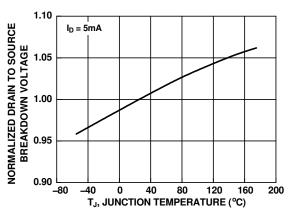


Figure 14. Normalized Drain-to-Source Breakdown Voltage vs. Junction Temperature

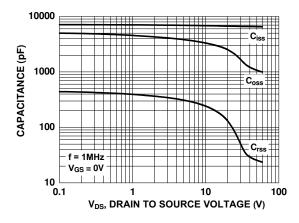


Figure 15. Capacitance vs. Drain-to-Source Voltage

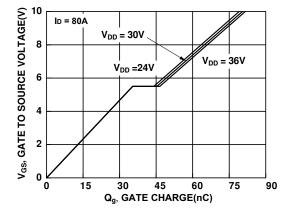
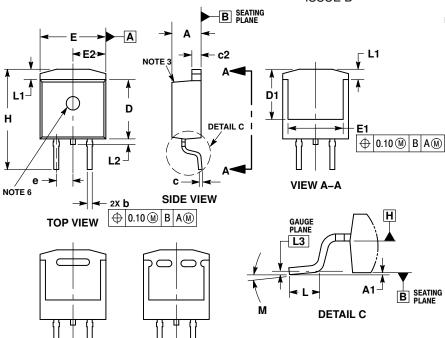


Figure 16. Gate Charge vs. Gate-to-Source Voltage

PACKAGE DIMENSIONS

D²PAK-3 (TO-263, 3-LEAD) CASE 418AJ ISSUE B



VIEW A-A
OPTIONAL CONSTRUCTIONS

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

 2. CONTROLLING DIMENSION: INCHES.

 3. CHAMFER OPTIONAL

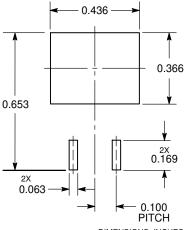
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.

 5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1 AND E1.

 6. OPTIONAL MOLD FEATURE

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
С	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260		6.60	
E	0.380	0.420	9.65	10.67
E1	0.245		6.22	
е	0.100 BSC		2.54 BSC	
Н	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1		0.066		1.68
L2		0.070		1.78
L3	0.010 BSC		0.25 BSC	
М	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: INCHES

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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