



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



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# NTHS5443

## Power MOSFET

-20 V, -4.9 A, P-Channel ChipFET™

### Features

- Low  $R_{DS(on)}$  for Higher Efficiency
- Logic Level Gate Drive
- Miniature ChipFET Surface Mount Package Saves Board Space
- Pb-Free Package is Available

### Applications

- Power Management in Portable and Battery-Powered Products; i.e., Cellular and Cordless Telephones and PCMCIA Cards

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	5 secs	Steady State	Unit
Drain-Source Voltage	$V_{DS}$	-20		V
Gate-Source Voltage	$V_{GS}$	$\pm 12$		V
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) (Note 1) $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	$I_D$	-4.9 -3.5	-3.6 -2.6	A
Pulsed Drain Current	$I_{DM}$	$\pm 15$		A
Continuous Source Current (Note 1)	$I_S$	-4.9	-3.6	A
Maximum Power Dissipation (Note 1) $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	$P_D$	2.5 1.3	1.3 0.7	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150		$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

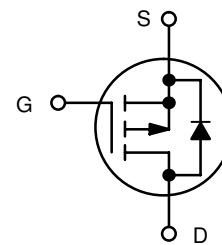
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).



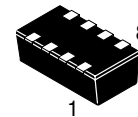
ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
-20 V	56 m $\Omega$ @ -4.5	-4.9 A

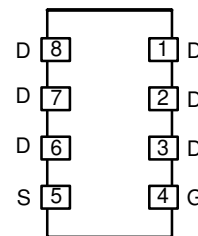


P-Channel MOSFET

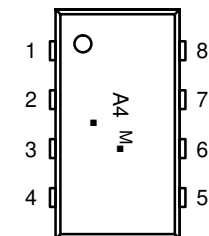


ChipFET  
CASE 1206A  
STYLE 1

### PIN CONNECTIONS



### MARKING DIAGRAM



A4 = Specific Device Code

M = Month Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTHS5443T1	ChipFET	3000/Tape & Reel
NTHS5443T1G	ChipFET (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTHS5443

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient (Note 2) $t \leq 5$ s Steady State	$R_{\theta JA}$	40 80	50 95	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Foot (Drain) Steady State	$R_{\theta JF}$	15	20	$^{\circ}\text{C}/\text{W}$

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-0.6			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1.0	$\mu\text{A}$
		$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 85^{\circ}\text{C}$			-5.0	
On-State Drain Current (Note 3)	$I_{D(on)}$	$V_{DS} \leq -5.0 \text{ V}, V_{GS} = -4.5 \text{ V}$	-15			A
Drain-Source On-State Resistance (Note 3)	$r_{DS(on)}$	$V_{GS} = -4.5 \text{ V}, I_D = -3.6 \text{ A}$ $V_{GS} = -3.6 \text{ V}, I_D = -3.3 \text{ A}$		0.056 0.065	0.065 0.074	$\Omega$
		$V_{GS} = -2.5 \text{ V}, I_D = -2.7 \text{ A}$		0.095	0.110	
Forward Transconductance (Note 3)	$g_{fs}$	$V_{DS} = -10 \text{ V}, I_D = -3.6 \text{ A}$		10		S
Diode Forward Voltage (Note 3)	$V_{SD}$	$I_S = -1.1 \text{ A}, V_{GS} = 0 \text{ V}$		-0.8	-1.2	V

### Dynamic (Note 4)

Total Gate Charge	$Q_G$	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -3.6 \text{ A}$		7.5	12	nC
Gate-Source Charge	$Q_{GS}$			0.9	2.8	
Gate-Drain Charge	$Q_{GD}$			2.2	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10 \text{ V}, R_L = 10 \Omega, I_D \cong -1.0 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_G = 6 \Omega$		8.5	13	ns
Rise Time	$t_r$			14	21	
Turn-Off Delay Time	$t_{d(off)}$			38	57	
Fall Time	$t_f$			30	45	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = -1.1 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		30	60	ns

- Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).
- Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.

TYPICAL ELECTRICAL CHARACTERISTICS

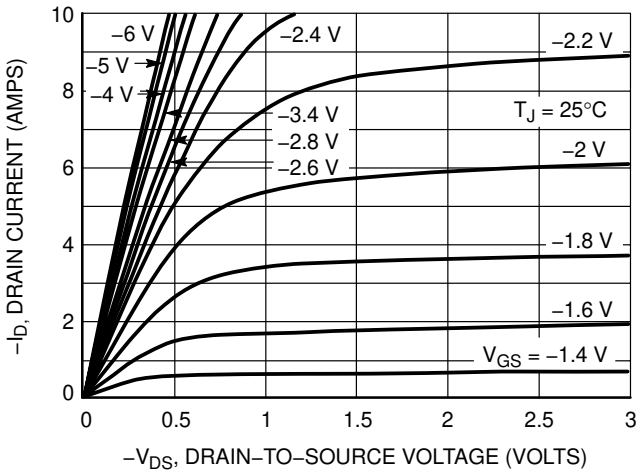


Figure 1. On-Region Characteristics

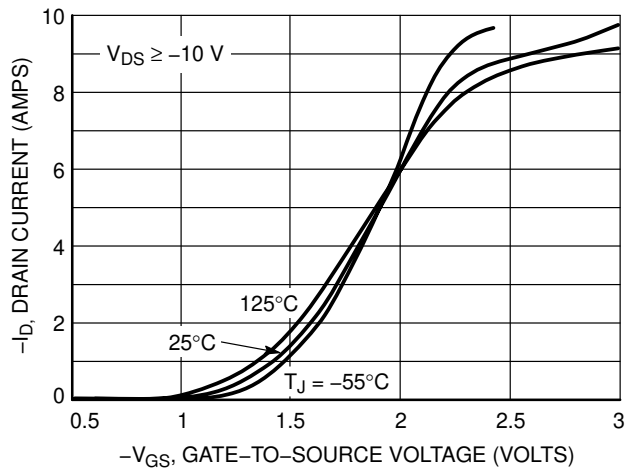


Figure 2. Transfer Characteristics

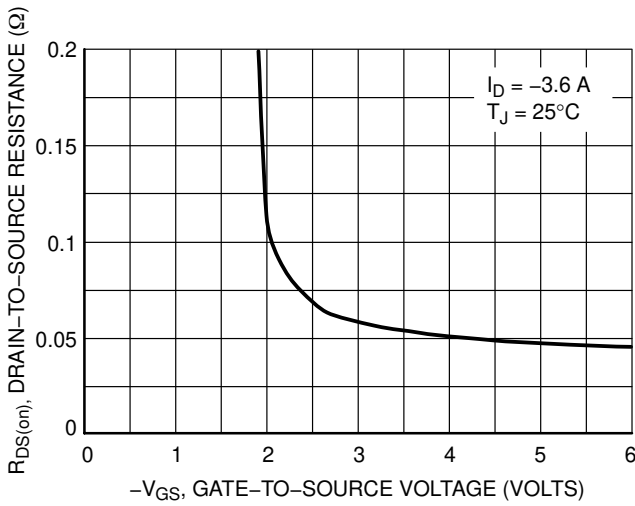


Figure 3. On-Resistance versus Gate-to-Source Voltage

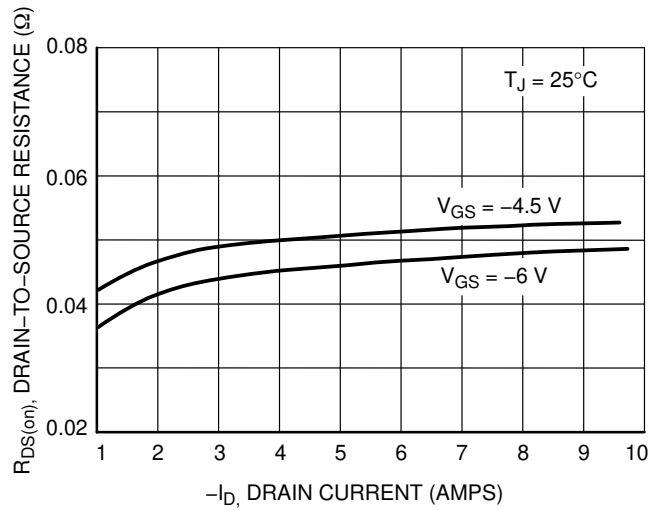


Figure 4. On-Resistance versus Drain Current and Gate Voltage

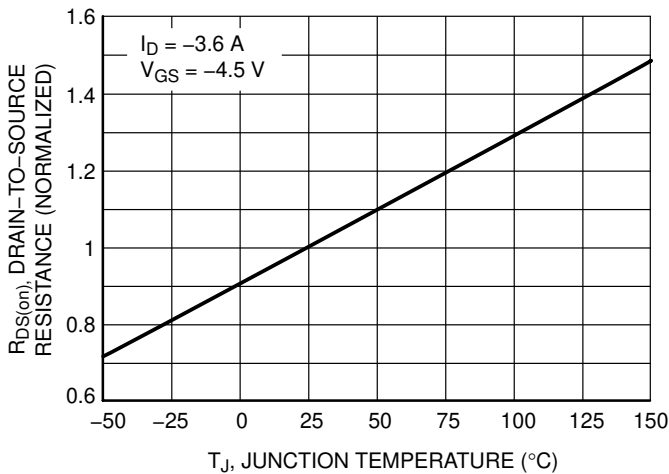


Figure 5. On-Resistance Variation with Temperature

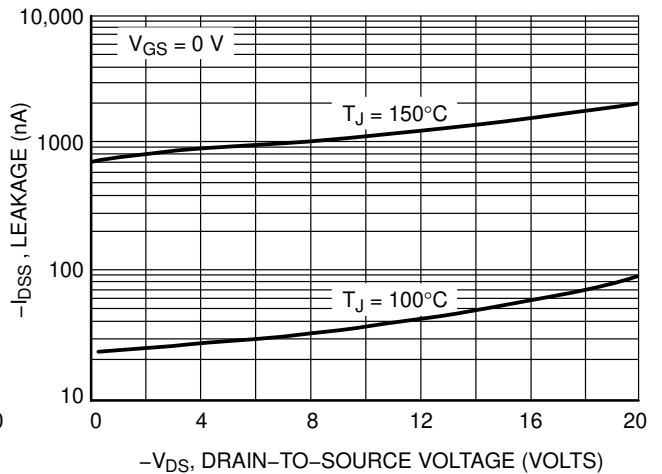


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

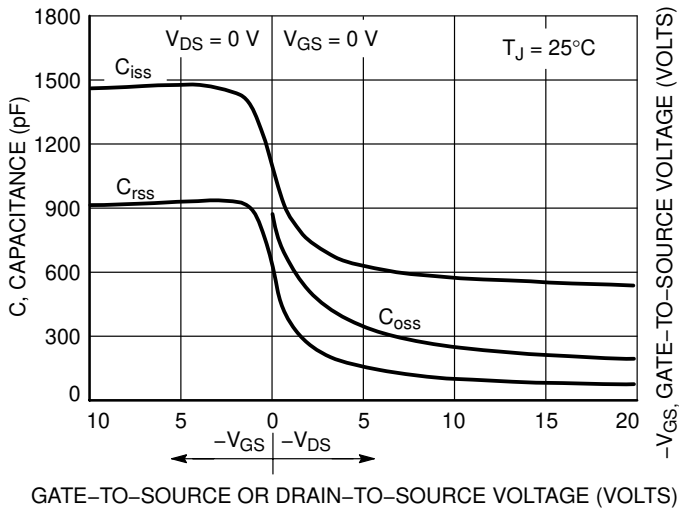


Figure 7. Capacitance Variation

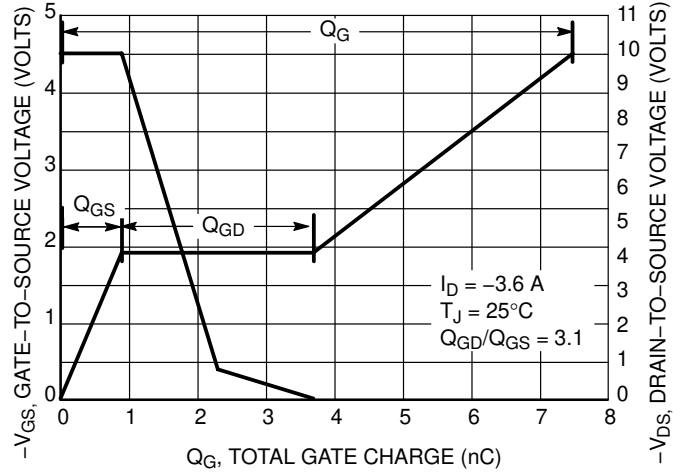


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

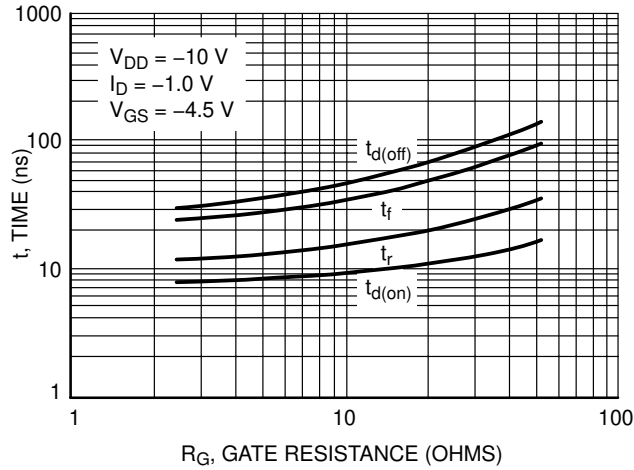


Figure 9. Resistive Switching Time Variation versus Gate Resistance

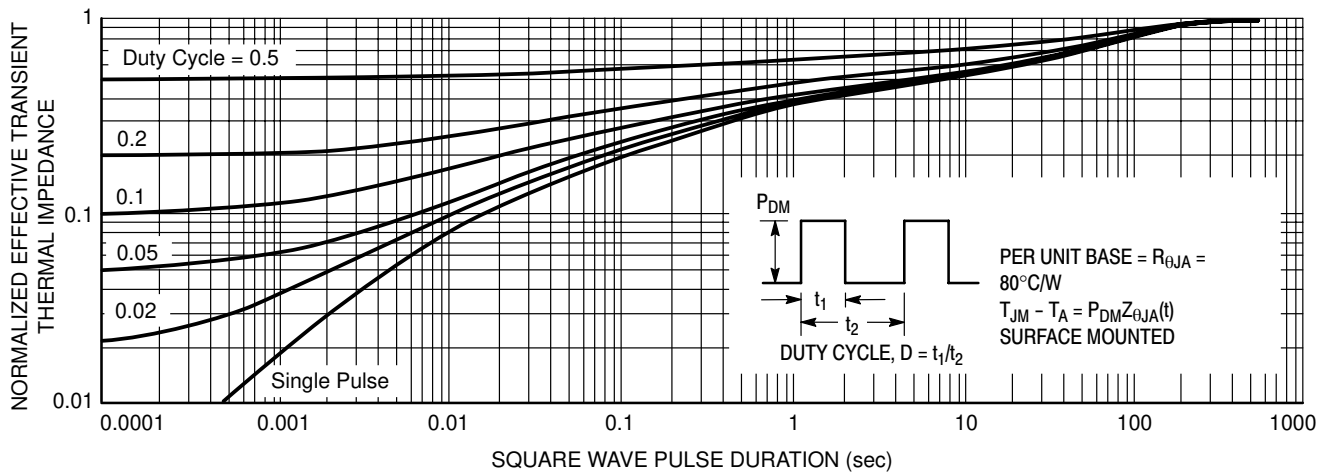
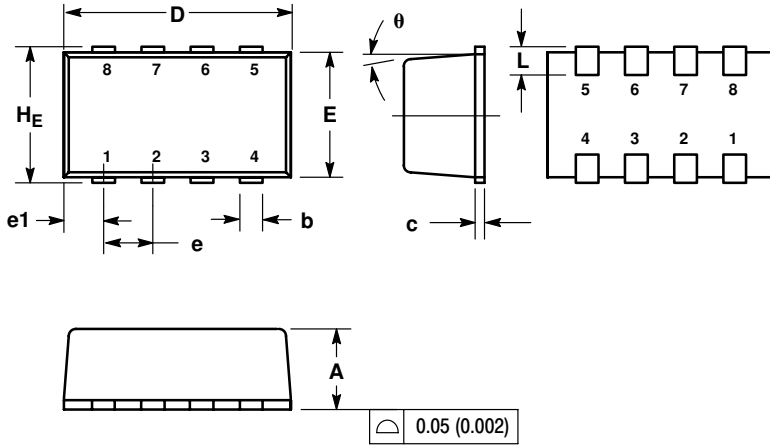


Figure 10. Normalized Thermal Transient Impedance, Junction-to-Ambient

# NTHS5443

## PACKAGE DIMENSIONS

ChipFET™  
CASE 1206A-03  
ISSUE G



### NOTES:

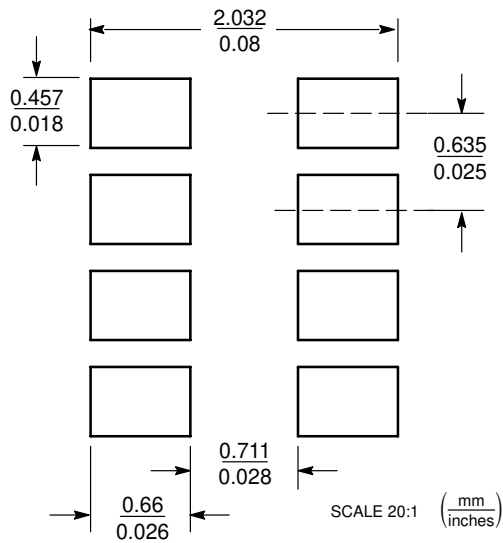
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
HE	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

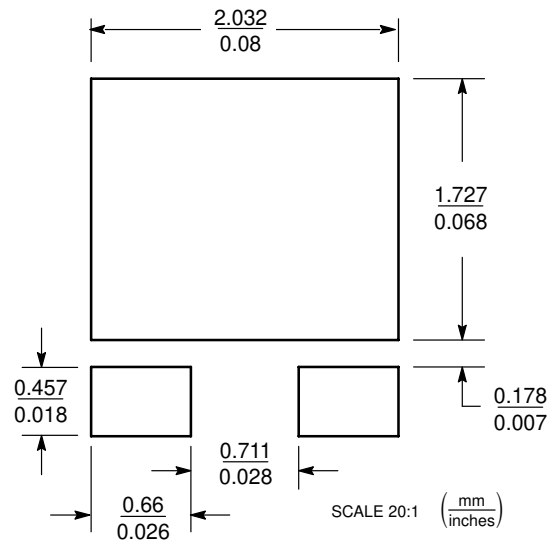
### STYLE 1:

- PIN 1: DRAIN  
2: DRAIN  
3: DRAIN  
4: GATE  
5: SOURCE  
6: DRAIN  
7: DRAIN  
8: DRAIN

## SOLDERING FOOTPRINT\*




Basic



Styles 1 and 4

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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