Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

NTLJD3183CZ

Power MOSFET

20 V/−20 V, 4.7 A/−4.0 A, Complementary, 2x2 mm, WDFN Package

Features

- WDFN 2x2 mm Package with Exposed Drain Pads for Excellent Thermal Conduction
- Lowest $R_{DS(on)}$ in 2x2 mm Package
- Footprint Same as SC−88 Package
- Low Profile (< 0.8 mm) for Easy Fit in Thin Environments
- ESD Protected
- This is a Pb−Free Device

Applications

- Optimized for Battery and Load Management Applications in Portable Equipment
- Load Switch
- Level Shift Circuits
- DC−DC Converters

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	20	V
Gate−to−Source Voltage			V_{GS}	±8.0	V
N−Channel Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	3.8	A
		T_A = 85°C		2.7	
	t ≤ 5 s	T_A = 25°C		4.7	
P−Channel Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	−3.2	A
		T_A = 85°C		−2.3	
	t ≤ 5 s	T_A = 25°C		−4.0	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.5	W
	t ≤ 5 s			2.3	
N−Channel Continuous Drain Current (Note 2)	Steady State	T_A = 25°C	I_D	2.6	A
		T_A = 85°C		1.9	
P−Channel Continuous Drain Current (Note 2)	Steady State	T_A = 25°C	I_D	−2.2	A
		T_A = 85°C		−1.6	
Power Dissipation (Note 2)	Steady State	T_A = 25°C	P_D	0.71	W
Pulsed Drain Current	N−Ch	t_p = 10 μs	I_{DM}	18	A
	P−Ch			−16	
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

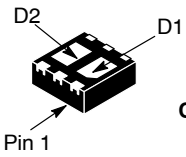
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface Mounted on FR4 Board using the minimum recommended pad size of 30 mm^2, 2 oz Cu.

ON Semiconductor®

www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
N−Channel 20 V	68 mΩ @ 4.5 V	4.7 A
	86 mΩ @ 2.5 V	4.2 A
	120 mΩ @ 1.8 V	3.5 A
P−Channel −20 V	100 mΩ @ −4.5 V	−4.0 A
	144 mΩ @ −2.5 V	−3.3 A
	200 mΩ @ −1.8 V	−2.8 A

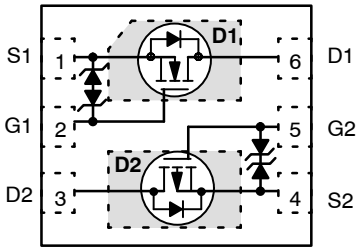


WDFN6
CASE 506AN

MARKING DIAGRAM

JN = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NTLJD3183CZTAG	WDFN6 (Pb−Free)	3000/Tape & Reel
NTLJD3183CZTBG	WDFN6 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
SINGLE OPERATION (SELF−HEATED)			
Junction−to−Ambient − Steady State (Note 3)	$R_{\theta JA}$	83	°C/W
Junction−to−Ambient − Steady State Min Pad (Note 4)	$R_{\theta JA}$	177	
Junction−to−Ambient − t ≤ 5 s (Note 3)	$R_{\theta JA}$	54	
DUAL OPERATION (EQUALLY HEATED)			
Junction−to−Ambient − Steady State (Note 3)	$R_{\theta JA}$	58	°C/W
Junction−to−Ambient − Steady State Min Pad (Note 4)	$R_{\theta JA}$	133	
Junction−to−Ambient − t ≤ 5 s (Note 3)	$R_{\theta JA}$	40	

3. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
4. Surface Mounted on FR4 Board using the minimum recommended pad size (30 mm^2, 2 oz Cu).

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions		Min	Typ	Max	Unit
OFF CHARACTERISTICS								
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	N	V_{GS} = 0 V	I_D = 250 μA	20			V
		P		I_D = −250 μA	−20			
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	N	Ref to 25°C	I_D = 250 μA		15		mV/°C
		P		I_D = −250 μA		13		
Zero Gate Voltage Drain Current	I_{DSS}	N	V_{GS} = 0 V, V_{DS} = 16 V	T_J = 25°C			1.0	μA
		P	V_{GS} = 0 V, V_{DS} = −16 V				−1.0	
		N	V_{GS} = 0 V, V_{DS} = 16 V	T_J = 85°C			10	
		P	V_{GS} = 0 V, V_{DS} = −16 V				−10	
Gate−to−Source Leakage Current	I_{GSS}	N	V_{DS} = 0 V, V_{GS} = ±8.0 V				±10	μA
		P					±10	
ON CHARACTERISTICS (Note 5)								
Gate Threshold Voltage	$V_{GS(TH)}$	N	V_{GS} = V_{DS}	I_D = 250 μA	0.4		1.0	V
		P		I_D = −250 μA	−0.4		−1.0	
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	N	Ref to 25°C	I_D = 250 μA		−3.0		mV/°C
		P		I_D = −250 μA		2.0		
Drain−to−Source On Resistance	$R_{DS(on)}$	N	V_{GS} = 4.5 V , I_D = 2.0 A			34	68	mΩ
		P	V_{GS} = −4.5 V , I_D = −2.0 A			68	100	
		N	V_{GS} = 2.5 V , I_D = 2.0 A			42	86	
		P	V_{GS} = −2.5 V, I_D = −2.0 A			90	144	
		N	V_{GS} = 1.8 V , I_D = 1.7 A			53	120	
		P	V_{GS} = −1.8 V, I_D = −1.7 A			125	200	
Forward Transconductance	g_{FS}	N	V_{DS} = 5.0 V, I_D = 2.0 A			7.0		S
		P	V_{DS} = −5.0 V , I_D = −2.0 A			6.5		

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions		Min	Typ	Max	Unit
CHARGES, CAPACITANCES AND GATE RESISTANCE								
Input Capacitance	C_{ISS}	N	f = 1.0 MHz, V_{GS} = 0 V	V_{DS} = 10 V		355		pF
		P		V_{DS} = −10 V		450		
Output Capacitance	C_{OSS}	N		V_{DS} = 10 V		70		
		P		V_{DS} = −10 V		90		
Reverse Transfer Capacitance	C_{RSS}	N		V_{DS} = 10 V		50		
		P		V_{DS} = −10 V		62		
Total Gate Charge	$Q_{G(TOT)}$	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 3.8 A			4.6	7.0	nC
		P	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −3.8 A			5.2	7.8	
Threshold Gate Charge	$Q_{G(TH)}$	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 3.8 A			0.3		
		P	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −3.8 A			0.3		
Gate−to−Source Charge	Q_{GS}	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 3.8 A			0.6		
		P	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −3.8 A			0.84		
Gate−to−Drain Charge	Q_{GD}	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 3.8 A			1.15		
		P	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −3.8 A			1.5		
SWITCHING CHARACTERISTICS (Note 6)								
Turn−On Delay Time	$t_{d(ON)}$	N	V_{GS} = 4.5 V, V_{DD} = 5 V, I_D = 2.0 A, R_G = 2.0 Ω			6.2		ns
Rise Time	t_r					5.5		
Turn−Off Delay Time	$t_{d(OFF)}$					15		
Fall Time	t_f					14		
Turn−On Delay Time	$t_{d(ON)}$	P	V_{GS} = −4.5 V, V_{DD} = −5 V, I_D = −2.0 A, R_G = 2.0 Ω			6.6		
Rise Time	t_r					9.0		
Turn−Off Delay Time	$t_{d(OFF)}$					14		
Fall Time	t_f					12.5		
DRAIN−SOURCE DIODE CHARACTERISTICS								
Forward Diode Voltage	V_{SD}	N	V_{GS} = 0 V, T_J = 25 °C	I_S = 1.0 A		0.65	1.0	V
		P		I_S = −1.0 A		−0.73	−1.0	
		N	V_{GS} = 0 V, T_J = 125 °C	I_S = 1.0 A		0.55		
		P		I_S = −1.0 A		−0.62		
Reverse Recovery Time	t_{RR}	N	V_{GS} = 0 V, dI_S / dt = 100 A/μs	I_S = 1.0 A		21		ns
		P		I_S = −1.0 A		23		
Charge Time	t_a	N		I_S = 1.0 A		10.5		
		P		I_S = −1.0 A		13		
Discharge Time	t_b	N		I_S = 1.0 A		10.5		
		P		I_S = −1.0 A		10		
Reverse Recovery Charge	Q_{RR}	N		I_S = 1.0 A		7.0		nC
		P		I_S = −1.0 A		10		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

N−CHANNEL TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

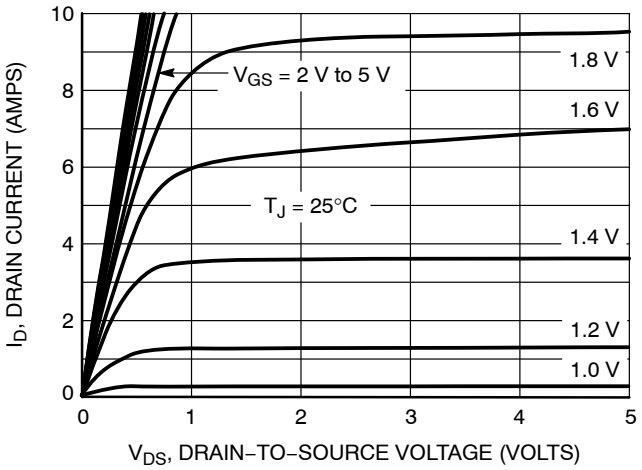


Figure 1. On−Region Characteristics

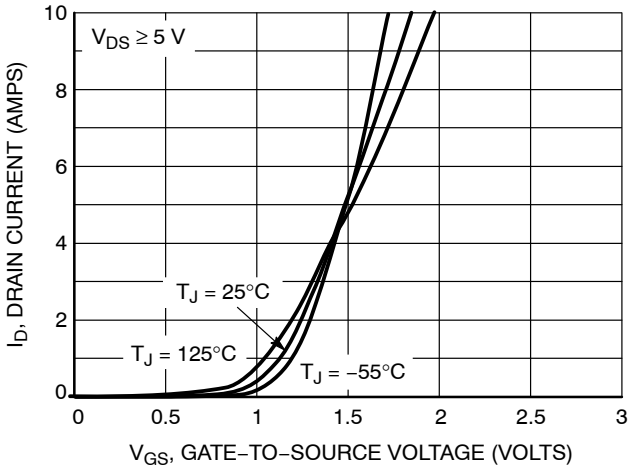


Figure 2. Transfer Characteristics

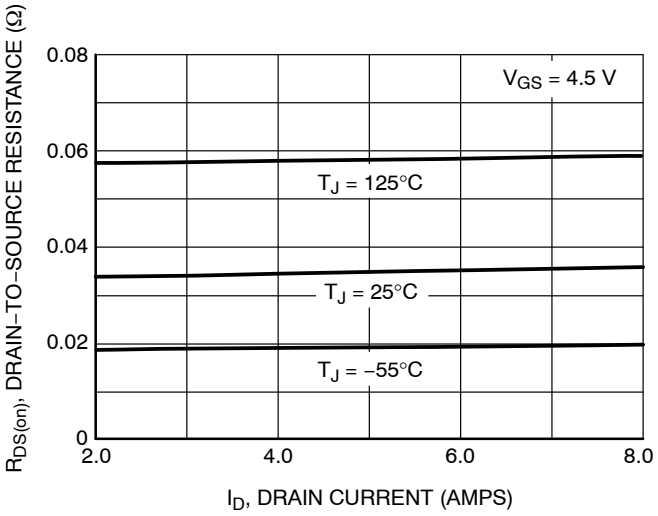


Figure 3. On−Resistance versus Drain Current

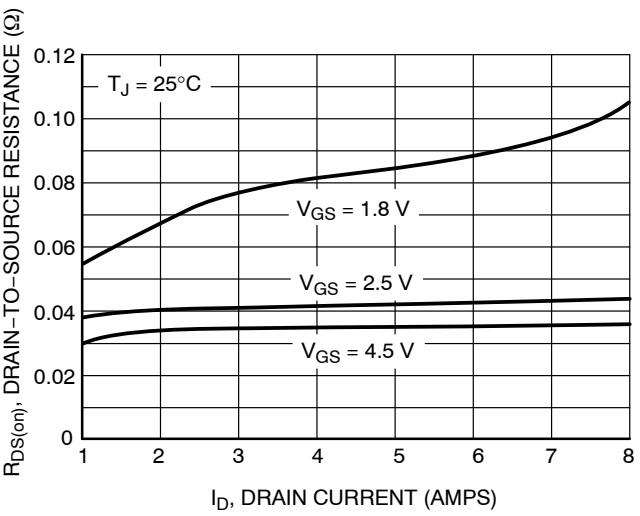


Figure 4. On−Resistance versus Drain Current and Gate Voltage

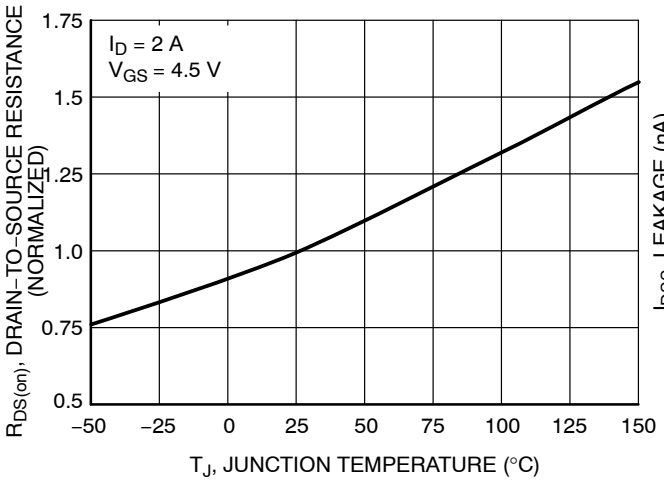


Figure 5. On−Resistance Variation with Temperature

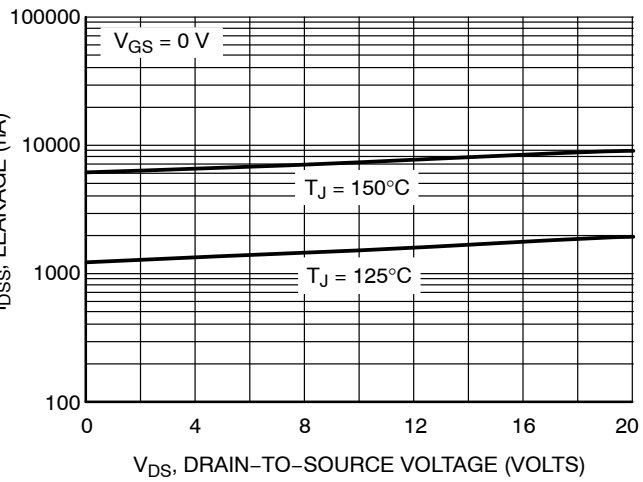


Figure 6. Drain−to−Source Leakage Current versus Voltage

N−CHANNEL TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

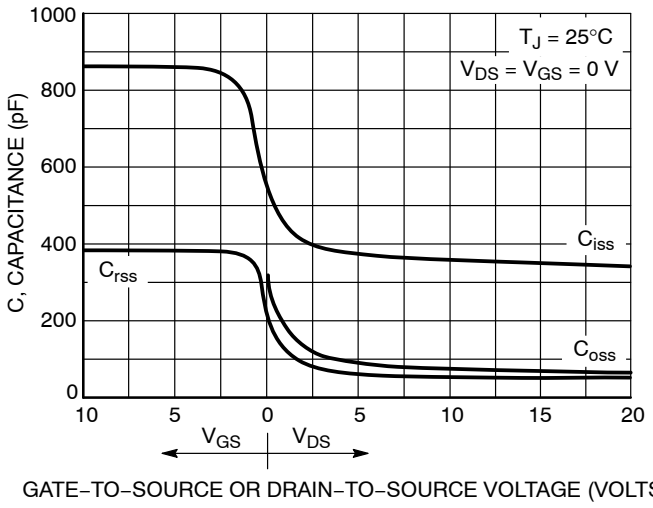


Figure 7. Capacitance Variation

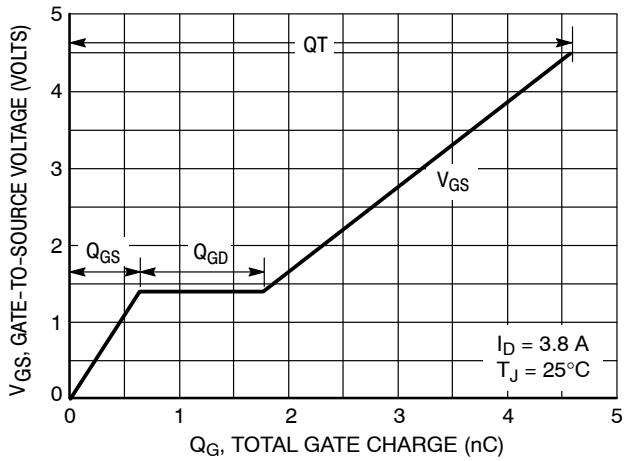


Figure 8. Gate−To−Source and Drain−To−Source Voltage versus Total Charge

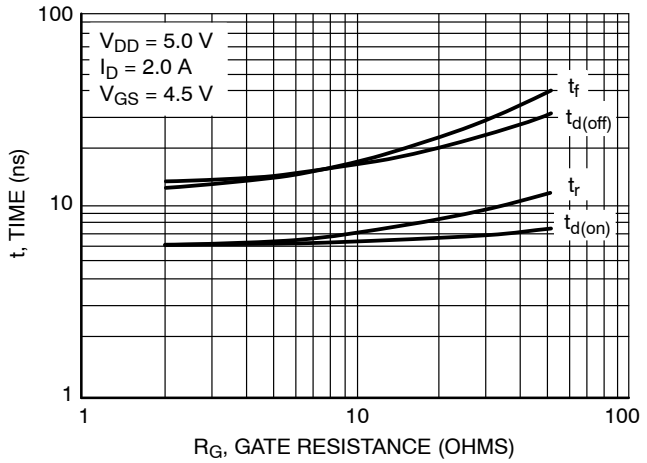


Figure 9. Resistive Switching Time Variation versus Gate Resistance

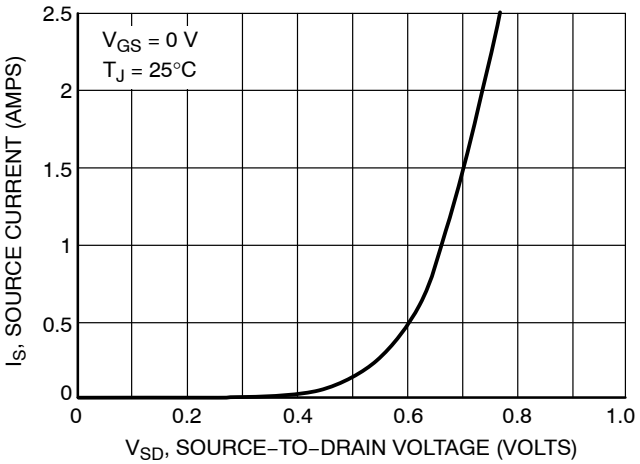


Figure 10. Diode Forward Voltage versus Current

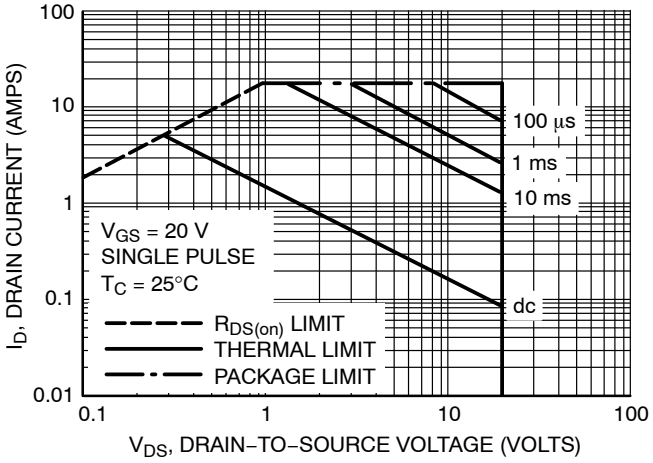


Figure 11. Maximum Rated Forward Biased Safe Operating Area

P−CHANNEL TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

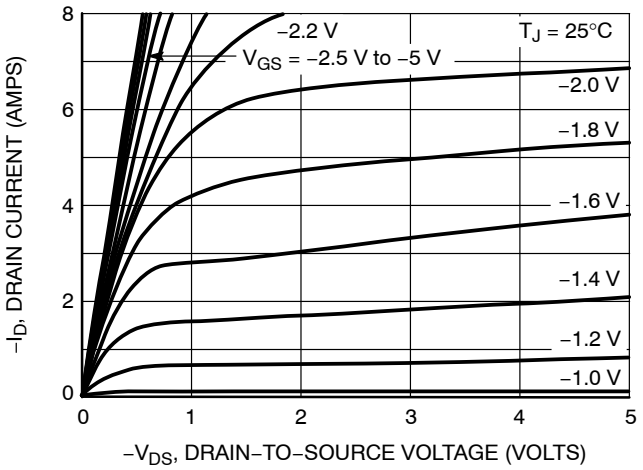


Figure 12. On−Region Characteristics

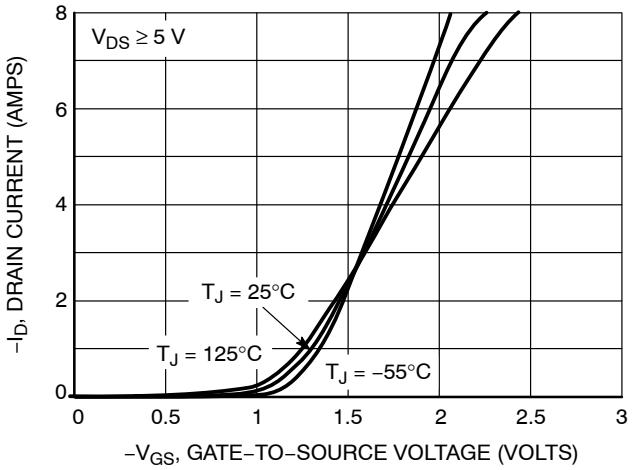


Figure 13. Transfer Characteristics

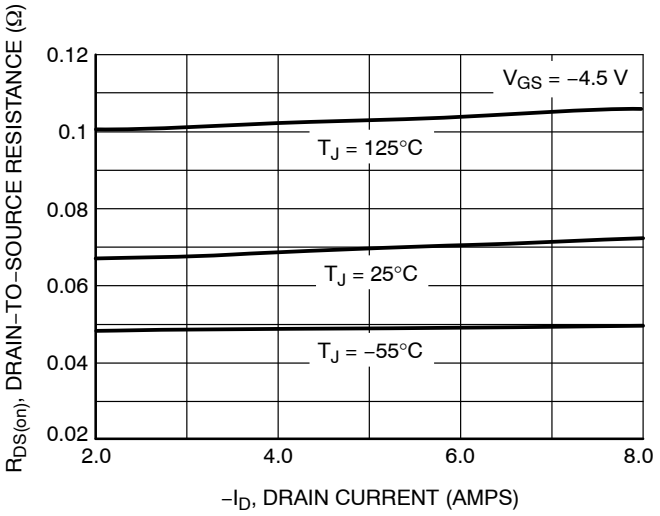


Figure 14. On−Resistance versus Drain Current

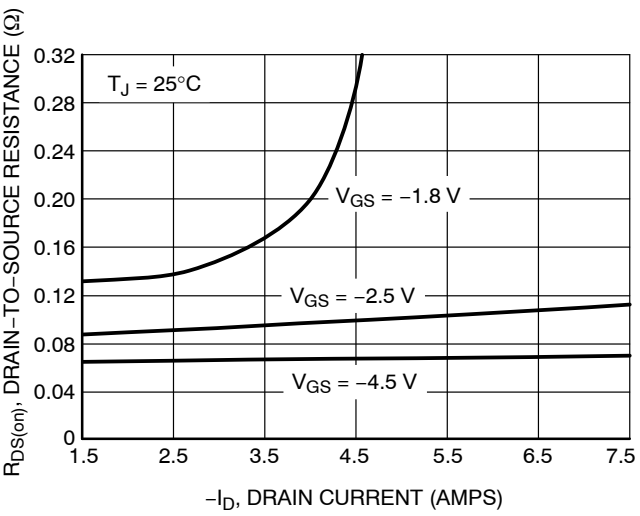


Figure 15. On−Resistance versus Drain Current and Gate Voltage

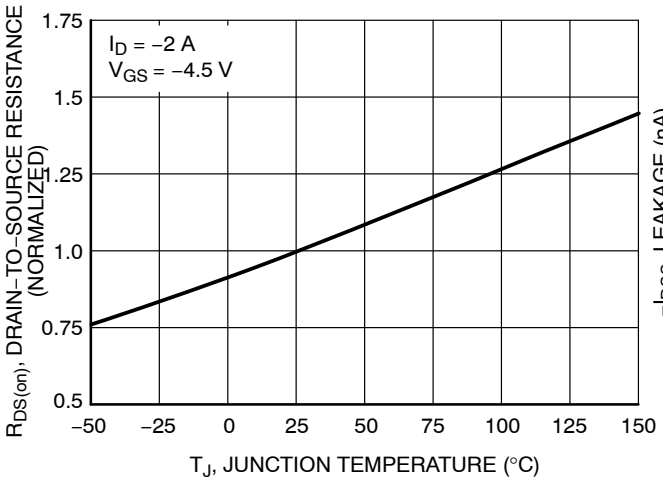


Figure 16. On−Resistance Variation with Temperature

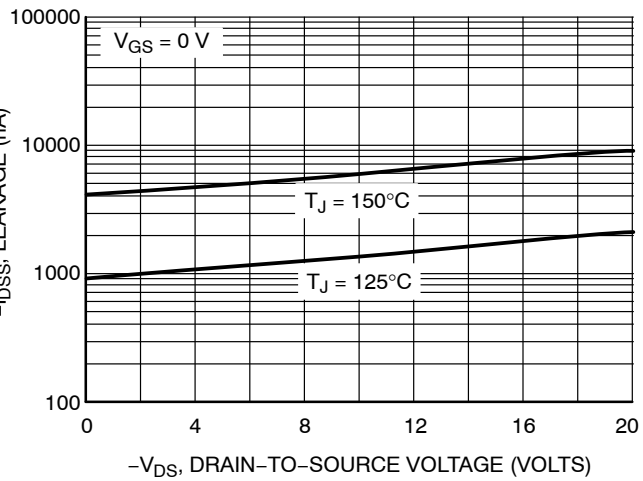


Figure 17. Drain−to−Source Leakage Current versus Voltage

P−CHANNEL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

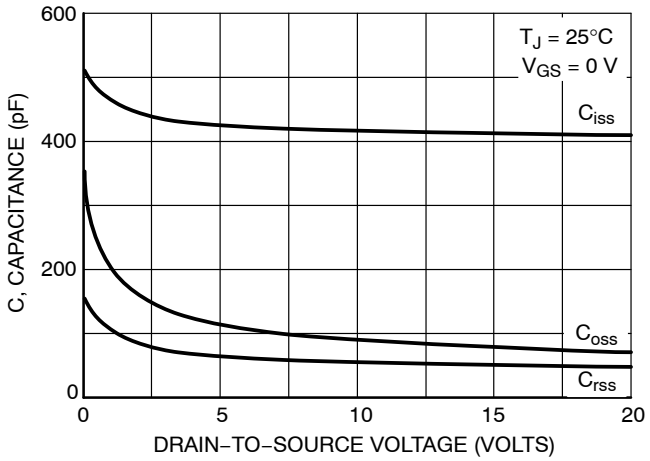


Figure 18. Capacitance Variation

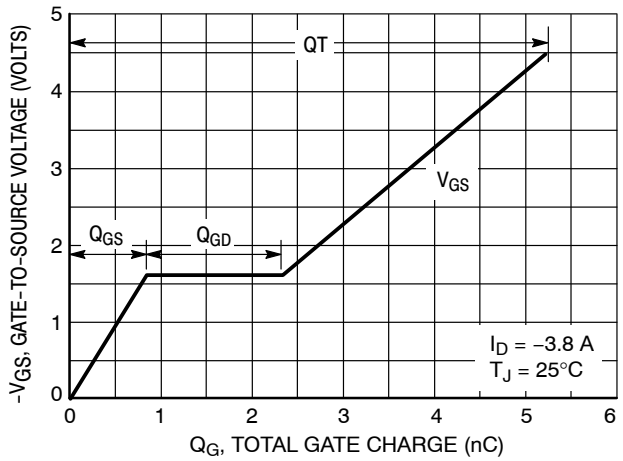


Figure 19. Gate−To−Source and Drain−To−Source Voltage versus Total Charge

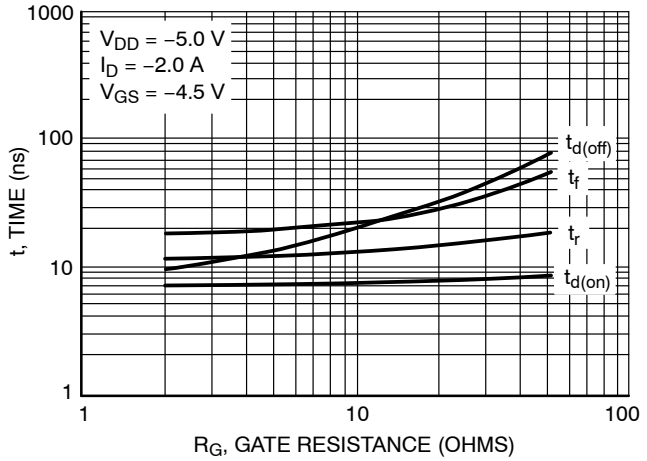


Figure 20. Resistive Switching Time Variation versus Gate Resistance

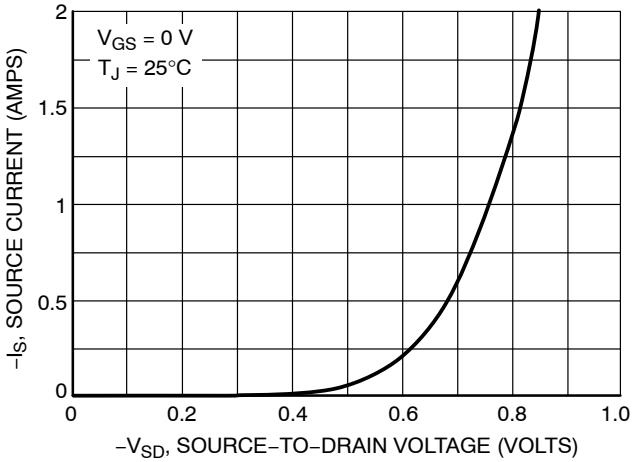


Figure 21. Diode Forward Voltage versus Current

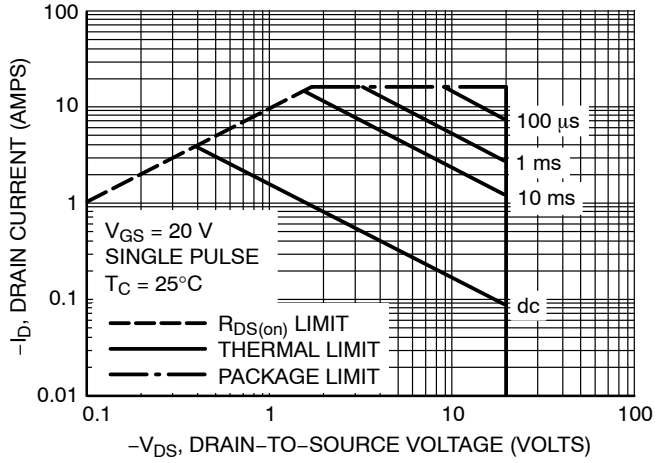


Figure 22. Maximum Rated Forward Biased Safe Operating Area

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

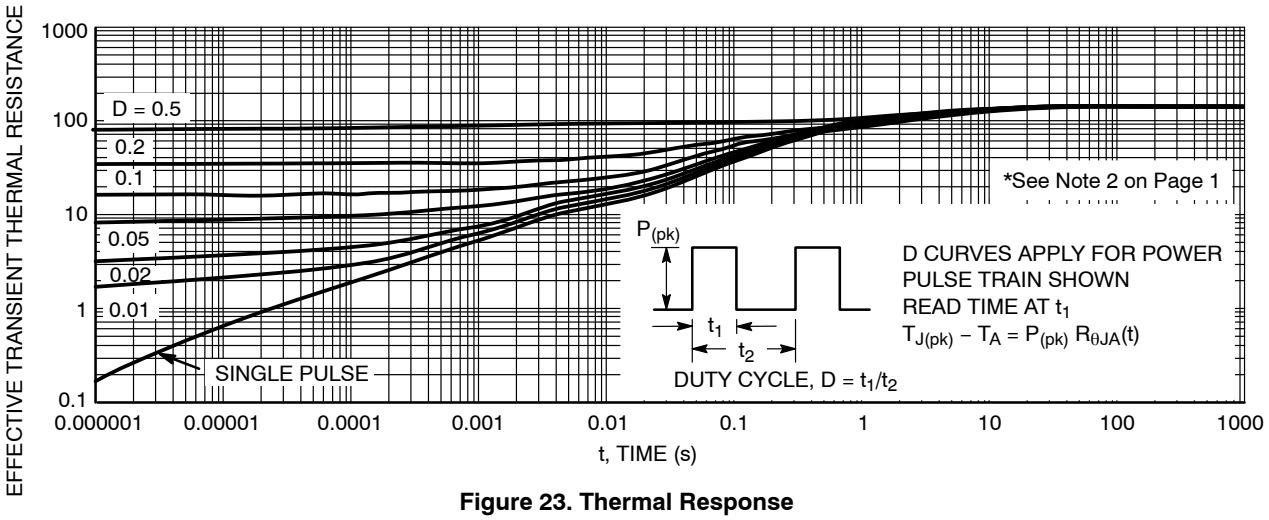
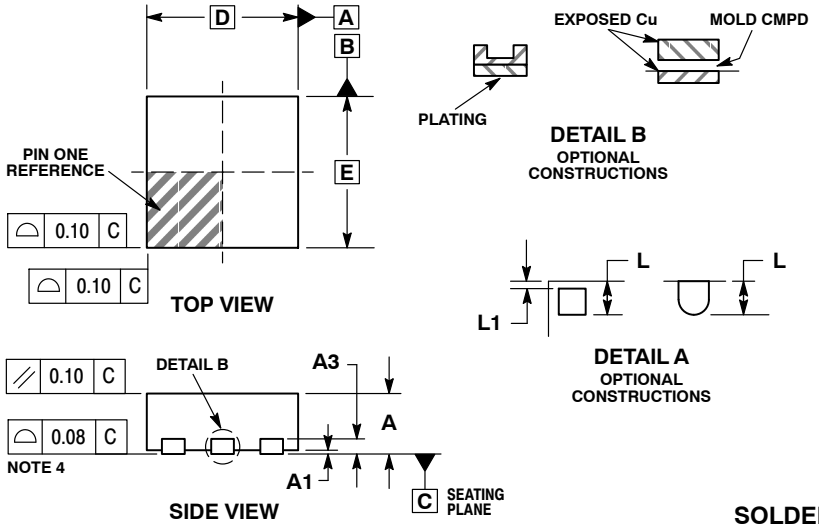


Figure 23. Thermal Response

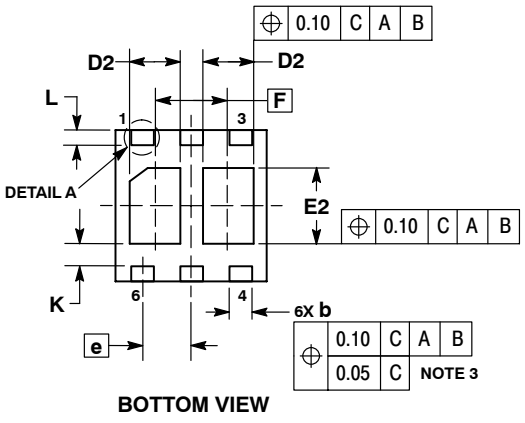
PACKAGE DIMENSIONS

WDFN6 2x2, 0.65P
CASE 506AN
ISSUE G

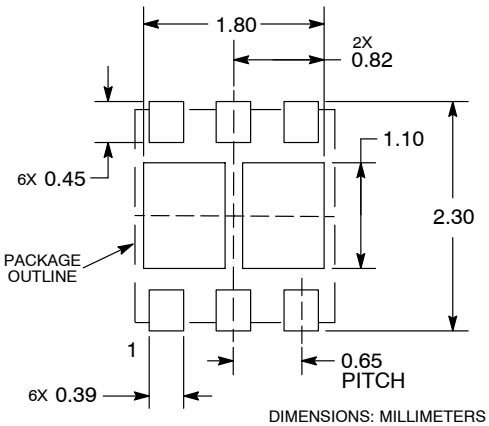


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
F	0.95 BSC	
K	0.25 REF	
L	0.20	0.30
L1	---	0.10



SOLDERMASK DEFINED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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