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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



NTLJS4149P

Power MOSFET

-30 V, -5.9 A, μ Cool™ Single P-Channel, 2x2 mm, WDFN Package

Features

- WDFN Package with Exposed Drain Pad for Excellent Thermal Conduction
- 2x2 mm Footprint Same as SC-88 Package
- Low Profile (< 0.8 mm) for Easy Fit in Thin Environments
- This is a Pb-Free Device

Applications

- Li Ion Battery Linear Mode Charging for Portable Power Management in Noisy Environment
- DC-DC Conversion Buck/Boost Circuits
- High Side Switching

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V _{DSS}	-30	V	
Gate-to-Source Voltage		V _{GS}	±12	V	
Continuous Drain Current (Note 1)	Steady State	I _D	T _A = 25°C	-4.5	A
			T _A = 85°C	-3.3	
	t ≤ 5 s	T _A = 25°C	-5.9		
Power Dissipation (Note 1)	Steady State	P _D	T _A = 25°C	1.9	W
			t ≤ 5 s	3.2	
Continuous Drain Current (Note 2)	Steady State	I _D	T _A = 25°C	-2.7	A
			T _A = 85°C	-2.0	
			T _A = 25°C	0.7	
Power Dissipation (Note 2)		P _D	0.7	W	
Pulsed Drain Current	t _p = 10 μs	I _{DM}	-18	A	
Operating Junction and Storage Temperature		T _J , T _{STG}	-55 to 150	°C	
Source Current (Body Diode) (Note 2)		I _S	-1.5	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T _L	260	°C	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

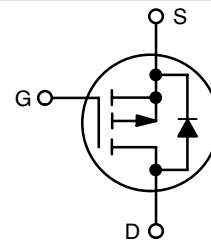
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface Mounted on FR4 Board using the minimum recommended pad size.



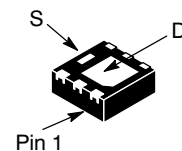
ON Semiconductor®

<http://onsemi.com>

V _{(BR)DSS}	R _{DS(on)} MAX
-30 V	62 mΩ @ -4.5 V
	75 mΩ @ -2.5 V

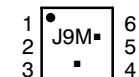


P-CHANNEL MOSFET



MARKING DIAGRAM

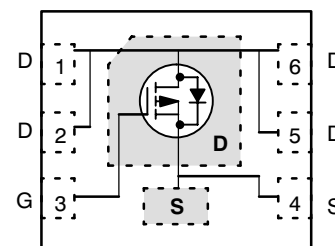
WDFN6
CASE 506AP



- J9 = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NTLJS4149PTAG	WDFN6 (Pb-Free)	3000/Tape & Reel
NTLJS4149PTBG	WDFN6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTLJS4149P

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	65	°C/W
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	38	
Junction-to-Ambient – Steady State Min Pad (Note 4)	$R_{\theta JA}$	180	

3. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
 4. Surface Mounted on FR4 Board using the minimum recommended pad size.

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = -250$ μ A	-30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250$ μ A, Ref to 25°C		-1.8		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24$ V, $V_{GS} = 0$ V		-0.1	-1.0	μ A
				-1.0	-10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 12$ V			± 0.1	μ A

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = -250$ μ A	-0.4		-1.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			3.1		mV/°C
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -4.5$ V, $I_D = -2.0$ A		43	62	m Ω
		$V_{GS} = -2.5$ V, $I_D = -2.0$ A		56	75	
		$V_{GS} = -4.5$ V, $I_D = -4.5$ A		43	62	
Forward Transconductance	g_{FS}	$V_{DS} = -6.0$ V, $I_D = -3.0$ A		10		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0$ V, $f = 1.0$ MHz, $V_{DS} = -15$ V		960		pF
Output Capacitance	C_{OSS}			130		
Reverse Transfer Capacitance	C_{RSS}			80		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5$ V, $V_{DS} = -15$ V, $I_D = -2.0$ A		9.9	15	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.8		
Gate-to-Source Charge	Q_{GS}			1.45		
Gate-to-Drain Charge	Q_{GD}			2.75		

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5$ V, $V_{DS} = -15$ V, $I_D = -2.0$ A, $R_G = 2.0$ Ω		6.9		ns
Rise Time	t_r			11		
Turn-Off Delay Time	$t_{d(OFF)}$			60		
Fall Time	t_f			55		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0$ V, $I_S = -1.5$ A	$T_J = 25^\circ\text{C}$	-0.75	-1.2	V
			$T_J = 85^\circ\text{C}$	-0.65		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0$ V, $dI_S/dt = 100$ A/ μ s, $I_S = -1.5$ A		35	60	ns
Charge Time	t_a			10		
Discharge Time	t_b			25		
Reverse Recovery Charge	Q_{RR}			0.016		

5. Pulse Test: Pulse Width ≤ 300 μ s, Duty Cycle $\leq 2\%$.
 6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

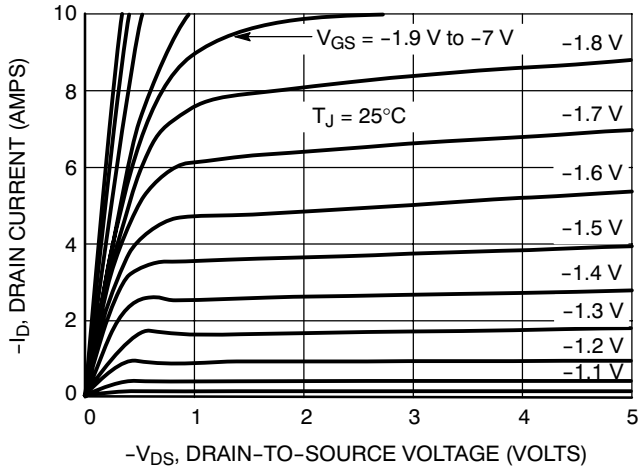


Figure 1. On-Region Characteristics

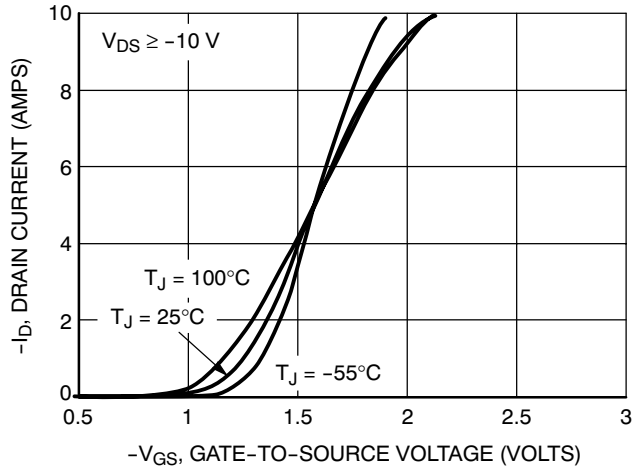


Figure 2. Transfer Characteristics

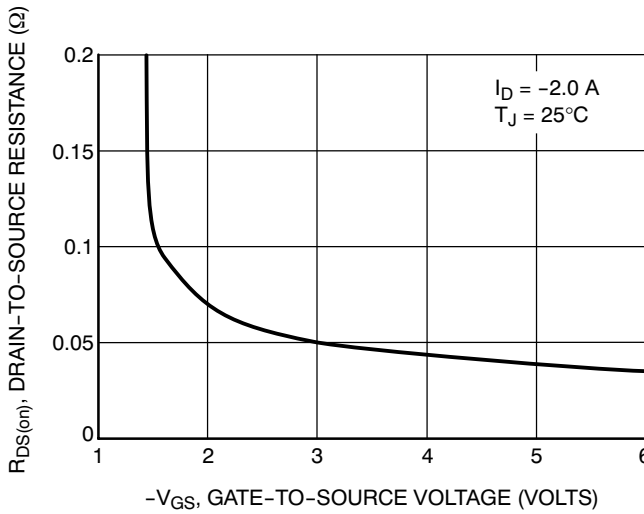


Figure 3. On-Resistance versus Gate-to-Source Voltage

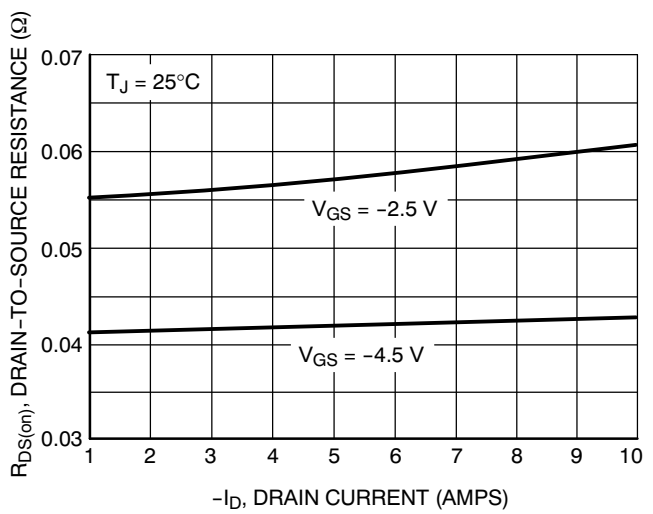


Figure 4. On-Resistance versus Drain Current and Gate Voltage

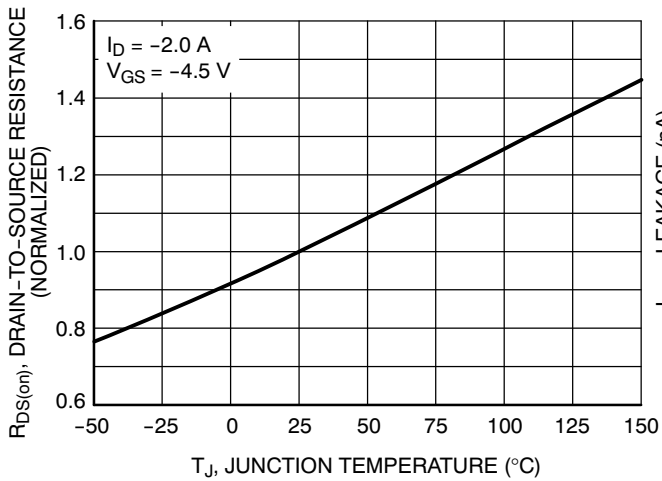


Figure 5. On-Resistance Variation with Temperature

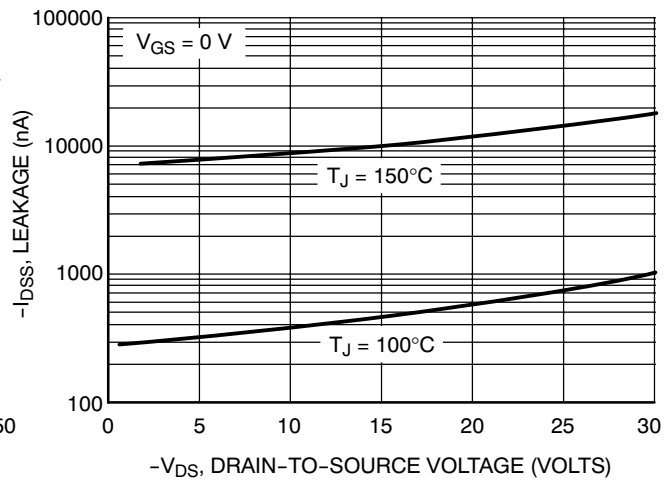


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

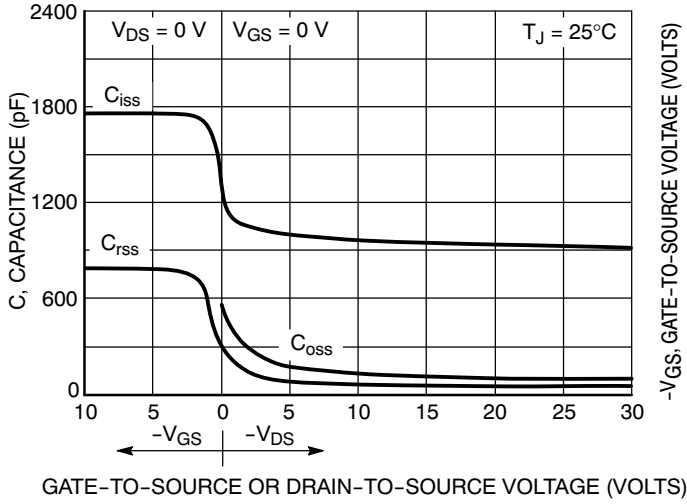


Figure 7. Capacitance Variation

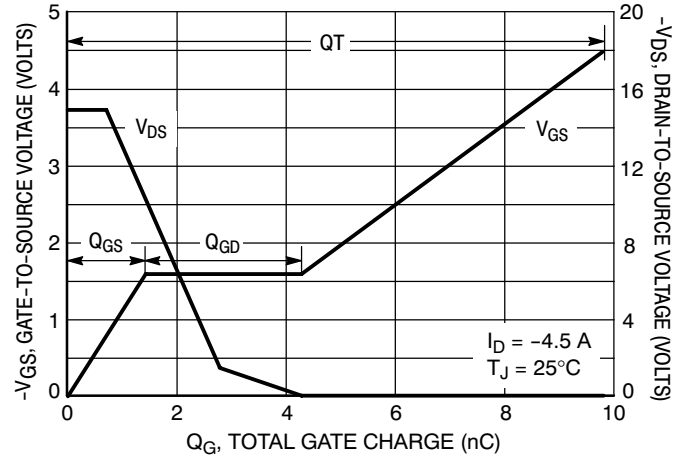


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

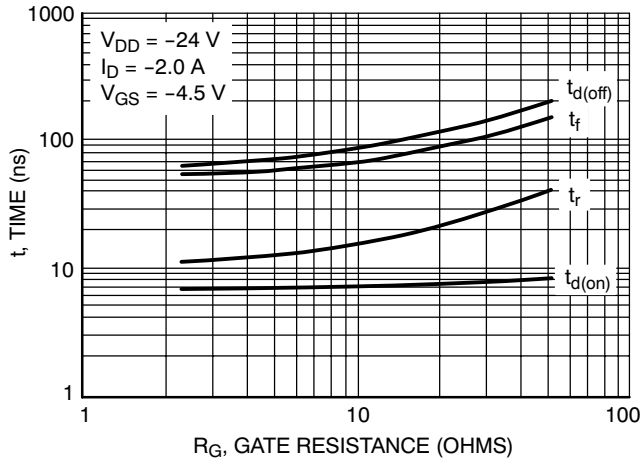


Figure 9. Resistive Switching Time Variation versus Gate Resistance

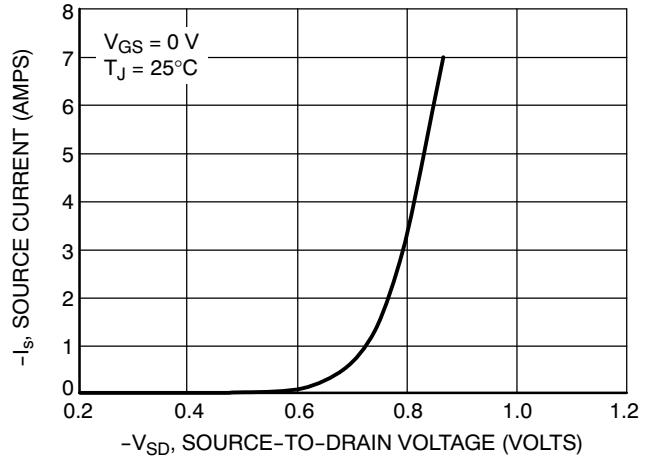
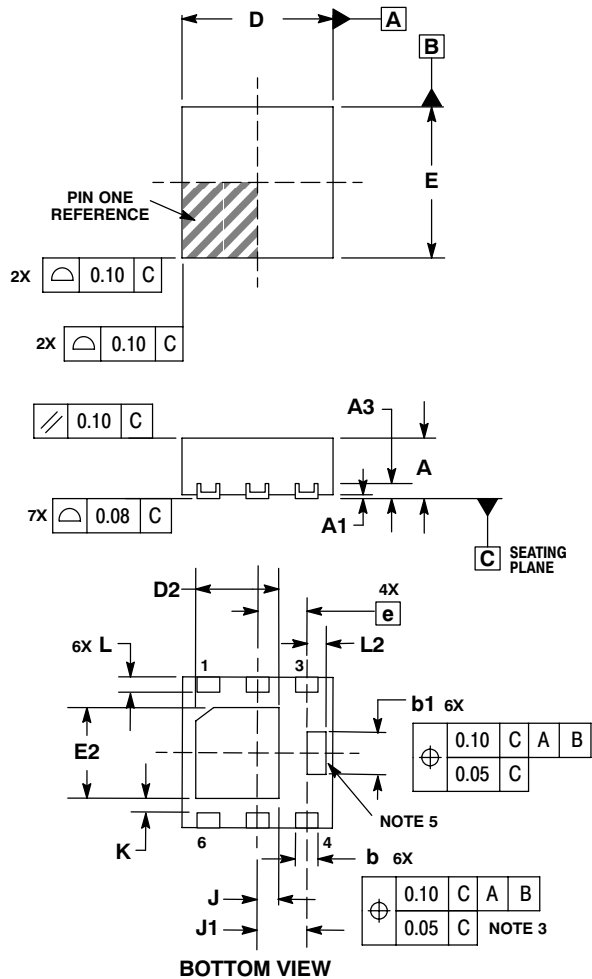


Figure 10. Diode Forward Voltage versus Current

NTLJS4149P

PACKAGE DIMENSIONS

WDFN6 2x2
CASE 506AP-01
ISSUE B

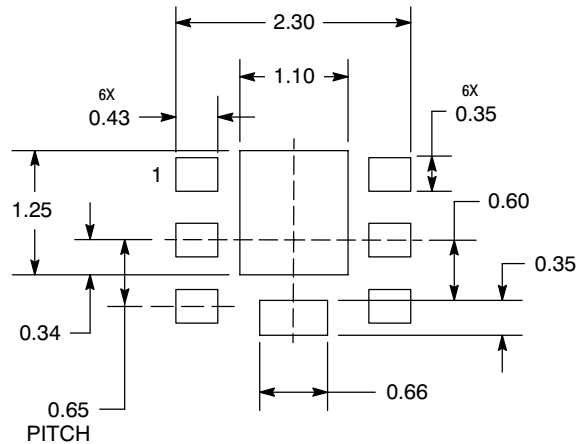


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. CENTER TERMINAL LEAD IS OPTIONAL. TERMINAL LEAD IS CONNECTED TO TERMINAL LEAD # 4.
6. PINS 1, 2, 5 AND 6 ARE TIED TO THE FLAG.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
b1	0.51	0.61
D	2.00 BSC	
D2	1.00	1.20
E	2.00 BSC	
E2	1.10	1.30
e	0.65 BSC	
K	0.15 REF	
L	0.20	0.30
L2	0.20	0.30
J	0.27 REF	
J1	0.65 REF	

SOLDERMASK DEFINED MOUNTING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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