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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



NTMFD4C88N

PowerPhase, Dual N-Channel SO8FL 30 V, High Side 20 A / Low Side 24 A

Features

- Co-Packaged Power Stage Solution to Minimize Board Space
- Minimized Parasitic Inductances
- Optimized Devices to Reduce Power Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- DC-DC Converters
- System Voltage Rails
- Point of Load

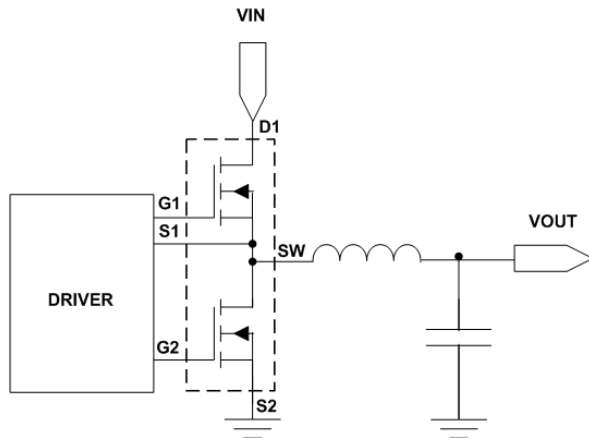


Figure 1. Typical Application Circuit

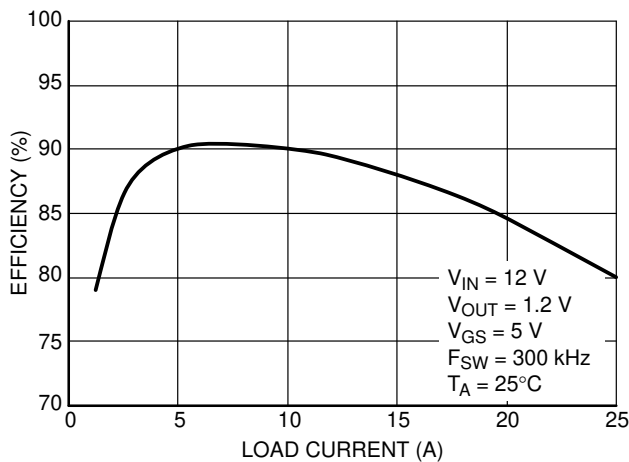


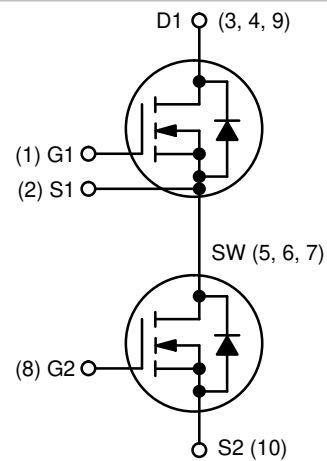
Figure 2. Typical Efficiency Performance POWERPHASEGEVB Evaluation Board



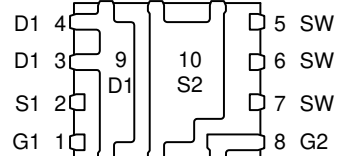
ON Semiconductor®

www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
Q1 Top FET 30 V	5.4 mΩ @ 10 V	20 A
	8.1 mΩ @ 4.5 V	
Q2 Bottom FET 30 V	4.4 mΩ @ 10 V	24 A
	6.0 mΩ @ 4.5 V	

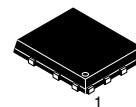


PIN CONNECTIONS

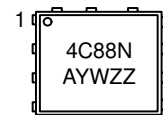


(Bottom View)

MARKING DIAGRAM



DFN8
CASE 506CR



- 4C88N = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

NTMFD4C88N

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Unit		
Drain-to-Source Voltage	Q1	V_{DSS}	30	V		
Drain-to-Source Voltage	Q2					
Gate-to-Source Voltage	Q1	V_{GS}	± 20	V		
Gate-to-Source Voltage	Q2					
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	Q1	$T_A = 25^\circ\text{C}$	15.4	A	
			$T_A = 85^\circ\text{C}$	11.1		
		Q2	$T_A = 25^\circ\text{C}$	18.7		
			$T_A = 85^\circ\text{C}$	13.5		
Power Dissipation $R_{\theta JA}$ (Note 1)	Steady State	Q1	$T_A = 25^\circ\text{C}$	P_D	1.89	W
Continuous Drain Current $R_{\theta JA} \leq 10$ s (Note 1)	Steady State	Q1	$T_A = 25^\circ\text{C}$	21.0	A	
			$T_A = 85^\circ\text{C}$	15.1		
		Q2	$T_A = 25^\circ\text{C}$	25.4		
			$T_A = 85^\circ\text{C}$	18.3		
Power Dissipation $R_{\theta JA} \leq 10$ s (Note 1)	Steady State	Q1	$T_A = 25^\circ\text{C}$	P_D	3.51	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)	Steady State	Q1	$T_A = 25^\circ\text{C}$	11.7	A	
			$T_A = 85^\circ\text{C}$	8.5		
		Q2	$T_A = 25^\circ\text{C}$	14.2		
			$T_A = 85^\circ\text{C}$	10.3		
Power Dissipation $R_{\theta JA}$ (Note 2)	Steady State	Q1	$T_A = 25^\circ\text{C}$	P_D	1.10	W
Pulsed Drain Current	Steady State	Q1	$T_A = 25^\circ\text{C}$ $t_p = 10 \mu\text{s}$	I_{DM}	160	A
					Q2	
Operating Junction and Storage Temperature		Q1	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$	
		Q2				
Source Current (Body Diode)	Steady State	Q1	I_S	10	A	
		Q2		10		
Drain to Source DV/DT			dV/dt	6	V/ns	
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}$, $V_{DD} = 50$ V, $V_{GS} = 10$ V, $L = 0.1$ mH, $R_G = 25 \Omega$)	Steady State	$I_L = 20$ A _{pk}	Q1	EAS	20	mJ
		$I_L = 24$ A _{pk}	Q2	EAS	29	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size of 100 mm².

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	66.0	°C/W
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	113.7	
Junction-to-Ambient – ($t \leq 10$ s) (Note 3)	$R_{\theta JA}$	35.6	

3. Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu.

4. Surface-mounted on FR4 board using the minimum recommended pad size of 100 mm².

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Break-down Voltage	Q1	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = 250$ μ A		30			V
	Q2				30			
Drain-to-Source Break-down Voltage Temperature Coefficient	Q1	$V_{(BR)DSS} / T_J$				18		mV / °C
	Q2					17		
Zero Gate Voltage Drain Current	Q1	I_{DSS}	$V_{GS} = 0$ V, $V_{DS} = 24$ V	$T_J = 25^\circ\text{C}$			1	μ A
				$T_J = 125^\circ\text{C}$			10	
	Q2		$V_{GS} = 0$ V, $V_{DS} = 24$ V	$T_J = 25^\circ\text{C}$			1	
Gate-to-Source Leakage Current	Q1	I_{GSS}	$V_{GS} = 0$ V, $V_{DS} = \pm 20$ V				100	nA
	Q2						100	

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	Q1	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250$ μ A		1.3		2.2	V
	Q2				1.3		2.2	
Negative Threshold Temperature Coefficient	Q1	$V_{GS(TH)} / T_J$				4.5		mV / °C
	Q2					4.6		
Drain-to-Source On Resistance	Q1	$R_{DS(on)}$	$V_{GS} = 10$ V	$I_D = 10$ A		4.3	5.4	m Ω
			$V_{GS} = 4.5$ V	$I_D = 10$ A		6.5	8.1	
	Q2		$V_{GS} = 10$ V	$I_D = 20$ A		2.8	4.4	
			$V_{GS} = 4.5$ V	$I_D = 20$ A		4.0	6.0	

CAPACITANCES

Input Capacitance	Q1	C_{ISS}	$V_{GS} = 0$ V, $f = 1$ MHz, $V_{DS} = 15$ V			1252		pF
	Q2					1546		
Output Capacitance	Q1	C_{OSS}				610		
	Q2					841		
Reverse Capacitance	Q1	C_{RSS}				126		
	Q2					39		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μ s, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit		
CHARGES, CAPACITANCES & GATE RESISTANCE									
Total Gate Charge	Q1	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 10\text{ A}$		10.9		nC		
	Q2				11				
Threshold Gate Charge	Q1	$Q_{G(TH)}$			1.2				
	Q2				1.6				
Gate-to-Source Charge	Q1	Q_{GS}			3.4				
	Q2				4.4				
Gate-to-Drain Charge	Q1	Q_{GD}			5.4				
	Q2				2.9				
Total Gate Charge	Q1	$Q_{G(TOT)}$		$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}; I_D = 10\text{ A}$		22.2			nC
	Q2					24.2			
Gate Resistance	Q1	R_G	$T_A = 25^\circ\text{C}$		1.0		Ω		
	Q2				1.0				

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	Q1	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		9.4		ns
	Q2				10.7		
Rise Time	Q1	t_r			19		
	Q2				4.8		
Turn-Off Delay Time	Q1	$t_{d(OFF)}$			16		
	Q2				19.3		
Fall Time	Q1	t_f			4.6		
	Q2				4.7		

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	Q1	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		6.8		ns
	Q2				7.5		
Rise Time	Q1	t_r			17		
	Q2				2.7		
Turn-Off Delay Time	Q1	$t_{d(OFF)}$			20.6		
	Q2				24.8		
Fall Time	Q1	t_f			2.64		
	Q2				2.88		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Voltage	Q1	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 10\text{ A}$	$T_J = 25^\circ\text{C}$		0.82	V
				$T_J = 125^\circ\text{C}$		0.64	
	Q2		$V_{GS} = 0\text{ V}, I_S = 10\text{ A}$	$T_J = 25^\circ\text{C}$		0.8	
				$T_J = 125^\circ\text{C}$		0.62	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS							
Reverse Recovery Time	Q1	t _{RR}	V _{GS} = 0 V, d _{IS} /d _t = 100 A/μs, I _S = 10 A		29		ns
	Q2				16.7		
Charge Time	Q1	t _a			14.2		
	Q2				19.5		
Discharge Time	Q1	t _b			15.0		
	Q2				36.2		
Reverse Recovery Charge	Q1	Q _{RR}			18.1		nC
	Q2				27.4		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS – Q1

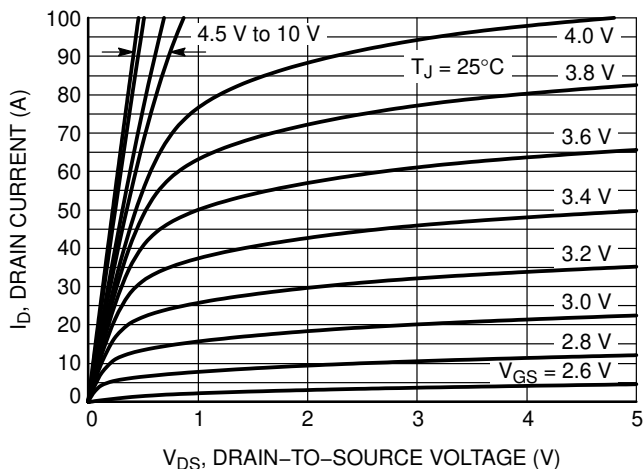


Figure 3. On-Region Characteristics

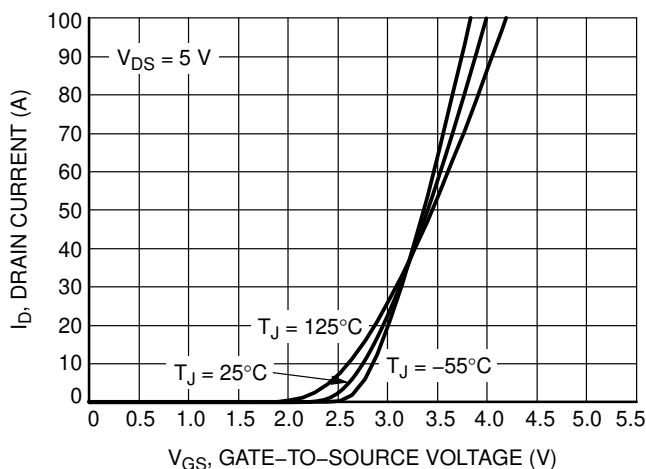


Figure 4. Transfer Characteristics

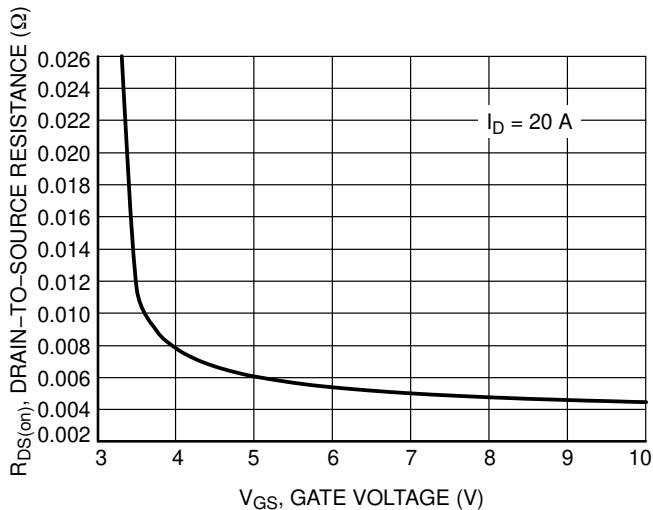


Figure 5. On-Resistance vs. Gate-to-Source Voltage

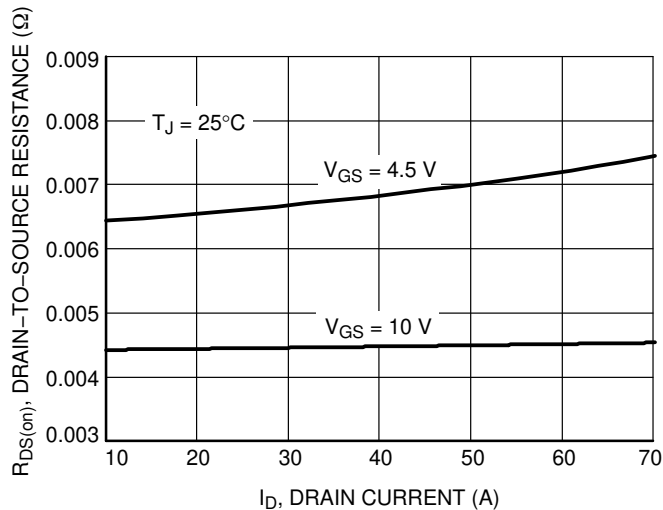


Figure 6. On-Resistance vs. Drain Current and Gate Voltage

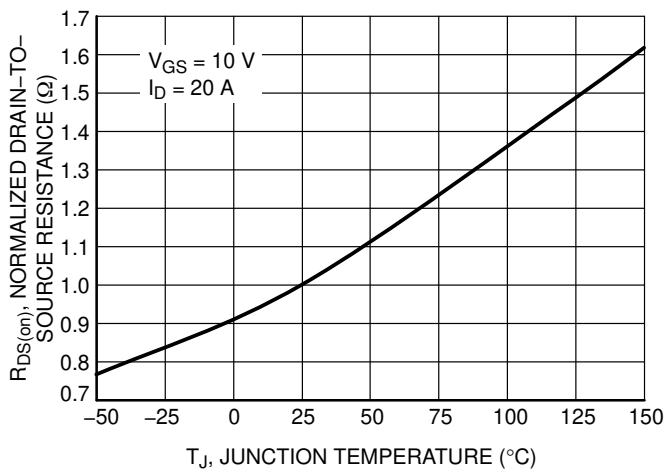


Figure 7. On-Resistance Variation with Temperature

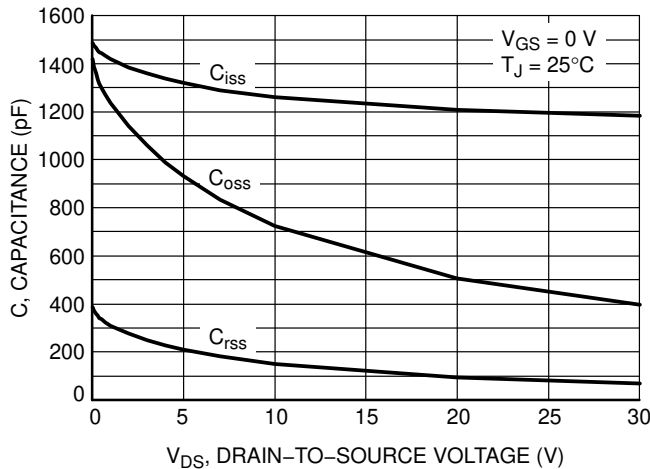


Figure 8. Capacitance Variation

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TYPICAL CHARACTERISTICS – Q1

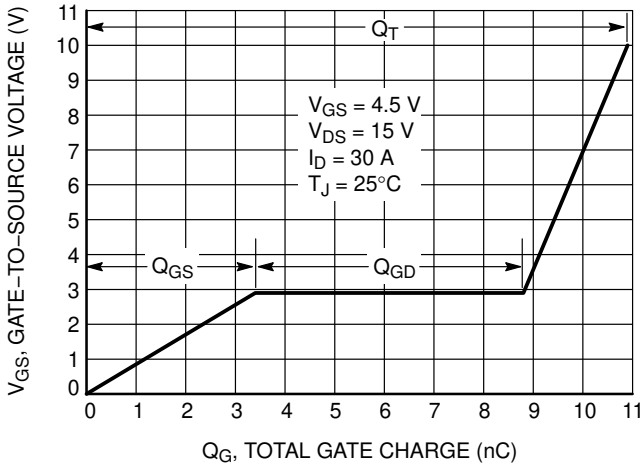


Figure 9. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

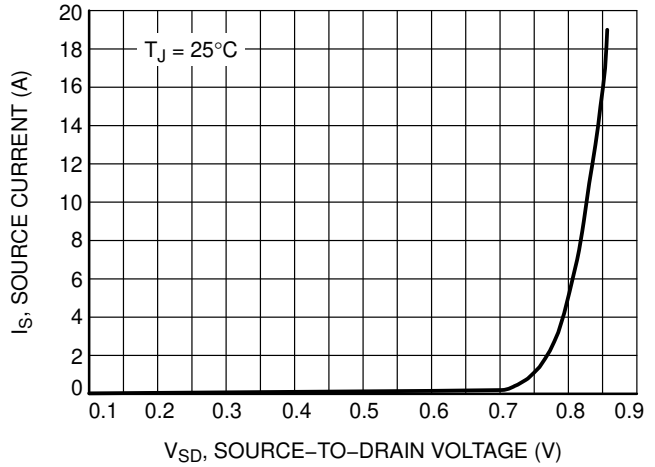


Figure 10. Diode Forward Voltage vs. Current

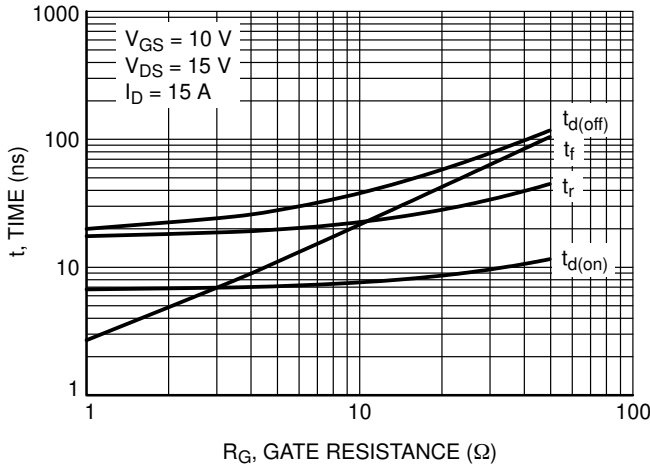


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

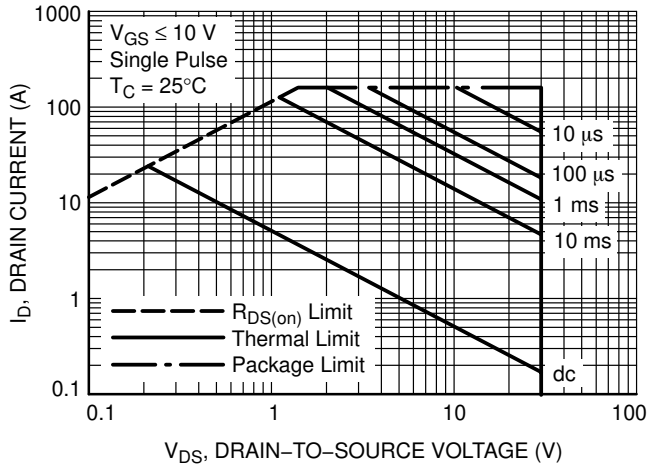


Figure 12. Maximum Rated Forward Biased Safe Operating Area

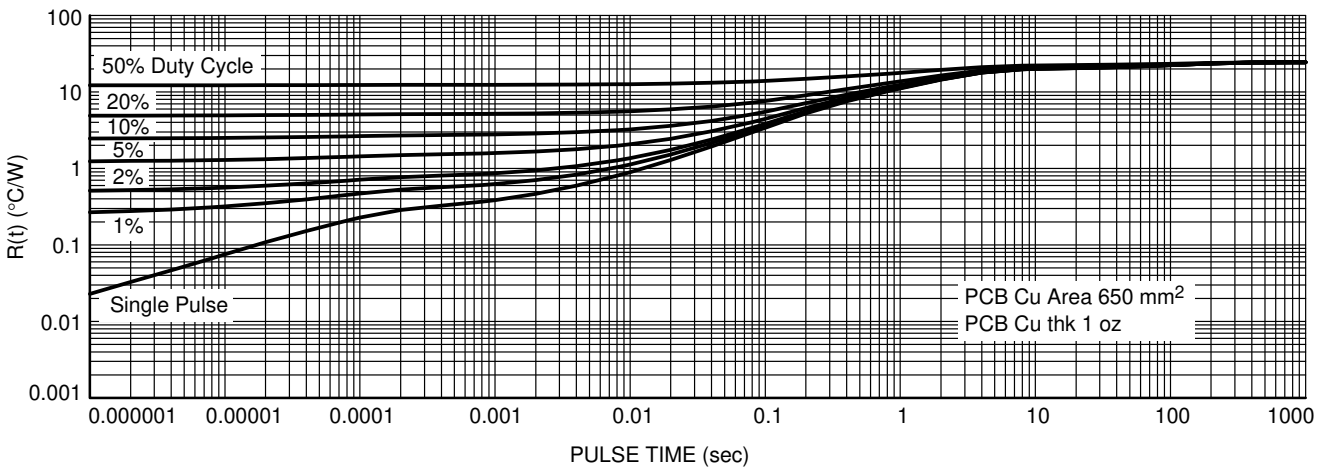


Figure 13. Thermal Characteristics

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TYPICAL CHARACTERISTICS – Q2

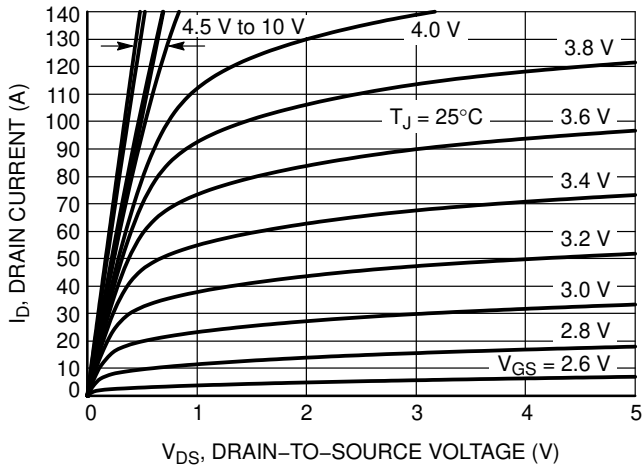


Figure 14. On-Region Characteristics

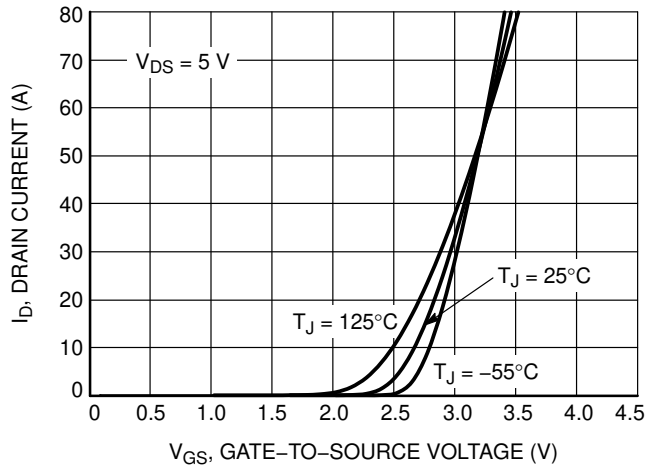


Figure 15. Transfer Characteristics

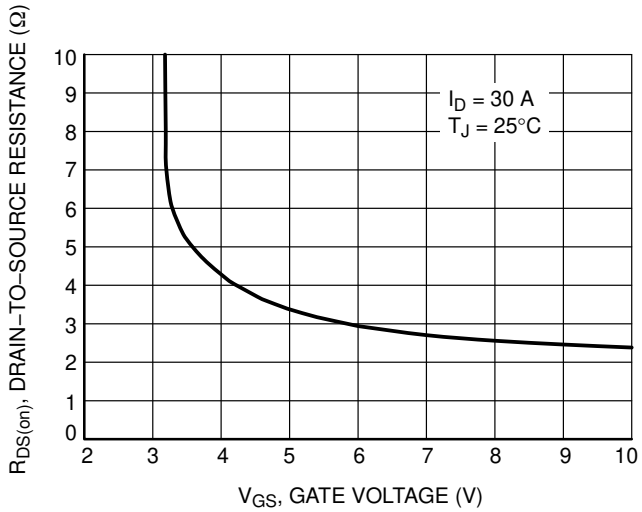


Figure 16. On-Resistance vs. Gate-to-Source Voltage

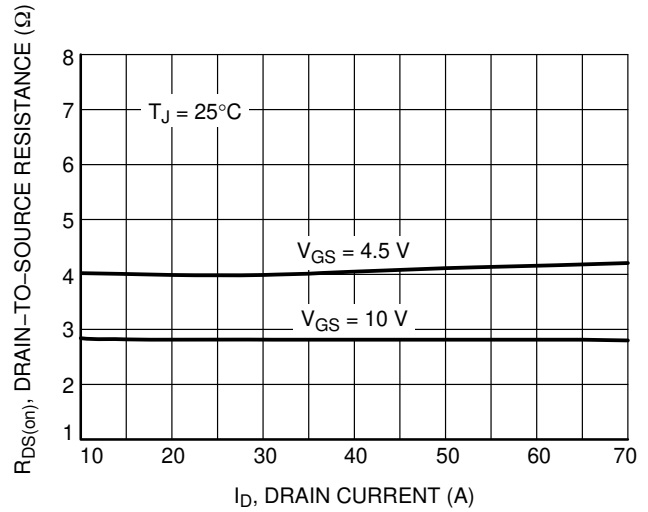


Figure 17. On-Resistance vs. Drain Current and Gate Voltage

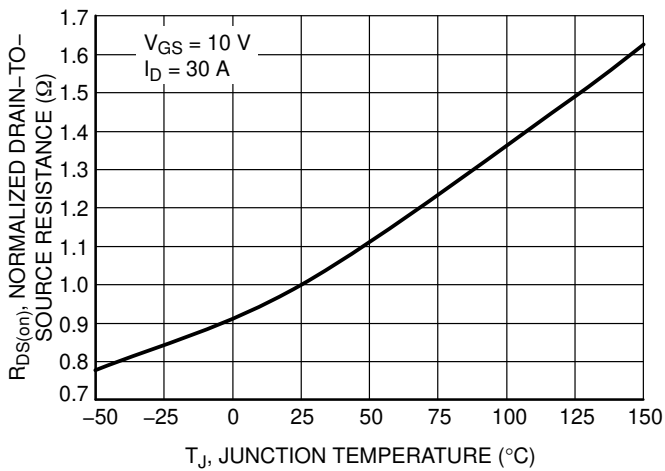


Figure 18. On-Resistance Variation with Temperature

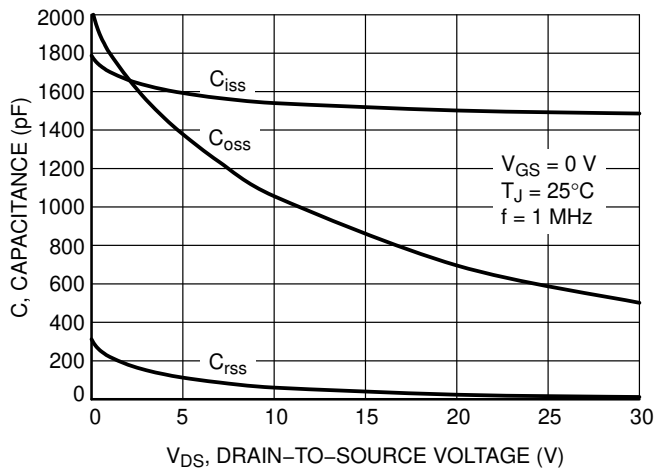


Figure 19. Capacitance Variation

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TYPICAL CHARACTERISTICS – Q2

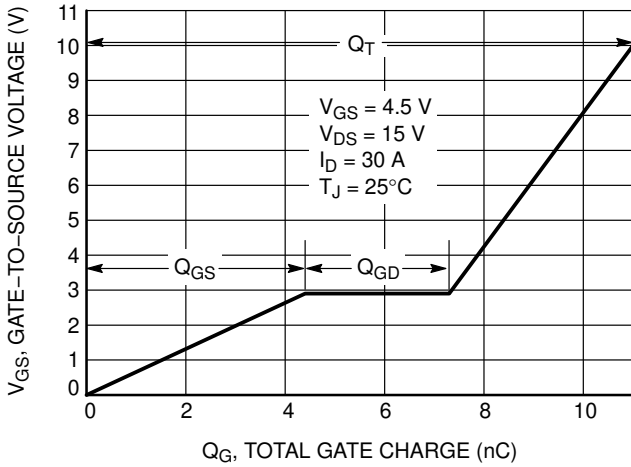


Figure 20. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

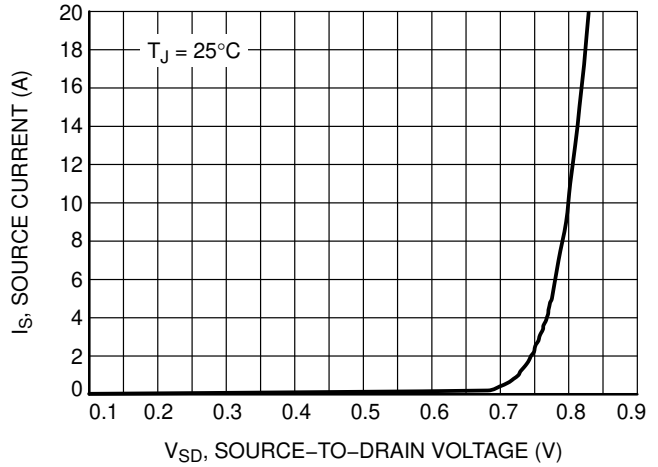


Figure 21. Diode Forward Voltage vs. Current

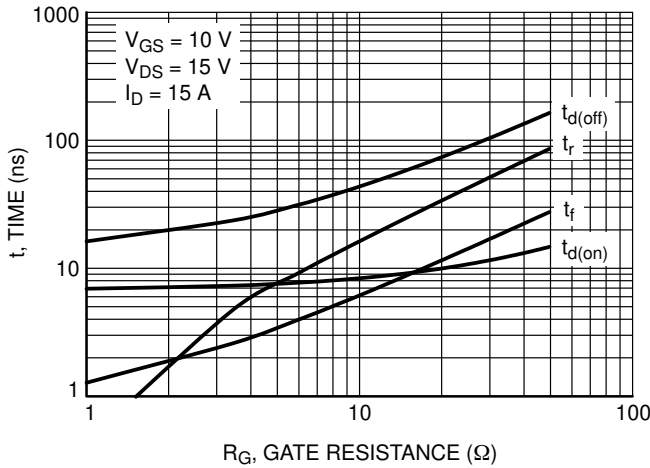


Figure 22. Resistive Switching Time Variation vs. Gate Resistance

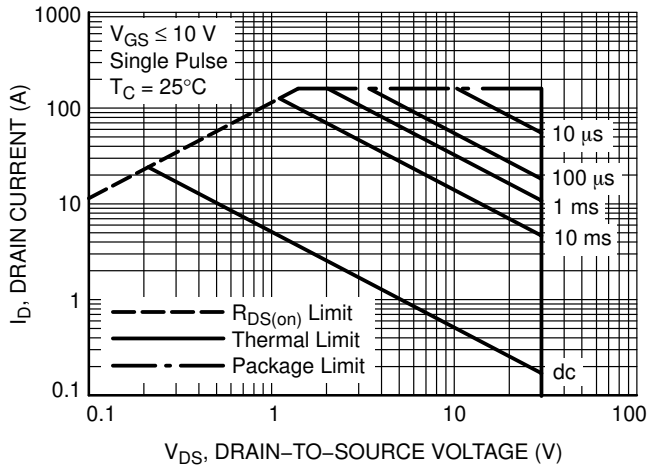


Figure 23. Maximum Rated Forward Biased Safe Operating Area

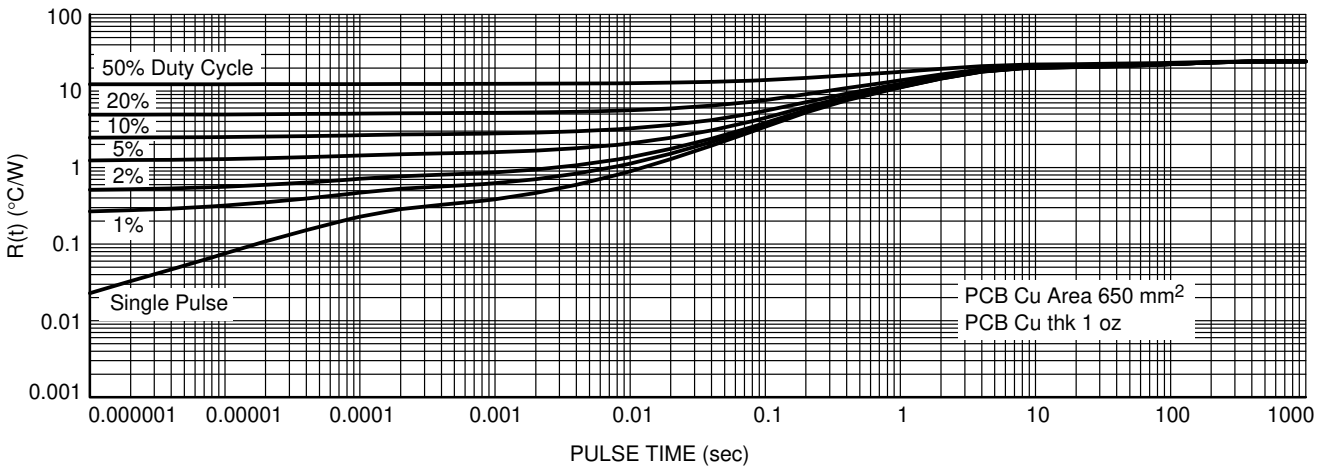


Figure 24. Thermal Characteristics

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ORDERING INFORMATION

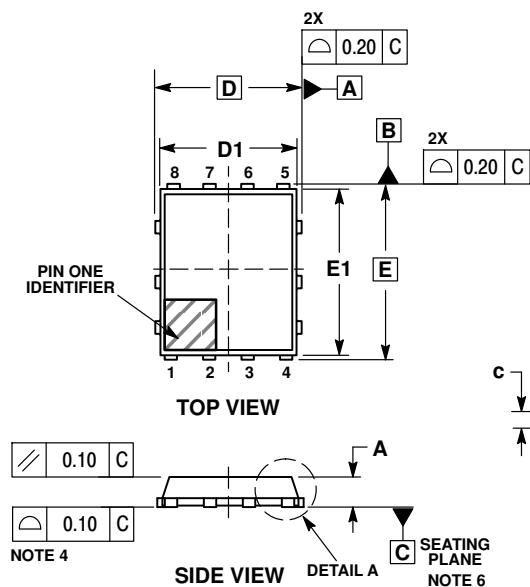
Device	Package	Shipping†
NTMFD4C88NT1G	DFN8 (Pb-Free)	1500 / Tape & Reel
NTMFD4C88NT3G	DFN8 (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

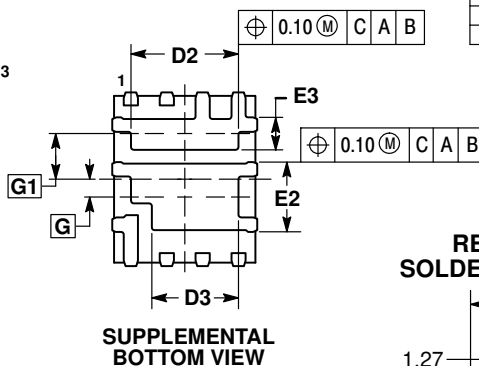
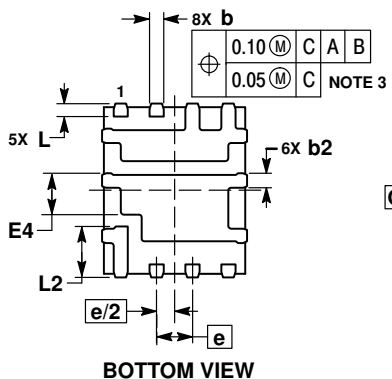
DFN8 5x6, 1.27P PowerPhase FET
CASE 506CR
ISSUE C



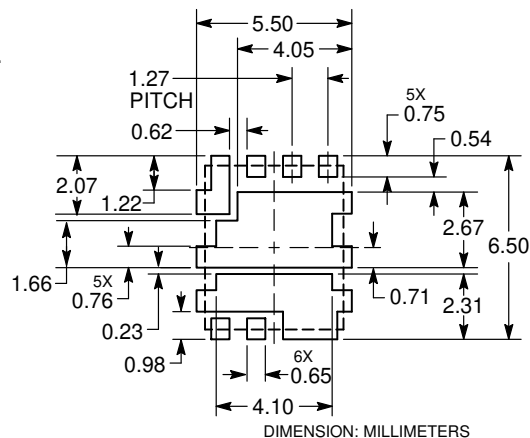
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b AND b1 APPLY TO PLATED TERMINAL AND ARE MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
A1	0.00	0.05
b	0.40	0.60
b2	0.40	0.60
c	0.20	0.30
D	5.15 BSC	
D1	4.90	5.10
D2	3.70	3.90
D3	2.96	3.16
E	6.15 BSC	
E1	5.80	6.00
E2	2.37	2.57
E3	1.05	1.25
E4	1.36	1.56
e	1.27 BSC	
G	0.625 BSC	
G1	1.615 BSC	
h	12 °	
L	0.34	0.59
L2	1.68	1.93




RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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