Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# NTMS10P02R2

# Power MOSFET
# -10 Amps, -20 Volts
## P−Channel Enhancement−Mode
## Single SOIC−8 Package

**Features**

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature SOIC−8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- SOIC−8 Mounting Information Provided
- Pb−Free Package is Available

**Applications**

- Power Management in Portable and Battery−Powered Products, i.e.: Cellular and Cordless Telephones and PCMCIA Cards

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain−to−Source Voltage | $V_{DSS}$ | −20 | Vdc |
| Gate−to−Source Voltage − Continuous | $V_{GS}$ | ±12 | Vdc |
| Thermal Resistance − Junction−to−Ambient (Note 1)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ 25°C<br>Continuous Drain Current @ 70°C<br>Maximum Operating Power Dissipation<br>Maximum Operating Drain Current<br>Pulsed Drain Current (Note 3) | $R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$P_D$<br>$I_D$<br>$I_{DM}$ | 50<br>2.5<br>−10<br>−8.0<br>0.6<br>−5.5<br>−50 | °C/W<br>W<br>A<br>A<br>W<br>A<br>A |
| Thermal Resistance − Junction−to−Ambient (Note 2)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ 25°C<br>Continuous Drain Current @ 70°C<br>Maximum Operating Power Dissipation<br>Maximum Operating Drain Current<br>Pulsed Drain Current (Note 3) | $R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$P_D$<br>$I_D$<br>$I_{DM}$ | 80<br>1.6<br>−8.8<br>−6.4<br>0.4<br>−4.5<br>−44 | °C/W<br>W<br>A<br>A<br>W<br>A<br>A |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | −55 to +150 | °C |
| Single Pulse Drain−to−Source Avalanche Energy − Starting $T_J$ = 25°C ($V_{DD}$ = −20 Vdc, $V_{GS}$ = −4.5 Vdc, Peak $I_L$ = 5.0 Apk, L = 40 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 500 | mJ |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

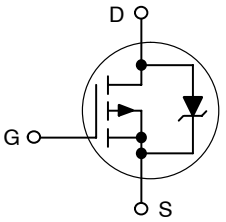
1. Mounted onto a 2″ square FR−4 Board (1 in sq, Cu 0.06″ thick single sided), t = 10 seconds.
2. Mounted onto a 2″ square FR−4 Board (1 in sq, Cu 0.06″ thick single sided), t = steady state.
3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2%.

**ON Semiconductor®**

**http://onsemi.com**

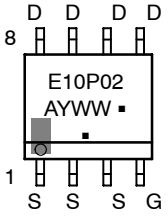
**−10 AMPERES**
**−20 VOLTS**
**14 mΩ @ $V_{GS}$ = −4.5 V**

**P−Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**


**SOIC−8**
**CASE 751**
**STYLE 12**




E10P02 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NTMS10P02R2 | SOIC−8 | 2500/Tape & Reel |
| NTMS10P02R2G | SOIC−8 (Pb−Free) | 2500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted) (Note 4)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain−to−Source Breakdown Voltage<br>($V_{GS}$ = 0 Vdc, $I_D$ = −250 μAdc)<br>Temperature Coefficient (Positive) | $V_{(BR)DSS}$ | <br>−20<br>− | <br>−<br>−12.1 | <br>−<br>− | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = −20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 25°C)<br>($V_{DS}$ = −20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 70°C) | $I_{DSS}$ | <br>−<br>− | <br>−<br>− | <br>−1.0<br>−5.0 | μAdc |
| Gate−Body Leakage Current<br>($V_{GS}$ = −12 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | − | − | −100 | nAdc |
| Gate−Body Leakage Current<br>($V_{GS}$ = +12 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | − | − | 100 | nAdc |
| **ON CHARACTERISTICS** | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = −250 μAdc)<br>Temperature Coefficient (Negative) | $V_{GS(th)}$ | <br>−0.6<br>− | <br>−0.88<br>2.8 | <br>−1.20<br>− | Vdc<br><br>mV/°C |
| Static Drain−to−Source On−State Resistance<br>($V_{GS}$ = −4.5 Vdc, $I_D$ = −10 Adc)<br>($V_{GS}$ = −2.5 Vdc, $I_D$ = −8.8 Adc) | $R_{DS(on)}$ | <br>−<br>− | <br>0.012<br>0.017 | <br>0.014<br>0.020 | Ω |
| Forward Transconductance ($V_{DS}$ = −10 Vdc, $I_D$ = −10 Adc) | $g_{FS}$ | − | 30 | − | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance | ($V_{DS}$ = −16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | − | 3100 | 3640 | pF |
| Output Capacitance | | $C_{oss}$ | − | 1100 | 1670 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | − | 475 | 1010 | |
| **SWITCHING CHARACTERISTICS** (Notes 5 & 6) | | | | | |
| Turn−On Delay Time | ($V_{DD}$ = −10 Vdc, $I_D$ = −1.0 Adc, $V_{GS}$ = −4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | − | 25 | 35 | ns |
| Rise Time | | $t_r$ | − | 40 | 65 | |
| Turn−Off Delay Time | | $t_{d(off)}$ | − | 110 | 190 | |
| Fall Time | | $t_f$ | − | 110 | 190 | |
| Turn−On Delay Time | ($V_{DD}$ = −10 Vdc, $I_D$ = −10 Adc, $V_{GS}$ = −4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | − | 25 | − | ns |
| Rise Time | | $t_r$ | − | 100 | − | |
| Turn−Off Delay Time | | $t_{d(off)}$ | − | 100 | − | |
| Fall Time | | $t_f$ | − | 125 | − | |
| Total Gate Charge | ($V_{DS}$ = −10 Vdc, $V_{GS}$ = −4.5 Vdc, $I_D$ = −10 Adc) | $Q_{tot}$ | − | 48 | 70 | nC |
| Gate−Source Charge | | $Q_{gs}$ | − | 6.5 | − | |
| Gate−Drain Charge | | $Q_{gd}$ | − | 17 | − | |
| **BODY−DRAIN DIODE RATINGS** (Note 5) | | | | | |
| Diode Forward On−Voltage | ($I_S$ = −2.1 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = −2.1 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>− | <br>−0.72<br>−0.60 | <br>−1.2<br>− | Vdc |
| Diode Forward On−Voltage | ($I_S$ = −10 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = −10 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>− | <br>−0.90<br>−0.75 | <br>−<br>− | Vdc |
| Reverse Recovery Time | ($I_S$ = −2.1 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | − | 65 | 100 | ns |
| | | $t_a$ | − | 25 | − | |
| | | $t_b$ | − | 40 | − | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | − | 0.075 | − | μC |

4. Handling precautions to protect against electrostatic discharge is mandatory.
5. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
6. Switching characteristics are independent of operating junction temperature.

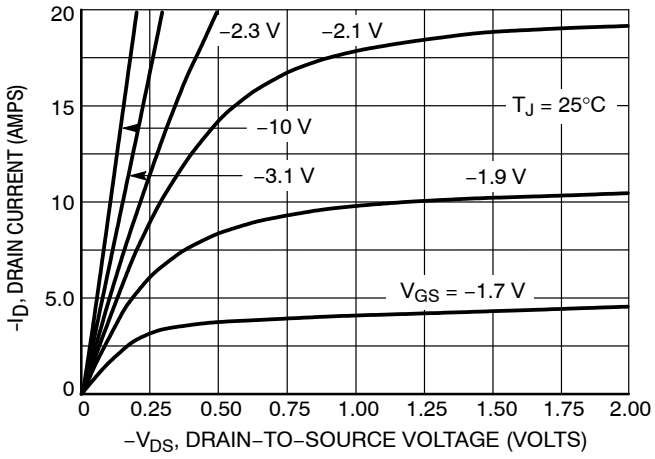



**Figure 1. On−Region Characteristics**

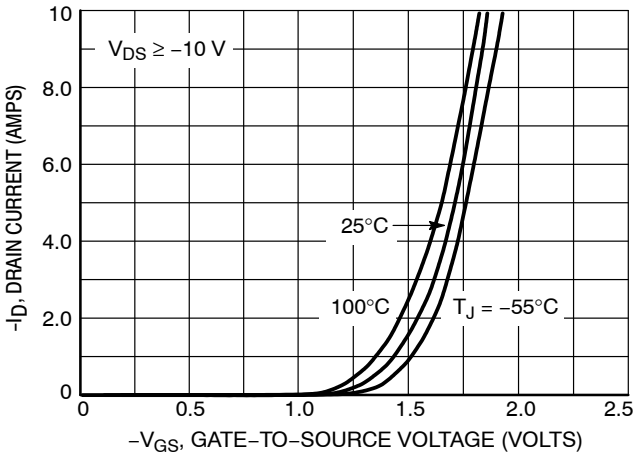



**Figure 2. Transfer Characteristics**

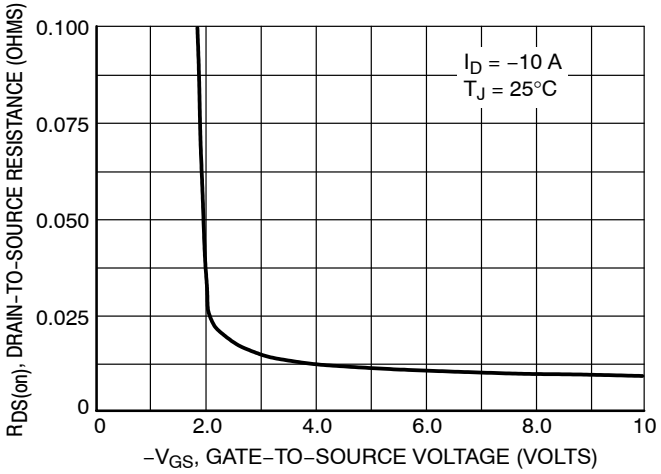



**Figure 3. On−Resistance versus Gate−To−Source Voltage**

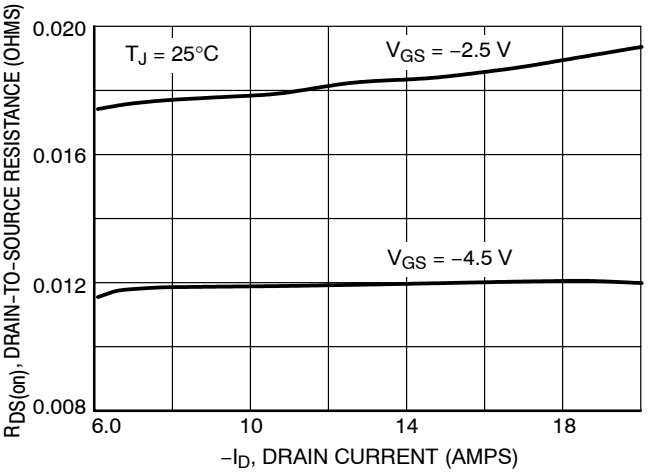



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**

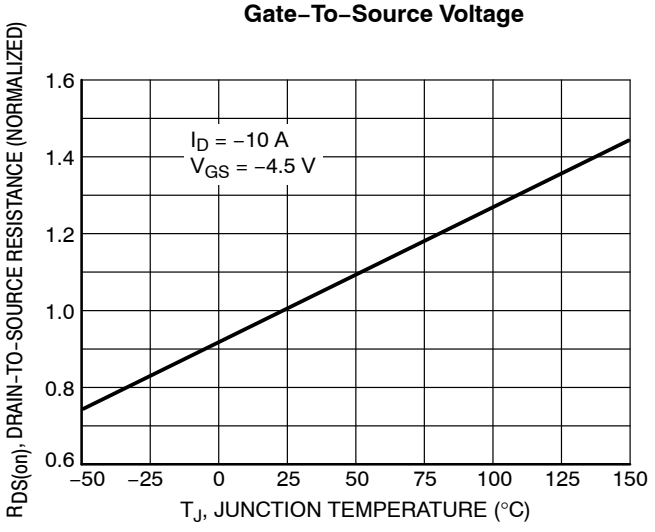



**Figure 5. On−Resistance Variation with Temperature**

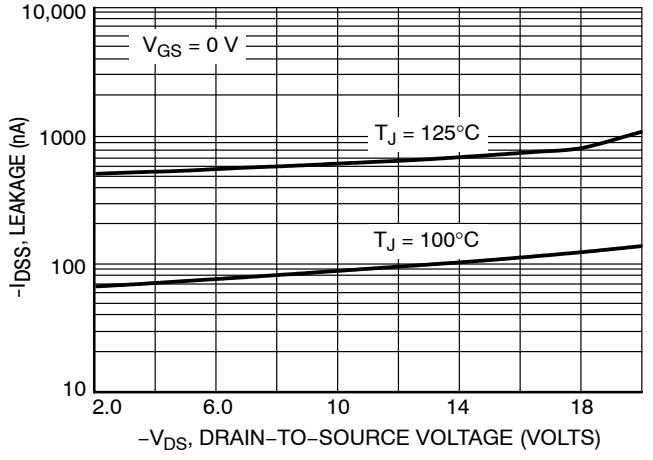



**Figure 6. Drain−To−Source Leakage Current versus Voltage**

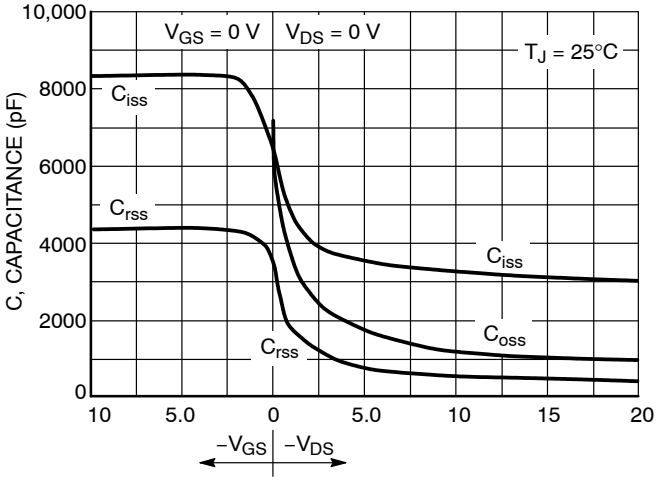



**Figure 7. Capacitance Variation**

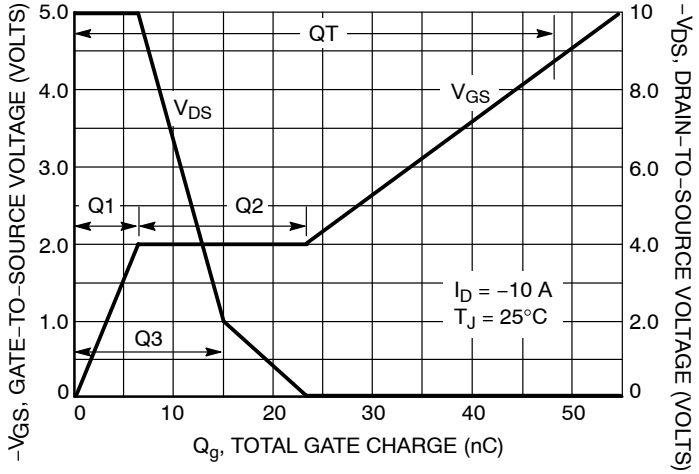



**Figure 8. Gate−To−Source and Drain−To−Source Voltage versus Total Charge**

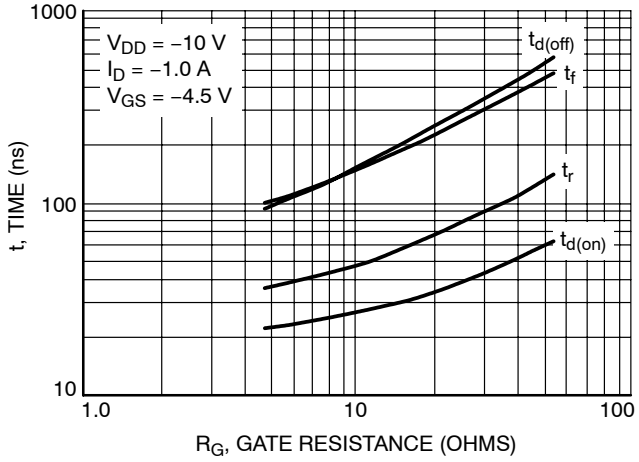



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

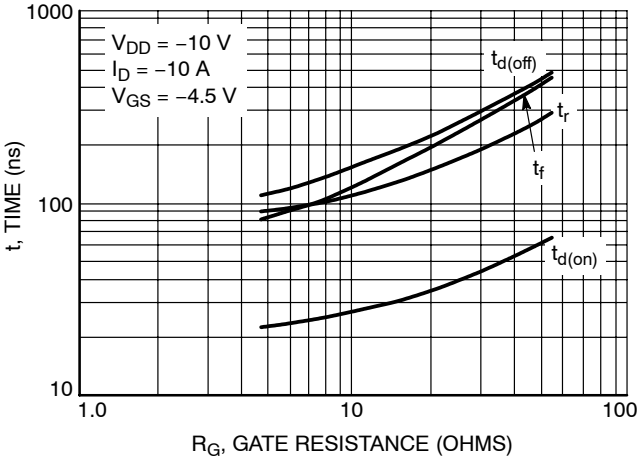



**Figure 10. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN−TO−SOURCE DIODE CHARACTERISTICS

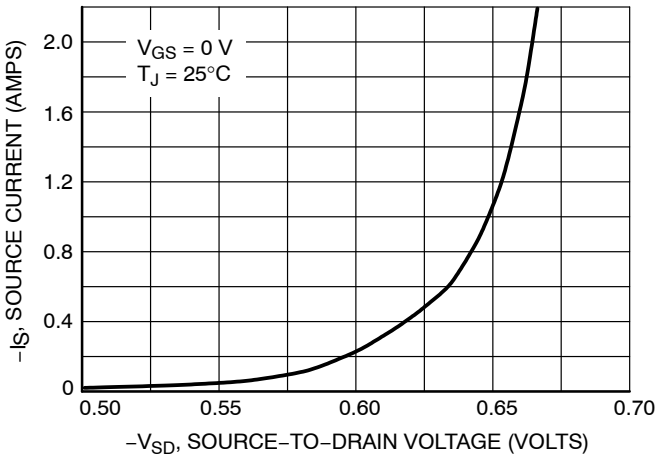



**Figure 11. Diode Forward Voltage versus Current**

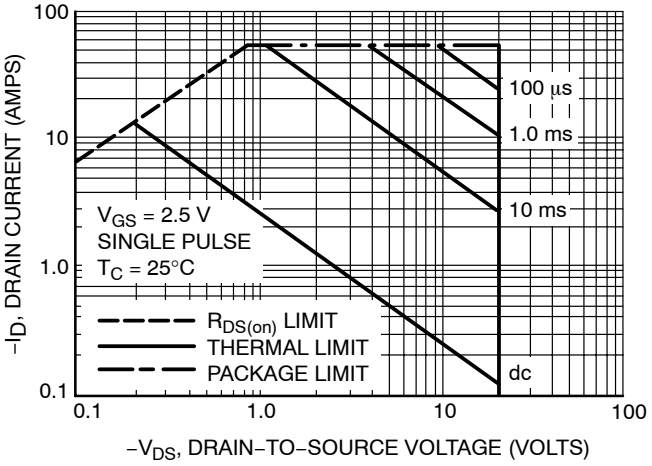



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

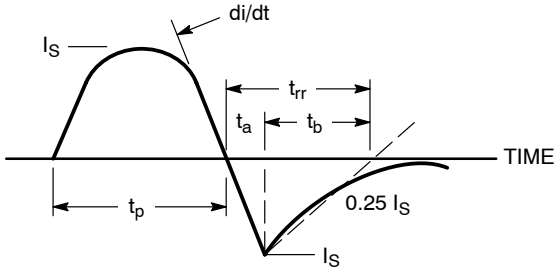



**Figure 13. Diode Reverse Recovery Waveform**

## TYPICAL ELECTRICAL CHARACTERISTICS

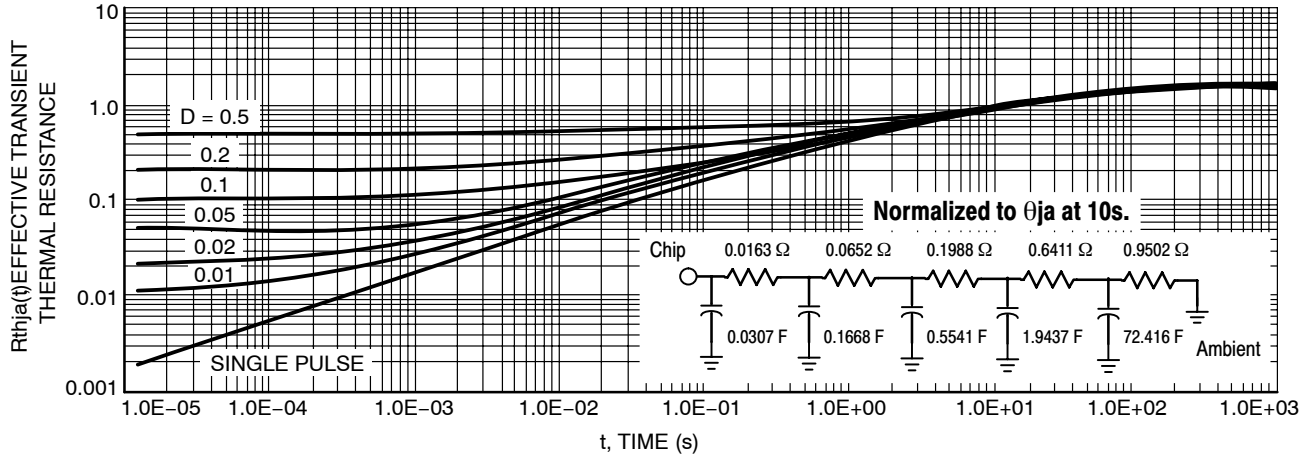
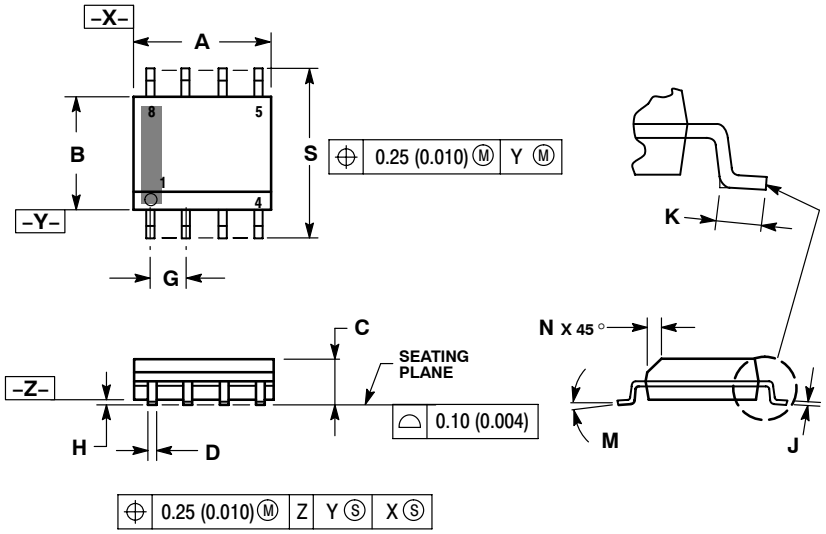



**Figure 14. Thermal Response**

## PACKAGE DIMENSIONS

**SOIC−8 NB**
CASE 751−07
ISSUE AG

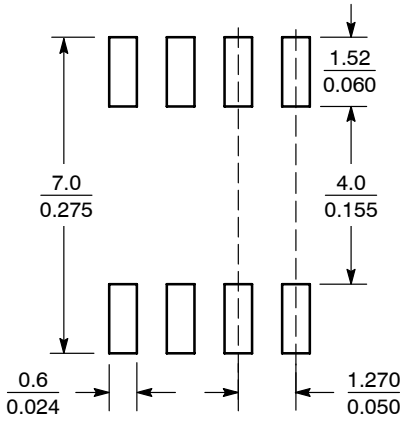



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

### SOLDERING FOOTPRINT*




SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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