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# NTS0101

Dual supply translating transceiver; open drain; auto direction sensing

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Product data sheet

## 1. General description

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The NTS0101 is a 1-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 1-bit input-output ports (A and B), one output enable input (OE) and two supply pins ( $V_{CC(A)}$  and  $V_{CC(B)}$ ).  $V_{CC(A)}$  can be supplied at any voltage between 1.65 V and 3.6 V.  $V_{CC(B)}$  can be supplied at any voltage between 2.3 V and 5.5 V. This flexibility makes the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins A and OE are referenced to  $V_{CC(A)}$  and pin B is referenced to  $V_{CC(B)}$ . A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

## 2. Features and benefits

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- Wide supply voltage range:
  - ◆  $V_{CC(A)}$ : 1.65 V to 3.6 V and  $V_{CC(B)}$ : 2.3 V to 5.5 V
- Maximum data rates:
  - ◆ Push-pull: 50 Mbps
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5 V
- ESD protection:
  - ◆ HBM JESD22-A114E Class 2 exceeds 2500 V for A port
  - ◆ HBM JESD22-A114E Class 3B exceeds 8000 V for B port
  - ◆ MM JESD22-A115-A exceeds 200 V
  - ◆ CDM JESD22-C101E exceeds 1500 V
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

## 3. Applications

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- I<sup>2</sup>C/SMBus
- UART
- GPIO



## 4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
NTS0101GW	-40 °C to +125 °C	SC-88	plastic surface-mounted package; 6 leads	SOT363
NTS0101GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
NTS0101GF	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1 × 0.5 mm	SOT891
NTS0101GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202

## 5. Marking

Table 2. Marking

Type number	Marking code <sup>[1]</sup>
NTS0101GW	s1
NTS0101GM	s1
NTS0101GF	s1
NTS0101GS	s1

[1] The pin 1 indicator is on the lower left corner of the device, below the marking code.

## 6. Functional diagram

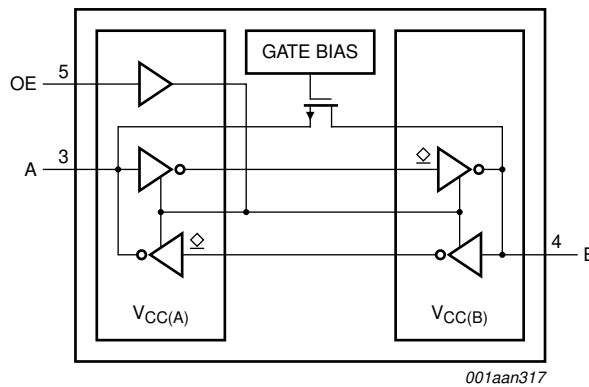
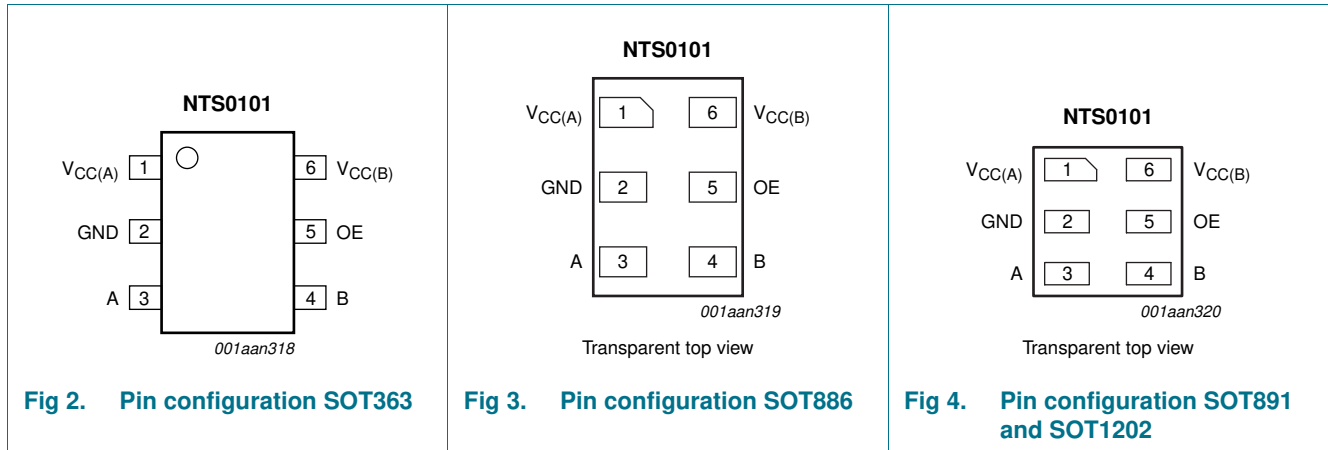


Fig 1. Logic symbol

## 7. Pinning information

### 7.1 Pinning



### 7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$V_{CC(A)}$	1	supply voltage A
GND	2	ground (0 V)
A	3	data input or output (referenced to $V_{CC(A)}$ )
B	4	data input or output (referenced to $V_{CC(B)}$ )
OE	5	output enable input (active HIGH; referenced to $V_{CC(A)}$ )
$V_{CC(B)}$	6	supply voltage B

## 8. Functional description

Table 4. Function table<sup>[1]</sup>

Supply voltage		Input	Input/output	
$V_{CC(A)}$	$V_{CC(B)}$	OE	A	B
1.65 V to $V_{CC(B)}$	2.3 V to 5.5 V	L	Z	Z
1.65 V to $V_{CC(B)}$	2.3 V to 5.5 V	H	input or output	output or input
GND <sup>[2]</sup>	GND <sup>[2]</sup>	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] When either  $V_{CC(A)}$  or  $V_{CC(B)}$  is at GND level, the device goes into power-down mode.

## 9. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+6.5	V
$V_{CC(B)}$	supply voltage B		-0.5	+6.5	V
$V_I$	input voltage	A port and OE input <a href="#">[1][2]</a>	-0.5	+6.5	V
		B port <a href="#">[1][2]</a>	-0.5	+6.5	V
$V_O$	output voltage	Active mode <a href="#">[1][2]</a>			
		A or B port	-0.5	$V_{CCO} + 0.5$	V
		Power-down or 3-state mode <a href="#">[1]</a>			
		A port	-0.5	+4.6	V
		B port	-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$I_O$	output current	$V_O = 0$ V to $V_{CCO}$ <a href="#">[2]</a>	-	$\pm 50$	mA
$I_{CC}$	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C <a href="#">[3]</a>	-	250	mW

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]  $V_{CCO}$  is the supply voltage associated with the output.

[3] For SC-88 and SC-74A packages: above 87.5 °C the value of  $P_{tot}$  derates linearly with 4.0 mW/K.  
For XSON6 packages: above 118 °C the value of  $P_{tot}$  derates linearly with 7.8 mW/K.

## 10. Recommended operating conditions

**Table 6. Recommended operating conditions**[\[1\]\[2\]](#)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.65	3.6	V
$V_{CC(B)}$	supply voltage B		2.3	5.5	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	A or B port; push-pull driving			
		$V_{CC(A)} = 1.65$ V to 3.6 V; $V_{CC(B)} = 2.3$ V to 5.5 V	-	10	ns/V
		OE input			
		$V_{CC(A)} = 1.65$ V to 3.6 V; $V_{CC(B)} = 2.3$ V to 5.5 V	-	10	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at  $V_{CC1}$  or both at GND.

[2]  $V_{CC(A)}$  must be less than or equal to  $V_{CC(B)}$ .

## 11. Static characteristics

**Table 7. Typical static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_I$	input leakage current	OE input; $V_I = 0\text{ V to }3.6\text{ V}$ ; $V_{CC(A)} = 1.65\text{ V to }3.6\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	A or B port; $V_O = 0\text{ V or }V_{CCO}$ ; $V_{CC(A)} = 1.65\text{ V to }3.6\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$ [1]	-	-	$\pm 1$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	A port; $V_I$ or $V_O = 0\text{ V to }3.6\text{ V}$ ; $V_{CC(A)} = 0\text{ V}$ ; $V_{CC(B)} = 0\text{ V to }5.5\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
		B port; $V_I$ or $V_O = 0\text{ V to }5.5\text{ V}$ ; $V_{CC(B)} = 0\text{ V}$ ; $V_{CC(A)} = 0\text{ V to }3.6\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$C_I$	input capacitance	OE input; $V_{CC(A)} = 3.3\text{ V}$ ; $V_{CC(B)} = 3.3\text{ V}$	-	1	-	pF
$C_{I/O}$	input/output capacitance	A port	-	4	-	pF
		B port	-	7.5	-	pF
		A or B port; $V_{CC(A)} = 3.3\text{ V}$ ; $V_{CC(B)} = 3.3\text{ V}$	-	11	-	pF

[1]  $V_{CCO}$  is the supply voltage associated with the output.

**Table 8. Typical supply current**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

$V_{CC(A)}$	$V_{CC(B)}$						Unit
	2.5 V		3.3 V		5.0 V		
	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	
1.8 V	0.1	0.5	0.1	1.5	0.1	4.6	$\mu\text{A}$
2.5 V	0.1	0.1	0.1	0.8	0.1	3.8	$\mu\text{A}$
3.3 V	-	-	0.1	0.1	0.1	2.8	$\mu\text{A}$

**Table 9. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$-40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$		$-40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C}$		Unit
			Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	A port					
		$V_{CC(A)} = 1.65\text{ V to }1.95\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$ [1]	$V_{CCI} - 0.2$	-	$V_{CCI} - 0.2$	-	V
		$V_{CC(A)} = 2.3\text{ V to }3.6\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$ [1]	$V_{CCI} - 0.4$	-	$V_{CCI} - 0.4$	-	V
		B port					
		$V_{CC(A)} = 1.65\text{ V to }3.6\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$ [1]	$V_{CCI} - 0.4$	-	$V_{CCI} - 0.4$	-	V
		OE input					
		$V_{CC(A)} = 1.65\text{ V to }3.6\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$	$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V

Dual supply translating transceiver; open drain; auto direction sensing

**Table 9. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V <sub>IL</sub>	LOW-level input voltage	A or B port V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	0.15	-	0.15	V
		OE input V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	0.35V <sub>CC(A)</sub>	-	0.35V <sub>CC(A)</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>O</sub> = -20 μA V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V [2]	0.67V <sub>CCO</sub>	-	0.67V <sub>CCO</sub>	-	V
		V <sub>OL</sub>	LOW-level output voltage	A or B port; I <sub>O</sub> = 1 mA [2] V <sub>I</sub> ≤ 0.15 V; V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	0.4	-
I <sub>I</sub>	input leakage current	OE input; V <sub>I</sub> = 0 V to 3.6 V; V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	±2	-	±12	μA
I <sub>OZ</sub>	OFF-state output current	A or B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V [2]	-	±2	-	±12	μA
I <sub>OFF</sub>	power-off leakage current	A port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 0 V to 5.5 V	-	±2	-	±12	μA
		B port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(B)</sub> = 0 V; V <sub>CC(A)</sub> = 0 V to 3.6 V	-	±2	-	±12	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A [1]					
		I <sub>CC(A)</sub> V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	2.4	-	15	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	2.2	-	15	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 5.5 V	-	-1	-	-8	μA
		I <sub>CC(B)</sub> V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	12	-	30	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	-1	-	-5	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 5.5 V	-	1	-	6	μA
		I <sub>CC(A)</sub> + I <sub>CC(B)</sub> V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	14.4	-	30	μA

[1] V<sub>CCI</sub> is the supply voltage associated with the input.

[2] V<sub>CCO</sub> is the supply voltage associated with the output.

## 12. Dynamic characteristics

**Table 10. Dynamic characteristics for temperature range  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$**

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 7](#); for wave forms, see [Figure 5](#) and [Figure 6](#).

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			$2.5\text{ V} \pm 0.2\text{ V}$		$3.3\text{ V} \pm 0.3\text{ V}$		$5.0\text{ V} \pm 0.5\text{ V}$		
			Min	Max	Min	Max	Min	Max	
<b><math>V_{CC(A)} = 1.8\text{ V} \pm 0.15\text{ V}</math></b>									
$t_{PHL}$	HIGH to LOW propagation delay	A to B	-	4.6	-	4.7	-	5.8	ns
$t_{PLH}$	LOW to HIGH propagation delay	A to B	-	6.8	-	6.8	-	7.0	ns
$t_{PHL}$	HIGH to LOW propagation delay	B to A	-	4.4	-	4.5	-	4.7	ns
$t_{PLH}$	LOW to HIGH propagation delay	B to A	-	5.3	-	4.5	-	0.5	ns
$t_{en}$	enable time	OE to A; B	-	200	-	200	-	200	ns
$t_{dis}$	disable time	OE to A; no external load <a href="#">[2]</a>	-	25	-	25	-	25	ns
		OE to B; no external load <a href="#">[2]</a>	-	25	-	25	-	25	ns
		OE to A	-	230	-	230	-	230	ns
		OE to B	-	200	-	200	-	200	ns
$t_{TLH}$	LOW to HIGH output transition time	A port	3.2	9.5	2.3	9.3	1.8	7.6	ns
		B port	3.3	10.8	2.7	9.1	2.7	7.6	ns
$t_{THL}$	HIGH to LOW output transition time	A port	2.0	5.9	1.9	6.0	1.7	13.3	ns
		B port	2.9	7.6	2.8	7.5	2.8	10.0	ns
$t_w$	pulse width	data inputs	20	-	20	-	20	-	ns
$f_{data}$	data rate		-	50	-	50	-	50	Mbps
<b><math>V_{CC(A)} = 2.5\text{ V} \pm 0.2\text{ V}</math></b>									
$t_{PHL}$	HIGH to LOW propagation delay	A to B	-	3.2	-	3.3	-	3.4	ns
$t_{PLH}$	LOW to HIGH propagation delay	A to B	-	3.5	-	4.1	-	4.4	ns
$t_{PHL}$	HIGH to LOW propagation delay	B to A	-	3.0	-	3.6	-	4.3	ns
$t_{PLH}$	LOW to HIGH propagation delay	B to A	-	2.5	-	1.6	-	0.7	ns
$t_{en}$	enable time	OE to A; B	-	200	-	200	-	200	ns
$t_{dis}$	disable time	OE to A; no external load <a href="#">[2]</a>	-	20	-	20	-	20	ns
		OE to B; no external load <a href="#">[2]</a>	-	20	-	20	-	20	ns
		OE to A	-	200	-	200	-	200	ns
		OE to B	-	200	-	200	-	200	ns
$t_{TLH}$	LOW to HIGH output transition time	A port	2.8	7.4	2.6	6.6	1.8	6.2	ns
		B port	3.2	8.3	2.9	7.9	2.4	6.8	ns



**Table 10. Dynamic characteristics for temperature range  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ <sup>[1]</sup> ...continued**Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 7](#); for wave forms, see [Figure 5](#) and [Figure 6](#).

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			$2.5\text{ V} \pm 0.2\text{ V}$		$3.3\text{ V} \pm 0.3\text{ V}$		$5.0\text{ V} \pm 0.5\text{ V}$		
			Min	Max	Min	Max	Min	Max	
$t_{THL}$	HIGH to LOW output transition time	A port	1.9	5.7	1.9	5.5	1.8	5.3	ns
		B port	2.2	7.8	2.4	6.7	2.6	6.6	ns
$t_W$	pulse width	data inputs	20	-	20	-	20	-	ns
$f_{data}$	data rate		-	50	-	50	-	50	Mbps
<b><math>V_{CC(A)} = 3.3\text{ V} \pm 0.3\text{ V}</math></b>									
$t_{PHL}$	HIGH to LOW propagation delay	A to B	-	-	-	2.4	-	3.1	ns
$t_{PLH}$	LOW to HIGH propagation delay	A to B	-	-	-	4.2	-	4.4	ns
$t_{PHL}$	HIGH to LOW propagation delay	B to A	-	-	-	2.5	-	3.3	ns
$t_{PLH}$	LOW to HIGH propagation delay	B to A	-	-	-	2.5	-	2.6	ns
$t_{en}$	enable time	OE to A; B	-	-	-	200	-	200	ns
$t_{dis}$	disable time	OE to A; no external load <sup>[2]</sup>	-	-	-	15	-	15	ns
		OE to B; no external load <sup>[2]</sup>	-	-	-	15	-	15	ns
		OE to A	-	-	-	260	-	260	ns
		OE to B	-	-	-	200	-	200	ns
$t_{TLH}$	LOW to HIGH output transition time	A port	-	-	2.3	5.6	1.9	5.9	ns
		B port	-	-	2.5	6.4	2.1	7.4	ns
$t_{THL}$	HIGH to LOW output transition time	A port	-	-	2.0	5.4	1.9	5.0	ns
		B port	-	-	2.3	7.4	2.4	7.6	ns
$t_W$	pulse width	data inputs	-	-	20	-	20	-	ns
$f_{data}$	data rate		-	-	-	50	-	50	Mbps

[1]  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ . $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

[2] Delay between OE going LOW and when the outputs are disabled.

**Table 11. Dynamic characteristics for temperature range –40 °C to +125 °C<sup>[1]</sup>**

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 7](#); for wave forms, see [Figure 5](#) and [Figure 6](#).

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
<b>V<sub>CC(A)</sub> = 1.8 V ± 0.15 V</b>									
t <sub>PHL</sub>	HIGH to LOW propagation delay	A to B	-	5.8	-	5.9	-	7.3	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	A to B	-	8.5	-	8.5	-	8.8	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	B to A	-	5.5	-	5.7	-	5.9	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	B to A	-	6.7	-	5.7	-	0.7	ns
t <sub>en</sub>	enable time	OE to A; B	-	200	-	200	-	200	ns
t <sub>dis</sub>	disable time	OE to A; no external load <a href="#">[2]</a>	-	30	-	30	-	30	ns
		OE to B; no external load <a href="#">[2]</a>	-	30	-	30	-	30	ns
		OE to A	-	250	-	250	-	250	ns
		OE to B	-	220	-	220	-	220	ns
t <sub>TLH</sub>	LOW to HIGH output transition time	A port	3.2	11.9	2.3	11.7	1.8	9.5	ns
		B port	3.3	13.5	2.7	11.4	2.7	9.5	ns
t <sub>THL</sub>	HIGH to LOW output transition time	A port	2.0	7.4	1.9	7.5	1.7	16.7	ns
		B port	2.9	9.5	2.8	9.4	2.8	12.5	ns
t <sub>w</sub>	pulse width	data inputs	20	-	20	-	20	-	ns
f <sub>data</sub>	data rate		-	50	-	50	-	50	Mbps
<b>V<sub>CC(A)</sub> = 2.5 V ± 0.2 V</b>									
t <sub>PHL</sub>	HIGH to LOW propagation delay	A to B	-	4.0	-	4.2	-	4.3	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	A to B	-	4.4	-	5.2	-	5.5	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	B to A	-	3.8	-	4.5	-	5.4	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	B to A	-	3.2	-	2.0	-	0.9	ns
t <sub>en</sub>	enable time	OE to A; B	-	200	-	200	-	200	ns
t <sub>dis</sub>	disable time	OE to A; no external load <a href="#">[2]</a>	-	25	-	25	-	25	ns
		OE to B; no external load <a href="#">[2]</a>	-	25	-	25	-	25	ns
		OE to A	-	220	-	220	-	220	ns
		OE to B	-	220	-	220	-	220	ns
t <sub>TLH</sub>	LOW to HIGH output transition time	A port	2.8	9.3	2.6	8.3	1.8	7.8	ns
		B port	3.2	10.4	2.9	9.7	2.4	8.3	ns
t <sub>THL</sub>	HIGH to LOW output transition time	A port	1.9	7.2	1.9	6.9	1.8	6.7	ns
		B port	2.2	9.8	2.4	8.4	2.6	8.3	ns

**Table 11. Dynamic characteristics for temperature range  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ <sup>[1]</sup> ...continued**

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 7](#); for wave forms, see [Figure 5](#) and [Figure 6](#).

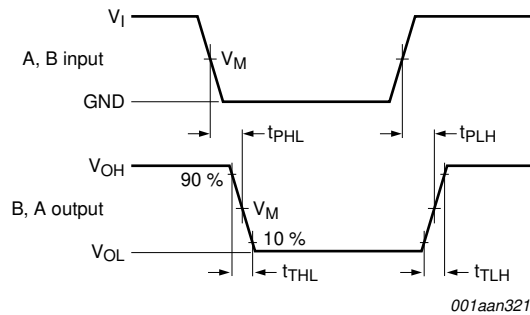
Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			$2.5\text{ V} \pm 0.2\text{ V}$		$3.3\text{ V} \pm 0.3\text{ V}$		$5.0\text{ V} \pm 0.5\text{ V}$		
			Min	Max	Min	Max	Min	Max	
$t_w$	pulse width	data inputs	20	-	20	-	20	-	ns
$f_{data}$	data rate		-	50	-	50	-	50	Mbps
<b><math>V_{CC(A)} = 3.3\text{ V} \pm 0.3\text{ V}</math></b>									
$t_{PHL}$	HIGH to LOW propagation delay	A to B	-	-	-	3.0	-	3.9	ns
$t_{PLH}$	LOW to HIGH propagation delay	A to B	-	-	-	5.3	-	5.5	ns
$t_{PHL}$	HIGH to LOW propagation delay	B to A	-	-	-	3.2	-	4.2	ns
$t_{PLH}$	LOW to HIGH propagation delay	B to A	-	-	-	3.2	-	3.3	ns
$t_{en}$	enable time	OE to A; B	-	-	-	200	-	200	ns
$t_{dis}$	disable time	OE to A; no external load <sup>[2]</sup>	-	-	-	20	-	20	ns
		OE to B; no external load <sup>[2]</sup>	-	-	-	20	-	20	ns
		OE to A	-	-	-	280	-	280	ns
		OE to B	-	-	-	220	-	220	ns
$t_{TLH}$	LOW to HIGH output transition time	A port	-	-	2.3	7.0	1.9	7.4	ns
		B port	-	-	2.5	8.0	2.1	9.3	ns
$t_{THL}$	HIGH to LOW output transition time	A port	-	-	2.0	6.8	1.9	6.3	ns
		B port	-	-	2.3	9.3	2.4	9.5	ns
$t_w$	pulse width	data inputs	-	-	20	-	20	-	ns
$f_{data}$	data rate		-	-	-	50	-	50	Mbps

[1]  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

$t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

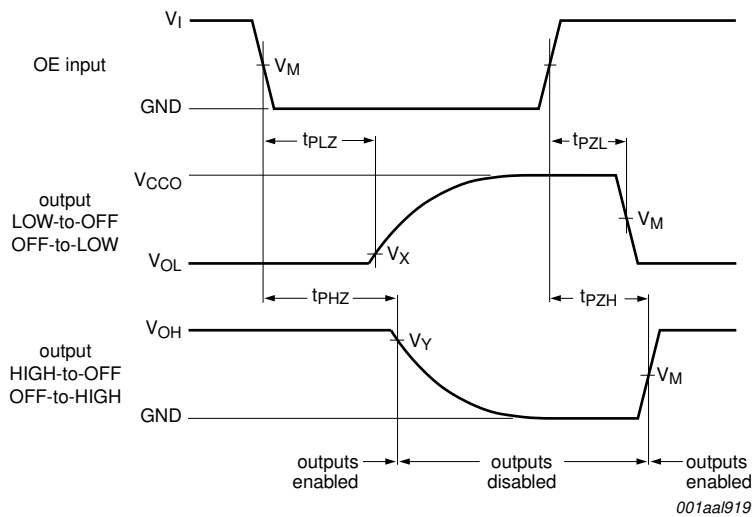
[2] Delay between OE going LOW and when the outputs are disabled.

13. Waveforms



Measurement points are given in [Table 12](#).  
 VOL and VOH are typical output voltage levels that occur with the output load.

**Fig 5. The data input (A, B) to data output (B, A) propagation delay times**



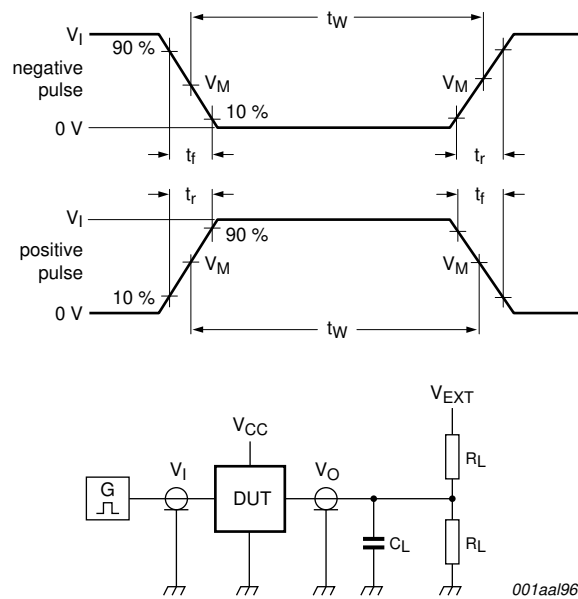
Measurement points are given in [Table 12](#).  
 VOL and VOH are typical output voltage levels that occur with the output load.

**Fig 6. Enable and disable times**

**Table 12. Measurement points<sup>[1][2]</sup>**

Supply voltage	Input	Output		
VCCO	VM	VM	VX	VY
1.8 V ± 0.15 V	0.5VCCI	0.5VCCO	VOL + 0.15 V	VOH - 0.15 V
2.5 V ± 0.2 V	0.5VCCI	0.5VCCO	VOL + 0.15 V	VOH - 0.15 V
3.3 V ± 0.3 V	0.5VCCI	0.5VCCO	VOL + 0.3 V	VOH - 0.3 V
5.0 V ± 0.5 V	0.5VCCI	0.5VCCO	VOL + 0.3 V	VOH - 0.3 V

[1] VCCI is the supply voltage associated with the input.  
 [2] VCCO is the supply voltage associated with the output.



Test data is given in [Table 13](#).

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z<sub>O</sub> = 50 Ω; dV/dt ≥ 1.0 V/ns.

R<sub>L</sub> = Load resistance.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

V<sub>EXT</sub> = External voltage for measuring switching times.

**Fig 7. Test circuit for measuring switching times**

**Table 13. Test data**

Supply voltage		Input		Load		V <sub>EXT</sub>		
V <sub>CC(A)</sub>	V <sub>CC(B)</sub>	V <sub>I</sub> <sup>[1]</sup>	Δt/ΔV	C <sub>L</sub>	R <sub>L</sub> <sup>[2]</sup>	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub> <sup>[3]</sup>
1.65 V to 3.6 V	2.3 V to 5.5 V	V <sub>CCI</sub>	≤ 1.0 ns/V	15 pF	50 kΩ, 1 MΩ	open	open	2V <sub>CCO</sub>

[1] V<sub>CCI</sub> is the supply voltage associated with the input.

[2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R<sub>L</sub> = 1 MΩ. For measuring enable and disable times, R<sub>L</sub> = 50 KΩ.

[3] V<sub>CCO</sub> is the supply voltage associated with the output.

## 14. Application information

### 14.1 Applications

Voltage level-translation applications. The NTS0101 can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device is primarily targeted at I<sup>2</sup>C or 1-wire which use open-drain drivers. It may also be used in applications where push-pull drivers are connected to the ports, however the NTB0101 may be more suitable.

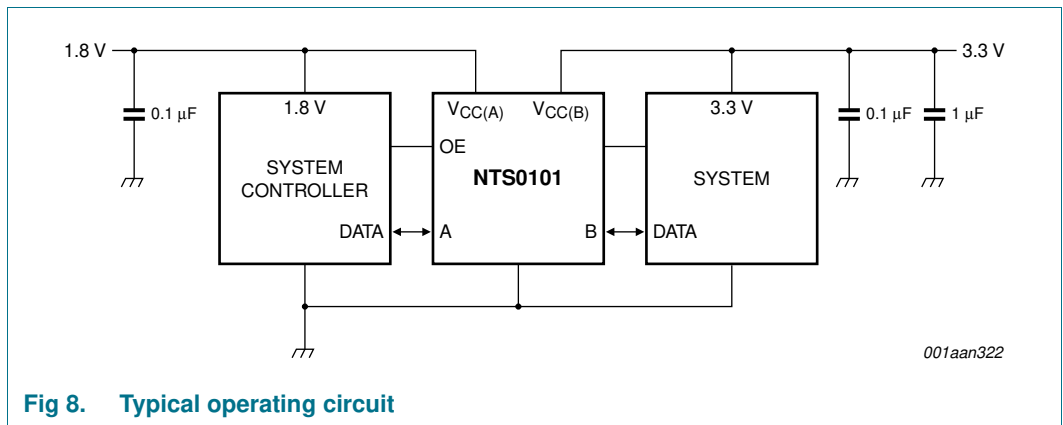


Fig 8. Typical operating circuit

### 14.2 Architecture

The architecture of the NTS0101 is shown in Figure 9. The device does not require an extra input signal to control the direction of data flow from A to B or B to A.

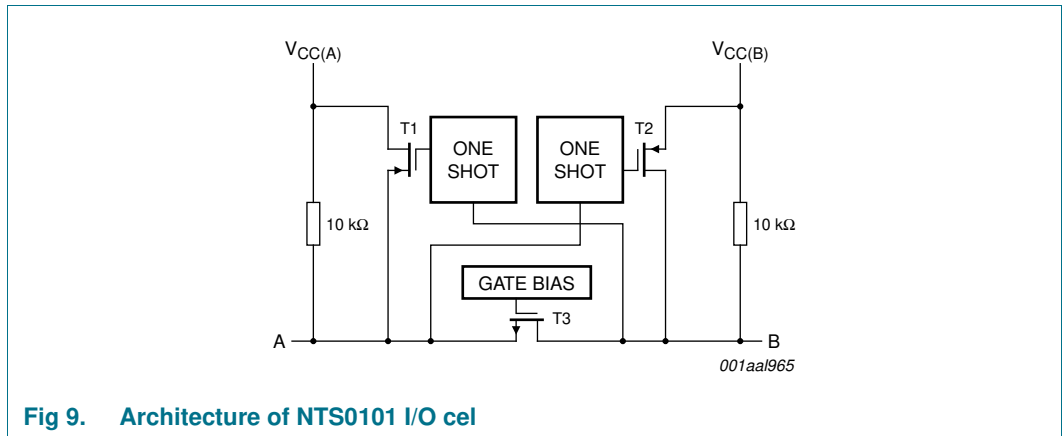


Fig 9. Architecture of NTS0101 I/O cell

The NTS0101 is a "switch" type voltage translator, it employs two key circuits to enable voltage translation:

1. A pass-gate transistor (N-channel) that ties the ports together.
2. An output edge-rate accelerator that detects and accelerates rising edges on the I/O pins.

The gate bias voltage of the pass gate transistor (T3) is set at approximately one threshold voltage above the  $V_{CC}$  level of the low-voltage side. During a LOW-to-HIGH transition, the output one-shot accelerates the output transition by switching on the PMOS transistors (T1, T2). It bypasses the 10 k $\Omega$  pull-up resistors and increases the current drive capability. The one-shot is activated once the input transition reaches approximately  $V_{CC}/2$ ; it is de-activated approximately 50 ns after the output reaches  $V_{CCO}/2$ . During the acceleration time, the driver output resistance is between approximately 50  $\Omega$  and 70  $\Omega$ . To avoid signal contention and minimize dynamic  $I_{CC}$ , the user should wait for the one-shot circuit to turn-off before applying a signal in the opposite direction. Pull-up resistors are included in the device for DC current sourcing capability.

### 14.3 Input driver requirements

As the NTS0101 is a switch type translator, properties of the input driver directly effect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system. The max data rate, HIGH-to-LOW output transition time ( $t_{THL}$ ), and propagation delay ( $t_{PHL}$ ), are dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters in the data sheet assume a driver with output impedance below 50  $\Omega$  is used.

### 14.4 Output load considerations

The maximum lumped capacitive load that can be driven is dependant upon the one-shot pulse duration. In cases with very heavy capacitive loading, there is a risk that the output does not reach the positive rail within the one-shot pulse duration.

To avoid excessive capacitive loading and to ensure correct triggering of the one-shot, use short trace lengths and low capacitance connectors on NTS0101 PCB layouts. The length of the PCB trace should be such that the round-trip delay of any reflection is within the one-shot pulse duration (approximately 50 ns). It ensures low impedance termination and avoids output signal oscillations and one-shot retriggering.

### 14.5 Power-up

During operation,  $V_{CC(A)}$  must never be higher than  $V_{CC(B)}$ . However, during power-up,  $V_{CC(A)} \geq V_{CC(B)}$  does not damage the device, so either power supply can be ramped up first. There is no special power-up sequencing required. The NTS0101 includes circuitry that disables all output ports when either  $V_{CC(A)}$  or  $V_{CC(B)}$  is switched off.

### 14.6 Enable and disable

An output enable input (OE) is used to disable the device. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time ( $t_{dis}$  with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time ( $t_{en}$ ) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor. The current-sourcing capability of the driver determines the minimum value of the resistor.

### 14.7 Pull-up or pull-down resistors on I/Os lines

The A port I/O has an internal 10 k $\Omega$  pull-up resistor to  $V_{CC(A)}$ . The B port I/O has an internal 10 k $\Omega$  pull-up resistor to  $V_{CC(B)}$ . If a smaller value of pull-up resistor is required, add an external resistor in parallel to the internal 10 k $\Omega$ . This pull-up resistor effects the  $V_{OL}$  level. When OE goes LOW, the internal pull-ups of the NTS0101 are disabled.



15. Package outline

Plastic surface-mounted package; 6 leads

SOT363

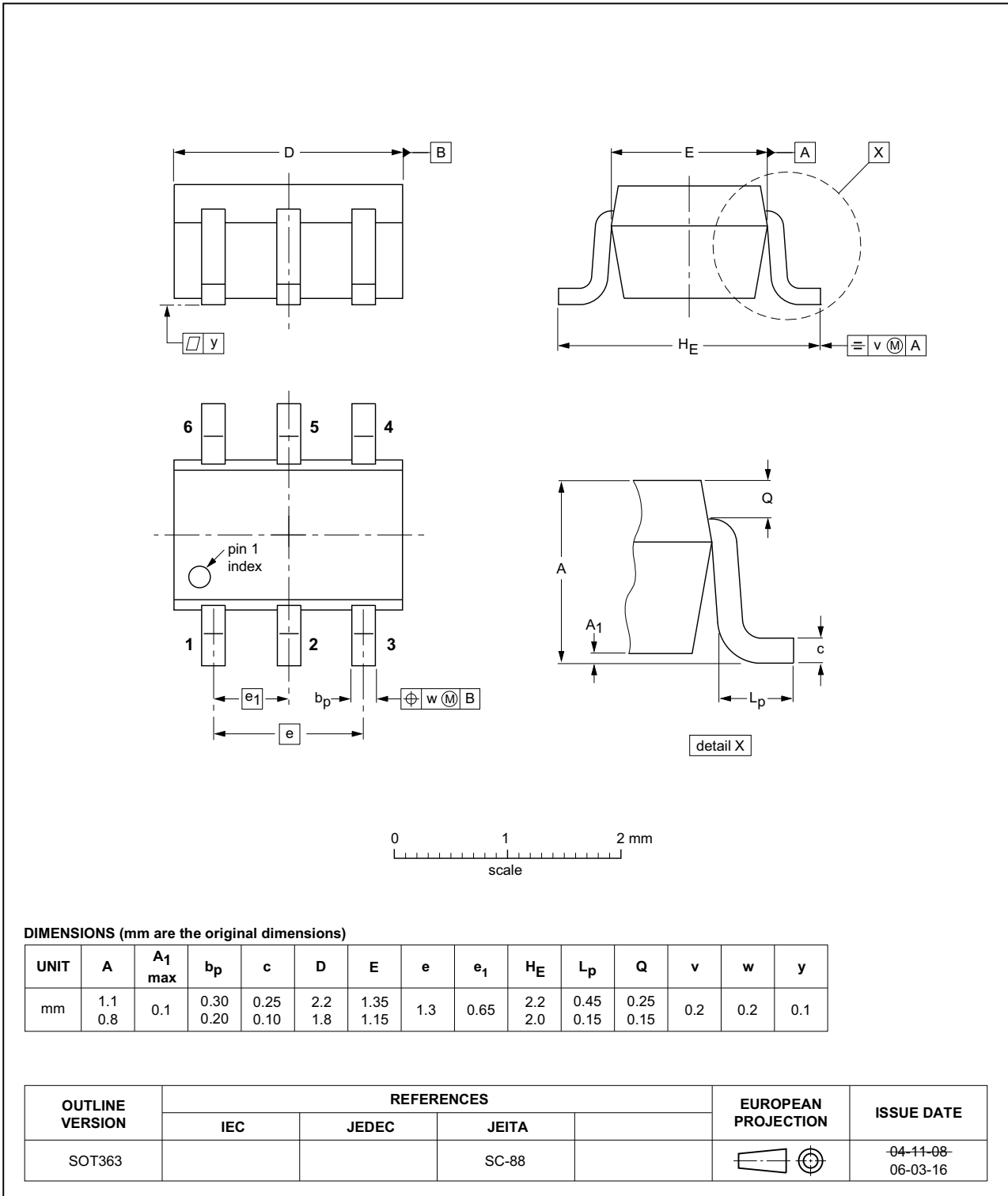


Fig 10. Package outline SOT363 (SC-88)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886

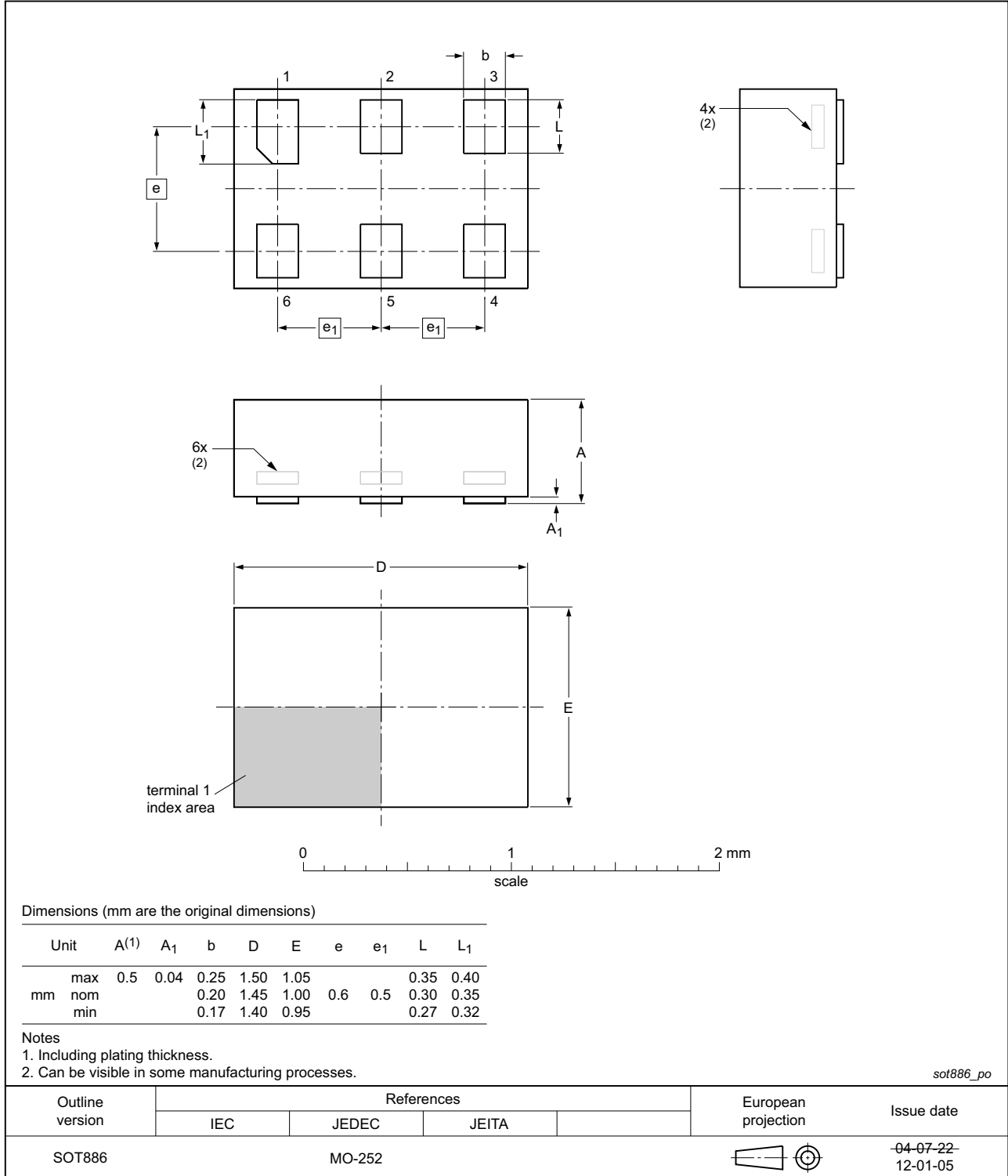


Fig 11. Package outline SOT886 (XSON6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm

SOT891

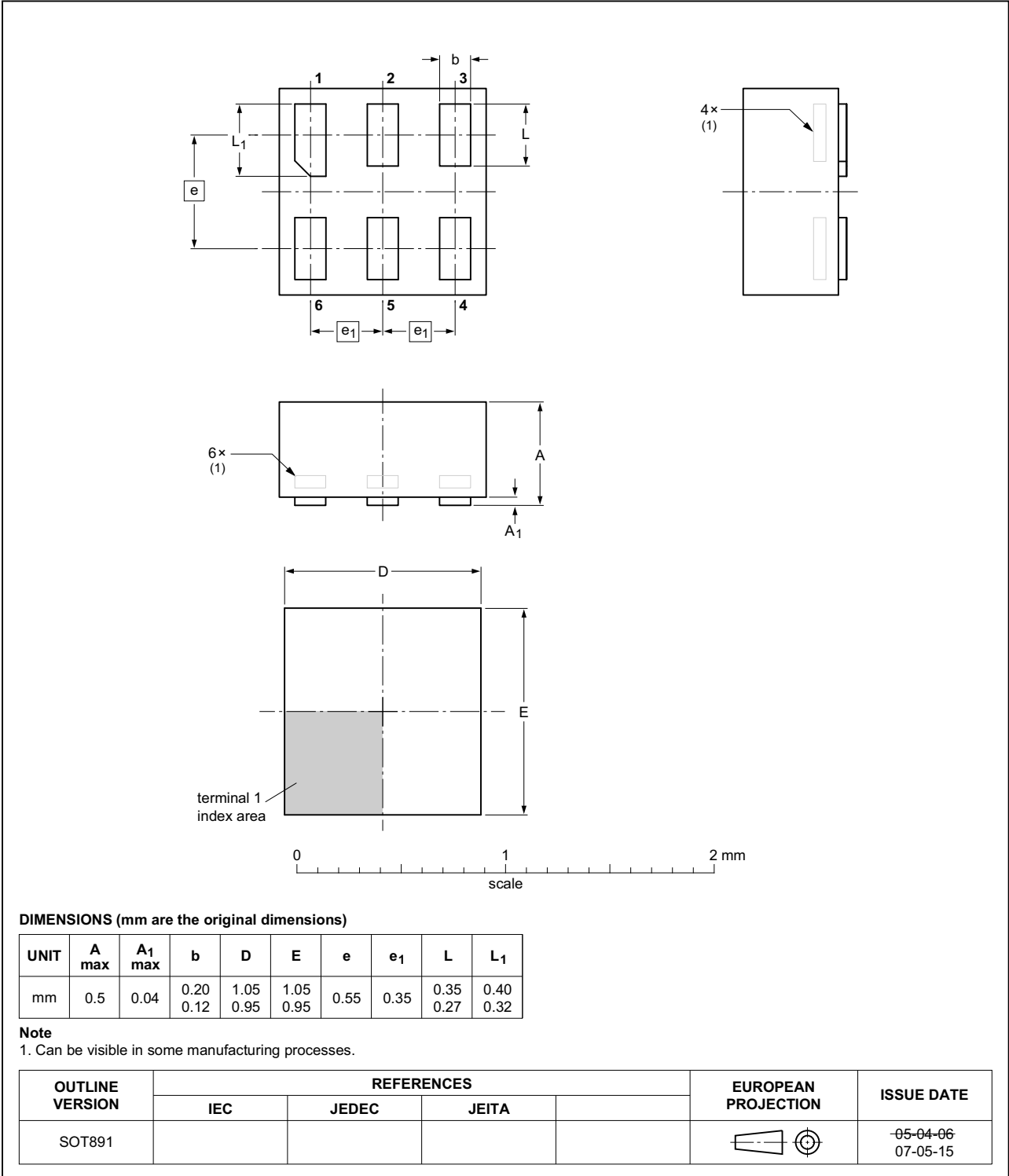
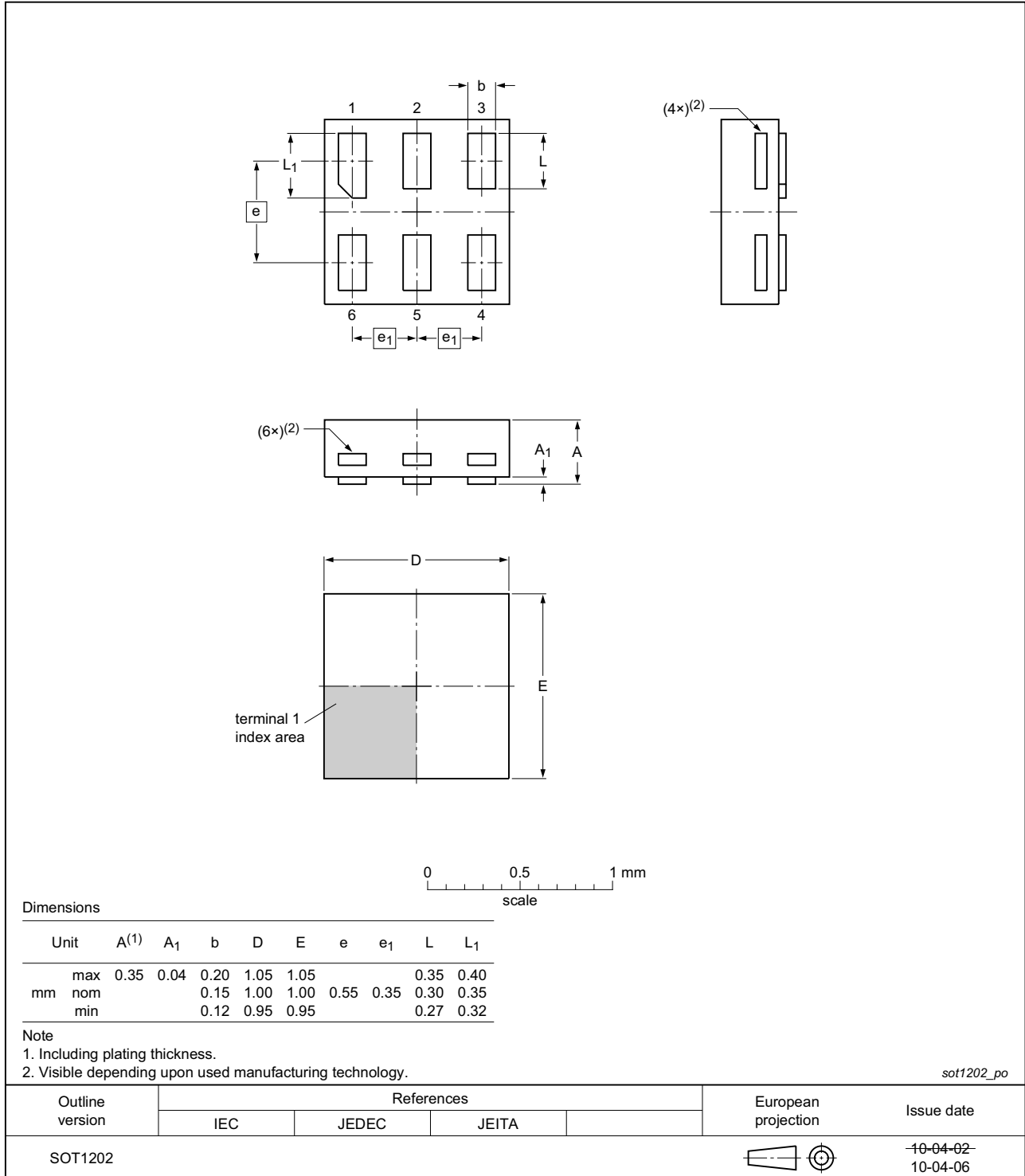


Fig 12. Package outline SOT891 (XSON6)

**XSON6: extremely thin small outline package; no leads;  
6 terminals; body 1.0 x 1.0 x 0.35 mm**

**SOT1202**



**Fig 13. Package outline SOT1202 (XSON6)**

## 16. Abbreviations

Table 14. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
GPIO	General Purpose Input Output
HBM	Human Body Model
I <sup>2</sup> C	Inter-Integrated Circuit
MM	Machine Model
PCB	Printed-Circuit Board
PMOS	Positive Metal Oxide Semiconductor
SMBus	System Management Bus
UART	Universal Asynchronous Receiver Transmitter

## 17. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NTS0101 v.5	20140811	Product data sheet	-	NTS0101 v.4
Modifications:	<ul style="list-style-type: none"> <li>Type number NTS0101GV has been removed</li> </ul>			
NTS0101 v.4	20120514	Product data sheet	-	NTS0101 v.3
Modifications:	<ul style="list-style-type: none"> <li>Package outline drawing of SOT886 (Figure 11) modified.</li> </ul>			
NTS0101 v.3	20111110	Product data sheet	-	NTS0101 v.2
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
NTS0101 v.2	20110427	Product data sheet	-	NTS0101 v.1
NTS0101 v.1	20101230	Product data sheet	-	-

## 18. Legal information

### 18.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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