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ARM Cortex™-M0
32-BIT MICROCONTROLLER

NuMicro™ Family
NUC100 Data Sheet

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1 GENERAL DESCRIPTION

The NuMicro™ NUC100 Series is 32-bit microcontrollers with embedded ARM® Cortex™-M0 core for industrial control and applications which need rich communication interfaces. The Cortex™-M0 is the newest ARM® embedded processor with 32-bit performance and at a cost equivalent to traditional 8-bit microcontroller. NuMicro™ NUC100 Series includes NUC100, NUC120, NUC130 and NUC140 product line.

The NuMicro™ NUC100 Advanced Line embeds Cortex™-M0 core running up to 50 MHz with 32K/64K/128K-byte embedded flash, 4K/8K/16K-byte embedded SRAM, and 4K-byte loader ROM for the ISP. It also equips with plenty of peripheral devices, such as Timers, Watchdog Timer, RTC, PDMA, UART, SPI, I²C, I²S, PWM Timer, GPIO, PS/2, 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-Out Detector.

Product Line	UART	SPI	I ² C	USB	LIN	CAN	PS/2	I ² S
NUC100	•	•	•				•	•
NUC120	•	•	•	•			•	•
NUC130	•	•	•		•	•	•	•
NUC140	•	•	•	•	•	•	•	•

Table 1-1 Connectivity Supported Table

2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 NuMicro™ NUC100 Features – Advanced Line

- Core
 - ARM® Cortex™-M0 core runs up to 50 MHz
 - One 24-bit system timer
 - Supports low power sleep mode
 - Single-cycle 32-bit hardware multiplier
 - NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Build-in LDO for wide operating voltage ranges from 2.5 V to 5.5 V
- Flash Memory
 - 32K/64K/128K bytes Flash for program code (128KB only support in NuMicro™ NUC100/NUC120 Medium Density)
 - 4KB flash for ISP loader
 - Support In-system program (ISP) application code update
 - 512 byte page erase for flash
 - Configurable data flash address and size for 128KB system, fixed 4KB data flash for the 32KB and 64KB system
 - Support 2 wire ICP update through SWD/ICE interface
 - Support fast parallel programming mode by external programmer
- SRAM Memory
 - 4K/8K/16K bytes embedded SRAM (16KB only support in NuMicro™ NUC100/NUC120 Medium Density)
 - Support PDMA mode
- PDMA (Peripheral DMA)
 - Support 9 channels PDMA for automatic data transfer between SRAM and peripherals (Only support 1 channel in NuMicro™ NUC100/NUC120 Low Density)
- Clock Control
 - Flexible selection for different applications
 - Built-in 22.1184 MHz high speed OSC for system operation
 - ◆ Trimmed to $\pm 1\%$ at $+25\text{ }^{\circ}\text{C}$ and $V_{DD} = 5\text{ V}$
 - ◆ Trimmed to $\pm 3\%$ at $-40\text{ }^{\circ}\text{C} \sim +85\text{ }^{\circ}\text{C}$ and $V_{DD} = 2.5\text{ V} \sim 5.5\text{ V}$
 - Built-in 10 kHz low speed OSC for Watchdog Timer and Wake-up operation
 - Support one PLL, up to 50 MHz, for high performance system operation
 - External 4~24 MHz high speed crystal input for precise timing operation
 - External 32.768 kHz low speed crystal input for RTC function and low power system operation
- GPIO
 - Four I/O modes:
 - ◆ Quasi bi-direction
 - ◆ Push-Pull output
 - ◆ Open-Drain output
 - ◆ Input only with high impedance



- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- High driver and high sink IO mode support
- Timer
 - Support 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
 - Independent clock source for each timer
 - Provides one-shot, periodic, toggle and continuous counting operation modes (NuMicro™ NUC100/NUC120 Medium Density only support one-shot and periodic mode)
 - Support event counting function (NuMicro™ NUC100/NUC120 Low Density only)
- Watchdog Timer
 - Multiple clock sources
 - 8 selectable time out period from 1.6ms ~ 26.0sec (depends on clock source)
 - WDT can wake-up from power down or idle mode
 - Interrupt or reset selectable on watchdog time-out
- RTC
 - Support software compensation by setting frequency compensate register (FCR)
 - Support RTC counter (second, minute, hour) and calendar counter (day, month, year)
 - Support Alarm registers (second, minute, hour, day, month, year)
 - Selectable 12-hour or 24-hour mode
 - Automatic leap year recognition
 - Support periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
 - Support wake-up function
- PWM/Capture
 - Built-in up to four 16-bit PWM generators provide eight PWM outputs or four complementary paired PWM outputs
 - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
 - Up to eight 16-bit digital Capture timers (shared with PWM timers) provide eight rising/falling capture inputs
 - Support Capture interrupt
- UART
 - Up to three UART controllers (NuMicro™ NUC100/NUC120 Low Density only support 2 UART controllers)
 - UART ports with flow control (TXD, RXD, CTS and RTS)
 - UART0 with 63-byte FIFO is for high speed
 - UART1/2(optional) with 15-byte FIFO for standard device
 - Support IrDA (SIR) function
 - Support RS-485 9-bit mode and direction control. (NuMicro™ NUC100/NUC120 Low Density Only)
 - Programmable baud-rate generator up to 1/16 system clock
 - Support PDMA mode
- SPI
 - Up to four sets of SPI controller (NuMicro™ NUC100/NUC120 Low Density only support 2 SPI controllers)
 - Master up to 16 MHz, and Slave up to 10 MHz (chip working @ 5V)
 - Support SPI master/slave mode



- Full duplex synchronous serial data transfer
- Variable length of transfer data from 1 to 32 bits
- MSB or LSB first data transfer
- Rx and Tx on both rising or falling edge of serial clock independently
- 2 slave/device select lines when it is as the master, and 1 slave/device select line when it is as the slave
- Support byte suspend mode in 32-bit transmission
- Support PDMA mode
- I²C
 - Up to two sets of I²C device
 - Master/Slave mode
 - Bidirectional data transfer between masters and slaves
 - Multi-master bus (no central master)
 - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
 - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
 - Programmable clocks allow versatile rate control
 - Support multiple address recognition (four slave address with mask option)
- I²S
 - Interface with external audio CODEC
 - Operate as either master or slave mode
 - Capable of handling 8-, 16-, 24- and 32-bit word sizes
 - Mono and stereo audio data supported
 - I²S and MSB justified data format supported
 - Two 8 word FIFO data buffers are provided, one for transmit and one for receive
 - Generates interrupt requests when buffer levels cross a programmable boundary
 - Support two DMA requests, one for transmit and one for receive
- PS/2 Device Controller
 - Host communication inhibit and request to send detection
 - Reception frame error detection
 - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
 - Double buffer for data reception
 - S/W override bus
- EBI (External bus interface) support (NuMicro™ NUC100/NUC120 Low Density 64-pin Package Only)
 - Accessible space: 64KB in 8-bit mode or 128KB in 16-bit mode
 - Support 8-/16-bit data width
 - Support byte write in 16-bit data width mode
- ADC
 - 12-bit SAR ADC with 600K SPS
 - Up to 8-ch single-end input or 4-ch differential input
 - Single scan/single cycle scan/continuous scan
 - Each channel with individual result register
 - Scan on enabled channels
 - Threshold voltage detection
 - Conversion start by software programming or external input
 - Support PDMA mode



- Analog Comparator
 - Up to two analog comparators
 - External input or internal bandgap voltage selectable at negative node
 - Interrupt when compare result change
 - Power down wake-up
- One built-in temperature sensor with 1°C resolution
- Brown-Out detector
 - With 4 levels: 4.5 V/3.8 V/2.7 V/2.2 V
 - Support Brown-Out Interrupt and Reset option
- Low Voltage Reset
 - Threshold voltage levels: 2.0 V
- Operating Temperature: -40°C~85°C
- Packages:
 - All Green package (RoHS)
 - LQFP 100-pin / 64-pin / 48-pin (100-pin for NuMicro™ NUC100/NUC120 Medium Density Only)



3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ NUC100 Products Selection Guide

3.1.1 NuMicro™ NUC100 Medium Density Advance Line Selection Guide

Part number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity						I ² S	Comp.	PWM	ADC	RTC	EBI	ISP ICP	Package
							UART	SPI	I ² C	USB	LIN	CAN								
NUC100LD3AN	64 KB	16 KB	4 KB	4 KB	up to 35	4x32-bit	2	1	2	-	-	-	1	1	6	8x12-bit	v	-	v	LQFP48
NUC100LE3AN	128 KB	16 KB	Definable	4 KB	up to 35	4x32-bit	2	1	2	-	-	-	1	1	6	8x12-bit	v	-	v	LQFP48
NUC100RD3AN	64 KB	16 KB	4 KB	4 KB	up to 49	4x32-bit	3	2	2	-	-	-	1	2	6	8x12-bit	v	-	v	LQFP64
NUC100RE3AN	128 KB	16 KB	Definable	4 KB	up to 49	4x32-bit	3	2	2	-	-	-	1	2	6	8x12-bit	v	-	v	LQFP64
NUC100VD2AN	64 KB	8 KB	4 KB	4 KB	up to 80	4x32-bit	3	4	2	-	-	-	1	2	8	8x12-bit	v	-	v	LQFP100
NUC100VD3AN	64 KB	16 KB	4 KB	4 KB	up to 80	4x32-bit	3	4	2	-	-	-	1	2	8	8x12-bit	v	-	v	LQFP100
NUC100VE3AN	128 KB	16 KB	Definable	4 KB	up to 80	4x32-bit	3	4	2	-	-	-	1	2	8	8x12-bit	v	-	v	LQFP100

3.1.2 NuMicro™ NUC100 Low Density Advance Line Selection Guide

Part number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity						I ² S	Comp.	PWM	ADC	RTC	EBI	ISP ICP	Package
							UART	SPI	I ² C	USB	LIN	CAN								
NUC100LC1BN	32 KB	4 KB	4 KB	4 KB	up to 35	4x32-bit	2	1	2	-	-	-	1	1	4	8x12-bit	v	-	v	LQFP48
NUC100LD1BN	64 KB	4 KB	4 KB	4 KB	up to 35	4x32-bit	2	1	2	-	-	-	1	1	4	8x12-bit	v	-	v	LQFP48
NUC100LD2BN	64 KB	8 KB	4 KB	4 KB	up to 35	4x32-bit	2	1	2	-	-	-	1	1	4	8x12-bit	v	-	v	LQFP48
NUC100RC1BN	32 KB	4 KB	4 KB	4 KB	up to 49	4x32-bit	2	2	2	-	-	-	1	2	4	8x12-bit	v	v	v	LQFP64
NUC100RD1BN	64 KB	4 KB	4 KB	4 KB	up to 49	4x32-bit	2	2	2	-	-	-	1	2	4	8x12-bit	v	v	v	LQFP64
NUC100RD2BN	64 KB	8 KB	4 KB	4 KB	up to 49	4x32-bit	2	2	2	-	-	-	1	2	4	8x12-bit	v	v	v	LQFP64



3.2 Pin Configuration

3.2.1 NuMicro™ NUC100 Medium Density Pin Diagram

3.2.1.1 NuMicro™ NUC100 Medium Density LQFP 100 pin

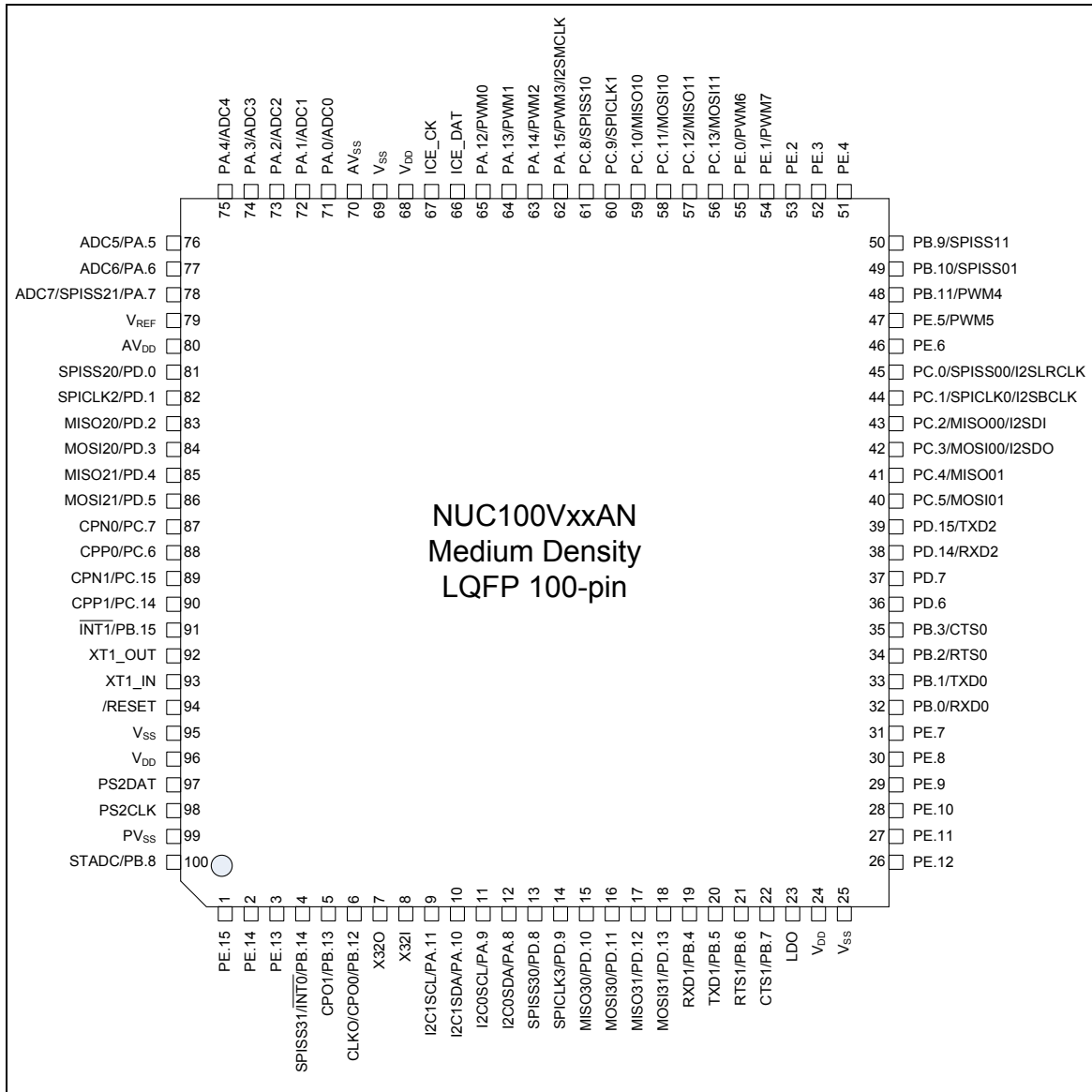


Figure 3-1 NuMicro™ NUC100 Medium Density LQFP 100-pin Pin Diagram



3.2.1.2 NuMicro™ NUC100 Medium Density LQFP 64 pin

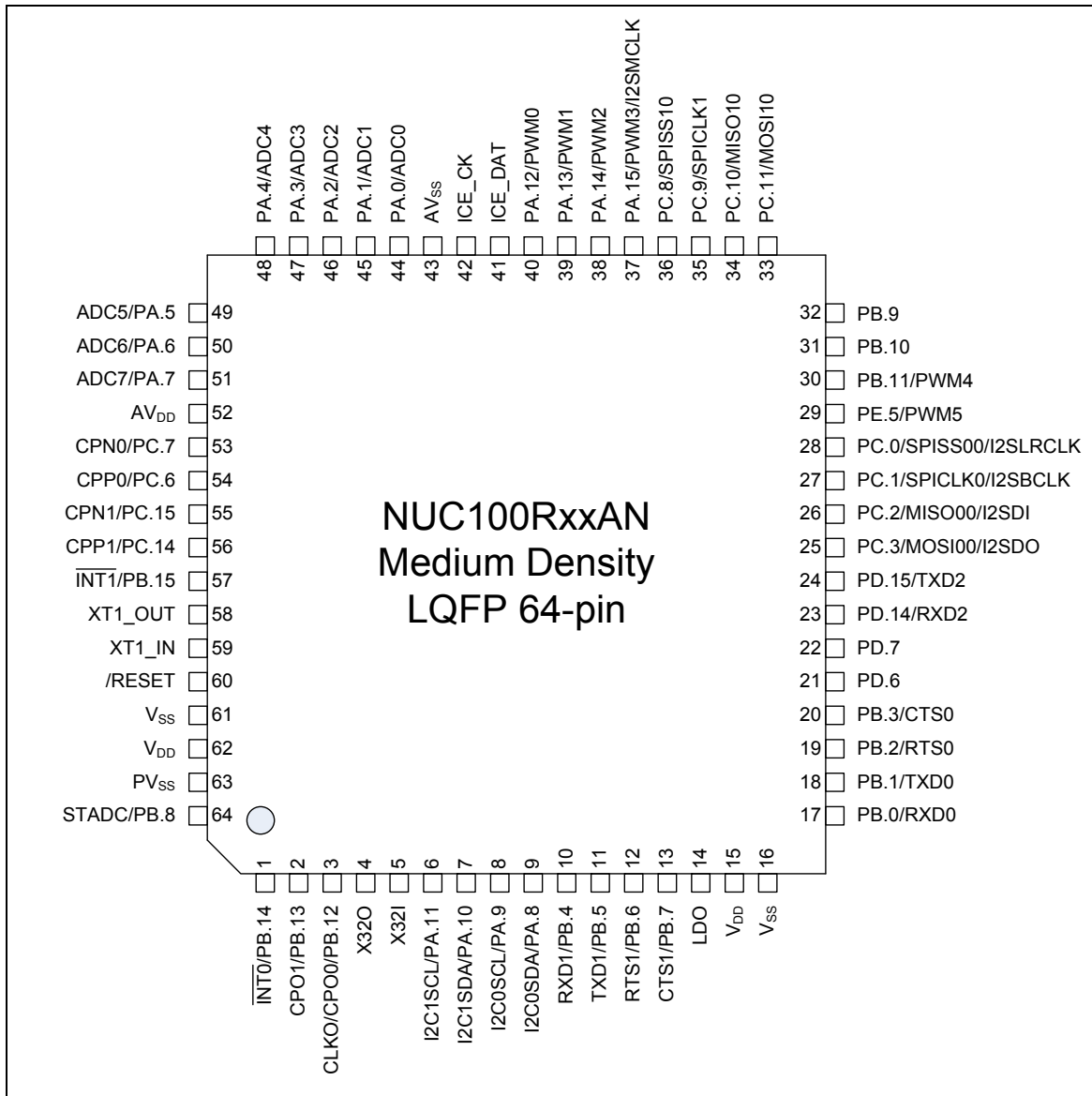


Figure 3-2 NuMicro™ NUC100 Medium Density LQFP 64-pin Pin Diagram



3.2.1.3 NuMicro™ NUC100 Medium Density LQFP 48 pin

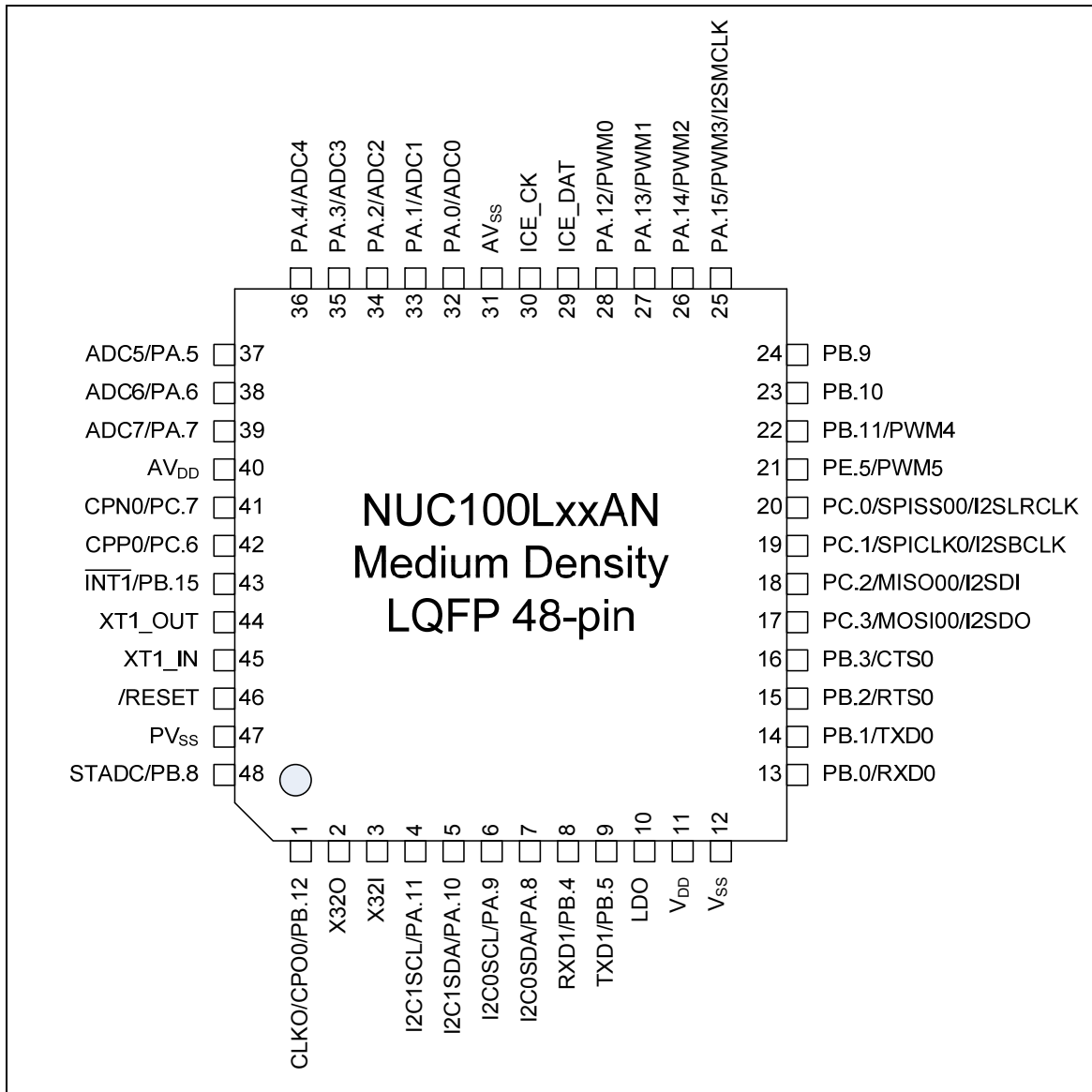


Figure 3-3 NuMicro™ NUC100 Medium Density LQFP 48-pin Pin Diagram

3.2.2 NuMicro™ NUC100 Low Density Pin Diagram

3.2.2.1 NuMicro™ NUC100 Low Density LQFP 64 pin

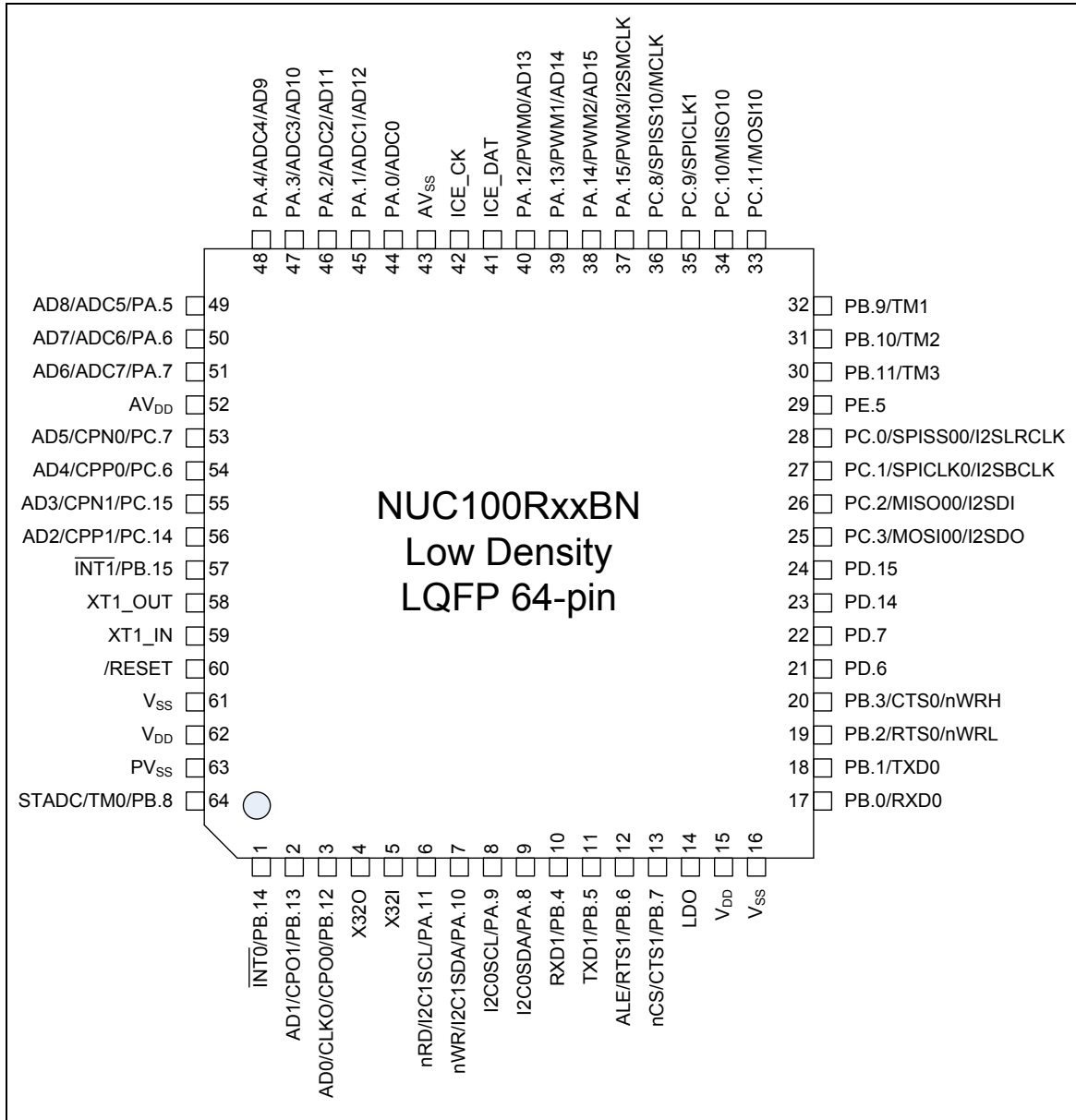


Figure 3-4 NuMicro™ NUC100 Low Density LQFP 64-pin Pin Diagram

3.2.2.2 NuMicro™ NUC100 Low Density LQFP 48 pin

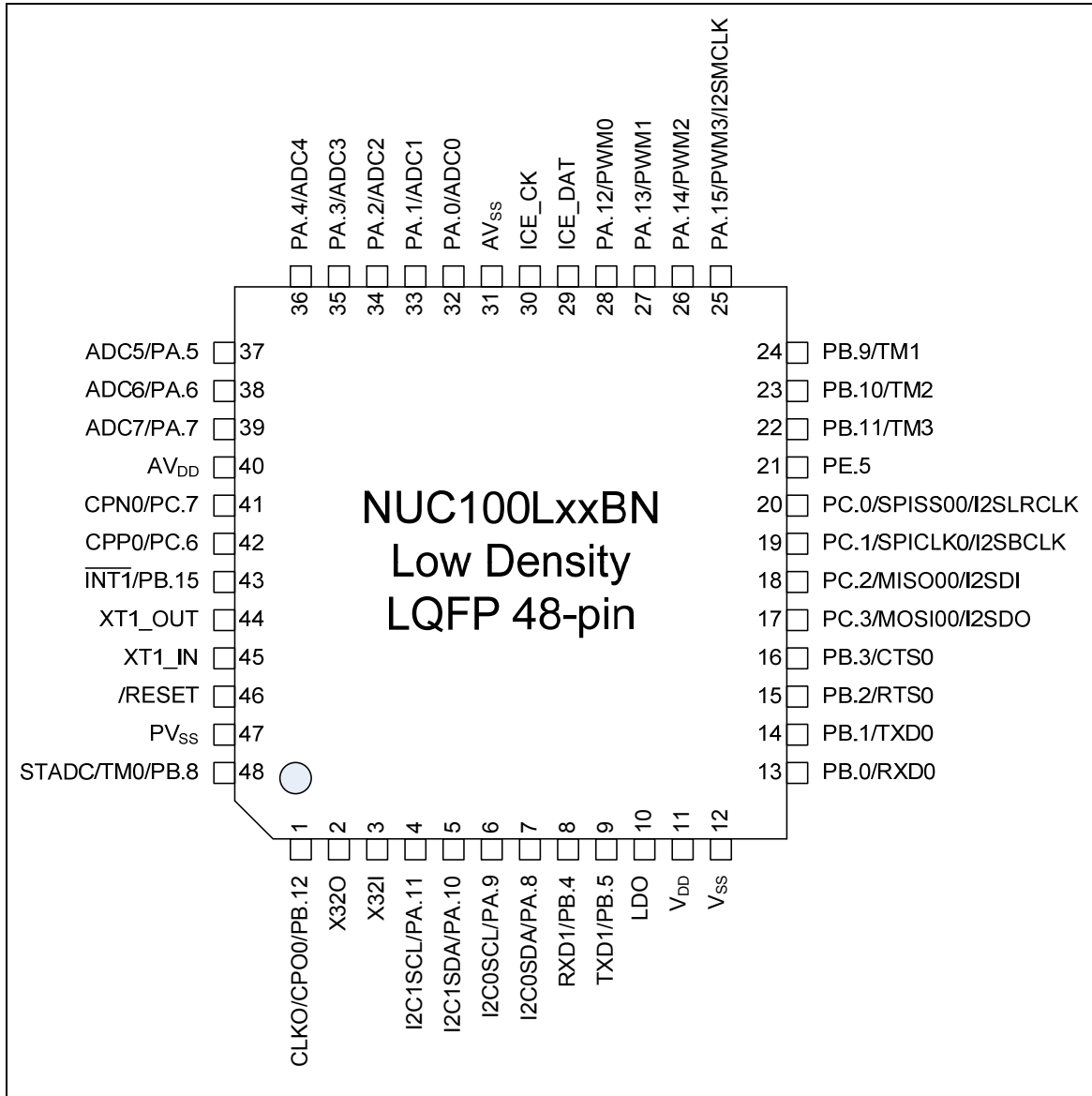


Figure 3-5 NuMicro™ NUC100 Low Density LQFP 48-pin Pin Diagram

4 BLOCK DIAGRAM

4.1 NuMicro™ NUC100 Medium Density Block Diagram

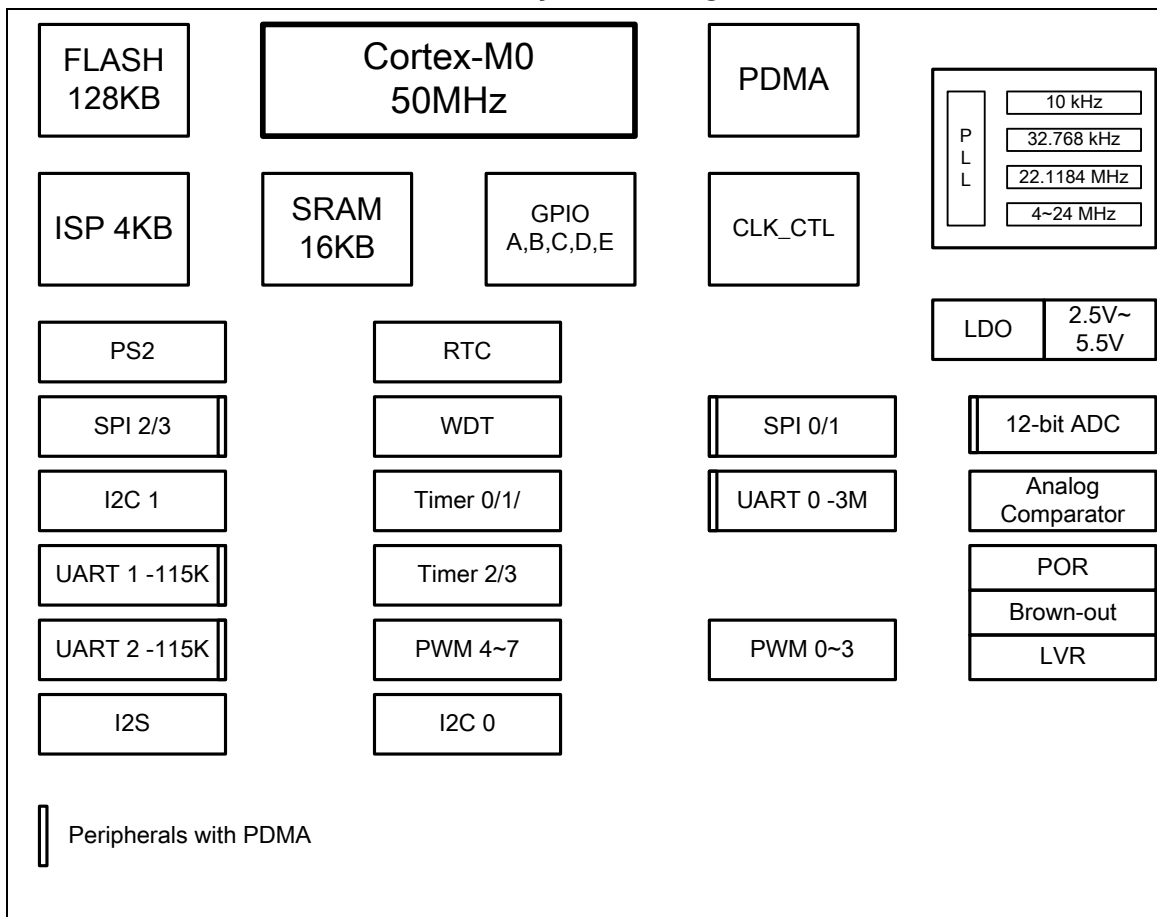


Figure 4-1 NuMicro™ NUC100 Medium Density Block Diagram

4.2 NuMicro™ NUC100 Low Density Block Diagram

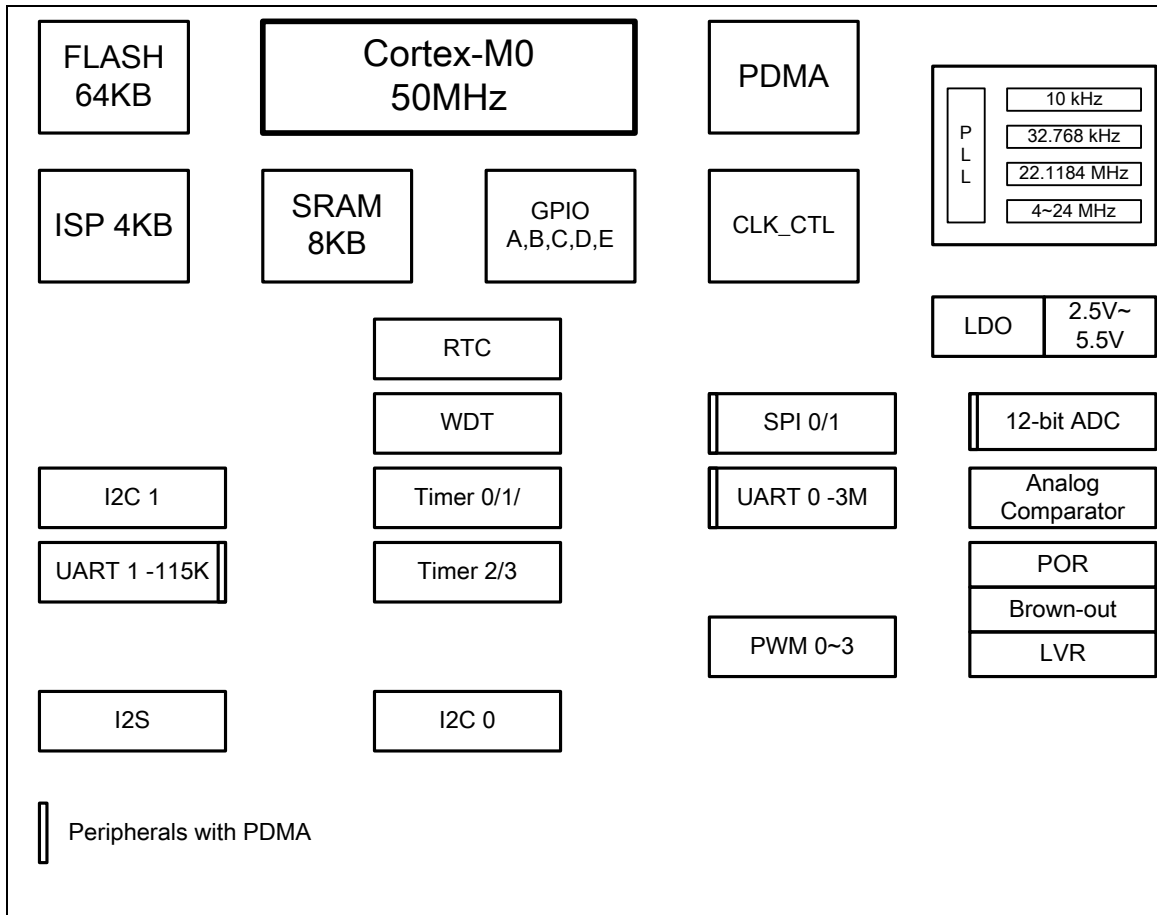


Figure 4-2 NuMicro™ NUC100 Low Density Block Diagram

5 FUNCTIONAL DESCRIPTION

5.1 ARM® Cortex™-M0 Core

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 5-1 shows the functional controller of processor.

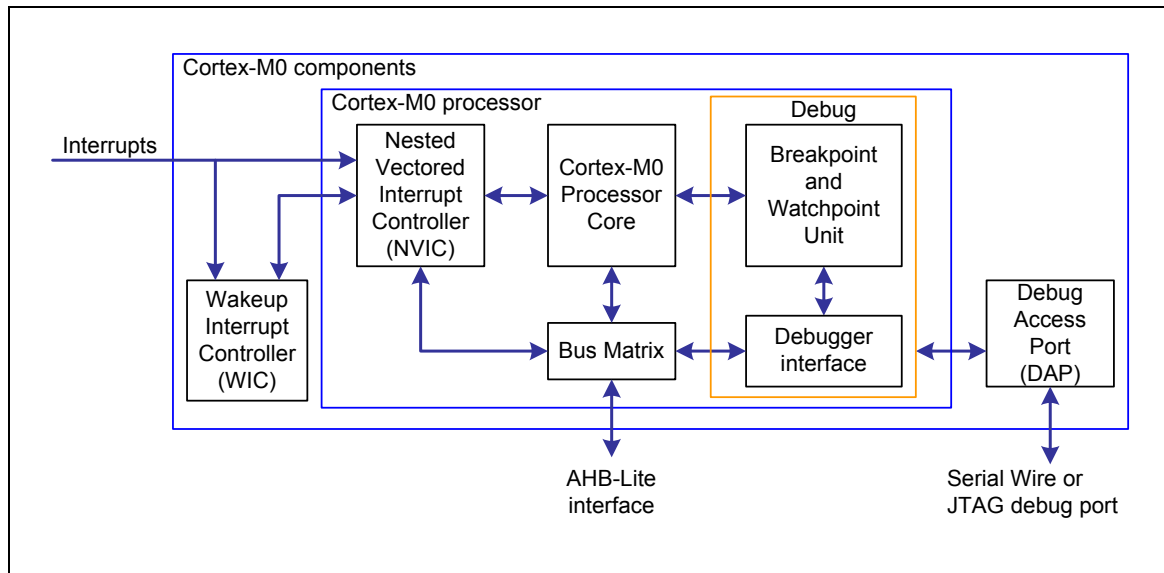


Figure 5-1 Functional Controller Diagram

The implemented device provides:

- A low gate count processor that features:
 - ◆ The ARMv6-M Thumb® instruction set
 - ◆ Thumb-2 technology
 - ◆ ARMv6-M compliant 24-bit SysTick timer
 - ◆ A 32-bit hardware multiplier
 - ◆ The system interface supports little-endian data accesses
 - ◆ The ability to have deterministic, fixed-latency, interrupt handling
 - ◆ Load/store-multiples and multicycle-multiples that can be abandoned and restarted to facilitate rapid interrupt handling
 - ◆ C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
 - ◆ Low power sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature

- NVIC that features:
 - ◆ 32 external interrupt inputs, each with four levels of priority
 - ◆ Dedicated Non-Maskable Interrupt (NMI) input.
 - ◆ Support for both level-sensitive and pulse-sensitive interrupt lines
 - ◆ Wake-up Interrupt Controller (WIC), providing ultra-low power sleep mode support.
- Debug support
 - ◆ Four hardware breakpoints.
 - ◆ Two watchpoints.
 - ◆ Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
 - ◆ Single step and vector catch capabilities.
- Bus interfaces:
 - ◆ Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
 - ◆ Single 32-bit slave port that supports the DAP (Debug Access Port).

5.2 System Manager

5.2.1 Overview

System management includes these following sections:

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

5.2.2 System Reset

The system reset can be issued by one of the below listed events. For these reset event flags can be read by RSTSRC register.

- The Power-On Reset
- The low level on the /RESET pin
- Watchdog Time Out Reset
- Low Voltage Reset
- Brown-Out Detector Reset
- CPU Reset
- System Reset

System Reset and Power-On Reset all reset the whole chip including all peripherals. The difference between System Reset and Power-On Reset is external crystal circuit and ISPCON.BS bit. System Reset doesn't reset external crystal circuit and ISPCON.BS bit, but Power-On Reset does.

5.2.3 System Power Distribution

In this chip, the power distribution is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 2.5 V power for digital operation and I/O pins.

The outputs of internal voltage regulators, LDO and V_{DD33} , require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 5-2 shows the power distribution of NuMicro™ NUC100.

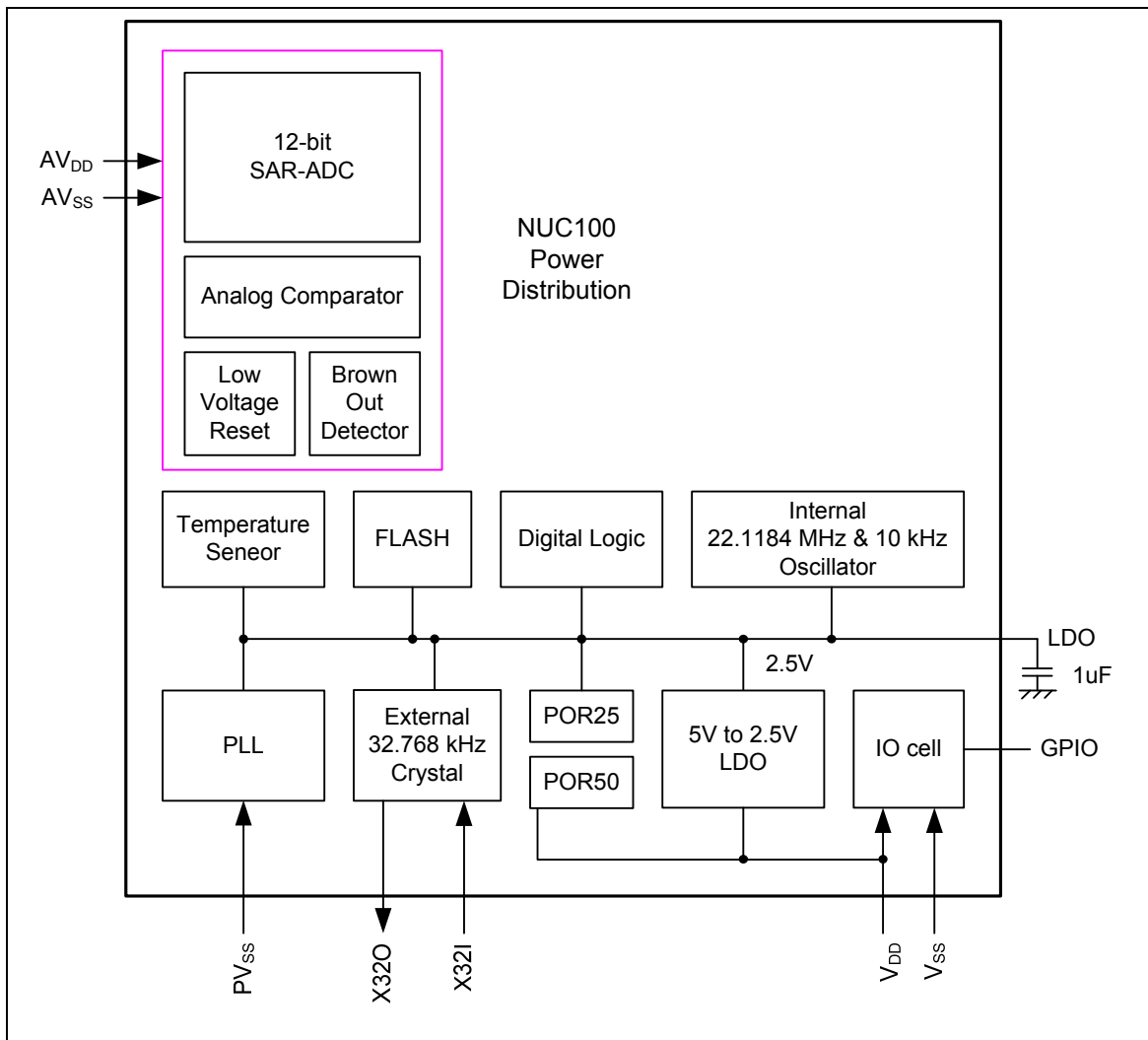


Figure 5-2 NuMicro™ NUC100 Power Distribution Diagram



5.2.4 System Memory Map

NuMicro™ NUC100 Series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in the following table. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip peripherals. NuMicro™ NUC100 Series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	FLASH Memory Space (128KB)
0x2000_0000 – 0x2000_3FFF	SRAM_BA	SRAM Memory Space (16KB)
0x6000_0000 – 0x6001_FFFF	EXTMEM_BA	External Memory Space (128KB) (NuMicro™ NUC100/NUC120 Low Density 64-pin Only)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	PDMA_BA	Peripheral DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_03FF	EBI_BA	External Bus Interface Control Registers (NuMicro™ NUC100/NUC120 Low Density 64-pin Only)
APB1 Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4000_8000 – 0x4000_BFFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I ² C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWMA_BA	PWM0/1/2/3 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4006_0000 – 0x4006_3FFF	USBD_BA	USB 2.0 FS device Controller Registers
0x400D_0000 – 0x400D_3FFF	ACMP_BA	Analog Comparator Control Registers



Address Space	Token	Controllers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
APB2 Controllers Space (0x4010_0000 ~ 0x401F_FFFF)		
0x4010_0000 – 0x4010_3FFF	PS2_BA	PS/2 Interface Control Registers
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I ² C1 Interface Control Registers
0x4013_0000 – 0x4013_3FFF	SPI2_BA	SPI2 with master/slave function Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x4013_4000 – 0x4013_7FFF	SPI3_BA	SPI3 with master/slave function Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x4014_0000 – 0x4014_3FFF	PWMB_BA	PWM4/5/6/7 Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4015_4000 – 0x4015_7FFF	UART2_BA	UART2 Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x401A_0000 – 0x401A_3FFF	I2S_BA	I ² S Interface Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 5-1 Address Space Assignments for On-Chip Controllers