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**ARM® Cortex®-M0  
32-bit Microcontroller**

**NuMicro® Family  
NUC123 Series  
Datasheet**

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## 1 GENERAL DESCRIPTION

The NuMicro® NUC123 series is a new 32-bit Cortex®-M0 microcontroller with USB 2.0 Full-speed devices and a 10-bit ADC. The NUC123 series provides the high 72 MHz operating speed, large 20 Kbytes SRAM, 8 USB endpoints and three sets of SPI controllers, which make it powerful in USB communication and data processing. The NUC123 series is ideal for industrial control, consumer electronics, and communication system applications such as printers, touch panel, gaming keyboard, gaming joystick, USB audio, PC peripherals, and alarm systems.

The NUC123 series runs up to 72 MHz and supports 32-bit multiplier, structure NVIC (Nested Vector Interrupt Control), dual-channel APB and PDMA (Peripheral Direct Memory Access) with CRC function. Besides, the NUC123 series is equipped with 36/68 Kbytes Flash memory, 12/20 Kbytes SRAM, and 4 Kbytes loader ROM for the ISP. It operates at a wide voltage range of 2.5V ~ 5.5V and temperature range of -40°C ~ +105°C and -40°C ~ +85°C. It is also equipped with plenty of peripheral devices, such as 8-channel 10-bit ADC, UART, SPI, I<sup>2</sup>C, I<sup>2</sup>S, USB 2.0 FS devices, and offers low-voltage reset and Brown-out detection, PWM (Pulse-width Modulation), capture and compare features, four sets of 32-bit timers, Watchdog Timer, and internal RC oscillator. All these peripherals have been incorporated into the NUC123 series to reduce component count, board space and system cost.

Additionally, the NUC123 series is equipped with ISP (In-System Programming), IAP (In-Application-Programming) and ICP (In-Circuit Programming) functions, which allows the user to update the program under software control through the on-chip connectivity interface, such as SWD, UART and USB.

Product Line	UART	SPI	I <sup>2</sup> C	USB	PS/2	I <sup>2</sup> S	PWM	ADC
NUC123	2	3	2	1	1	1	4	8

Table 1-1 Key Features Support Table

## 2 FEATURES

### 2.1 NuMicro® NUC123 Series Features

- Core
  - ARM® Cortex®-M0 core runs up to 72 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Supports Serial Wire Debug with 2 watchpoints/4 breakpoints
- Built-in LDO for wide operating voltage ranges from 2.5 V to 5.5 V
- Flash Memory
  - 36/68 KB Flash for program code
  - 4 KB flash for ISP loader
  - Supports In-System Program (ISP) application code update
  - 512 byte page erase for flash
  - Configurable Data Flash address and size for both 36KB and 68KB system
  - Supports 2-wire ICP update through SWD/ICE interface
  - Supports fast parallel programming mode by external programmer
- SRAM Memory
  - 12/20 KB embedded SRAM
  - Supports PDMA mode
- PDMA (Peripheral DMA)
  - Supports 6 channels PDMA for automatic data transfer between SRAM and peripherals such as SPI, UART, I<sup>2</sup>S, USB 2.0 FS device, PWM and ADC
  - Supports CRC calculation with four common polynomials, CRC-CCITT, CRC-8, CRC-16 and CRC-32
- Clock Control
  - Flexible selection for different applications
  - Built-in 22.1184 MHz high speed oscillator (Trimmed to 1%) for system operation, and low power 10 kHz low speed oscillator for watchdog and wake-up operation
  - Supports one PLL, up to 144 MHz, for high performance system operation
  - External 4~24 MHz high speed crystal input for precise timing operation
- GPIO
  - Four I/O modes:
    - ◆ Quasi bi-direction
    - ◆ Push-Pull output
    - ◆ Open-Drain output
    - ◆ Input only with high impedance
  - TTL/Schmitt trigger input selectable
  - I/O pin configured as interrupt source with edge/level setting
  - Supports High Driver and High Sink I/O mode
- Timer
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent clock source for each timer
  - Provides one-shot, periodic, toggle and continuous counting operation modes
  - Supports event counting function
- Watchdog/Windowed-Watchdog Timer
  - Multiple clock sources

- 8 selectable time-out period from 1.6ms ~ 26.0sec (depending on clock source)
- Wake-up from Power-down or Idle mode
- Interrupt or reset selectable on watchdog timer time-out
- Interrupt on windowed-watchdog timer time-out
- Reset on windowed-watchdog timer time-out or reload in an unexpected time window
- PWM/Capture
  - Up to two built-in 16-bit PWM generators provided with four PWM outputs or two complementary paired PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-zone generator for complementary paired PWM
  - Up to four 16-bit digital Capture timers (shared with PWM timers) provided with four rising/falling capture inputs
  - Supports Capture interrupt
- UART
  - Up to two UART controllers
  - UART ports with flow control (TXD, RXD, CTS and RTS)
  - UART0/1 with 16-byte FIFO for standard device
  - Support IrDA (SIR) function
  - Supports RS-485 9-bit mode and direction control.
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports PDMA mode
- SPI
  - Up to three sets of SPI controllers
  - Supports SPI master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Up to two slave/device select lines in Master mode
  - Supports Byte Suspend mode in 16/24/32-bit transmission
  - Supports PDMA transfer
- I<sup>2</sup>C
  - Up to two sets of I<sup>2</sup>C devices
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allowing versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports wake-up by address recognition (for 1st slave address only)
- I<sup>2</sup>S
  - Interface with external audio CODEC
  - Operated as either master or Slave mode
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Supports Mono and stereo audio data
  - Supports I<sup>2</sup>S and MSB justified data format
  - Two 8 word FIFO data buffers are provided, one for transmitting and the other for receiving

- Generates interrupt requests when buffer levels cross a programmable boundary
- Supports two DMA requests, one for transmitting and the other for receiving
- PS/2 Device Controller
  - Host communication inhibit and request to send detection
  - Reception frame error detection
  - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
  - Double buffer for data reception
  - S/W override bus
- USB 2.0 Full-Speed Device
  - One set of USB 2.0 FS Device 12 Mbps
  - On-chip USB transceiver
  - Provides 1 interrupt source with 4 interrupt events
  - Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provides 8 programmable endpoints
  - Includes 512 bytes internal SRAM as USB buffer
  - Provides remote wake-up capability
- ADC
  - 10-bit SAR ADC with 150K SPS (for NUC123xxxANx)
  - 10-bit SAR ADC with 200K SPS (for NUC123xxxAEx)
  - Up to 8-ch single-end input
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion start by software programming or external input
  - Supports PDMA mode
- Brown-out detector
  - With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage levels: 2.0 V
- One built-in LDO
- Operating Temperature: -40°C ~85°C (for NUC123xxxANx)
- Operating Temperature: -40°C ~105°C (for NUC123xxxAEx)
- Packages:
  - All Green package (RoHS)
  - LQFP 64-pin
  - LQFP 48-pin
  - QFN 33-pin

### 3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~20 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface

SPS	Samples per Second
TDES	Triple Data Encryption Standard
TK	Touch Key
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations

## 4 PARTS INFORMATION LIST AND PIN CONFIGURATION

### 4.1 NuMicro® NUC123 Series Naming Rule

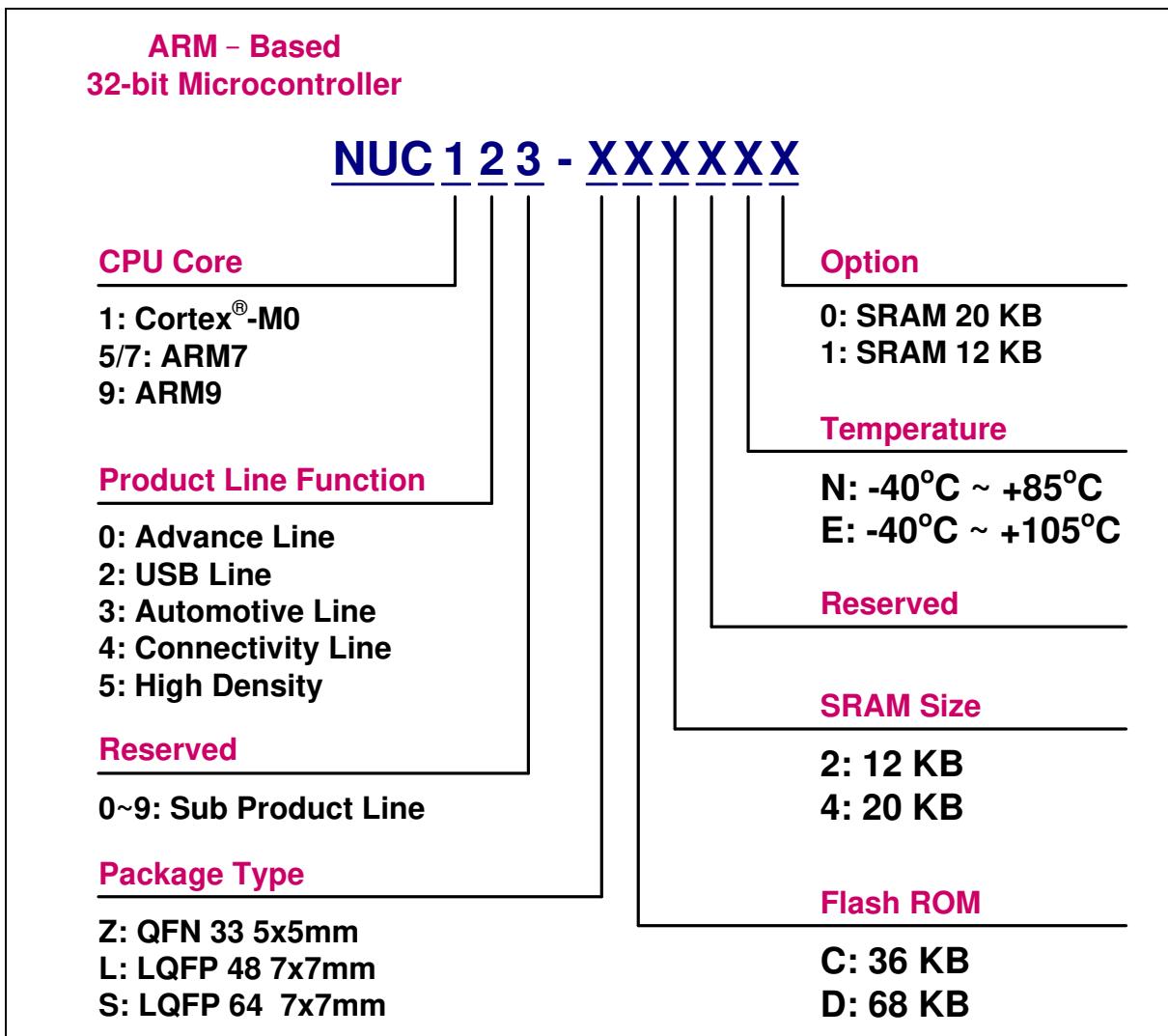


Figure 4-1 NuMicro® NUC123 Series Selection Code

## 4.2 NuMicro® NUC123 Series Selection Guide

### 4.2.1 NuMicro® NUC123xxxANx Selection Guide

Part Number	Flash (KB)	SRAM (KB)	ISP ROM (KB)	I/O	Timer	Connectivity						PS/2	I <sup>2</sup> S	Comp.	PWM	ADC	RTC	EBI	ISP\ICP\IAP	1.8V Power Pin	Package
						UART	SPI	I <sup>2</sup> C	USB	LIN											
NUC123ZD4AN0	68	20	4	Up to 20	4x32-bit	1	3	1	1	-	-	1	-	2	3x10-bit	-	-	v	-	QFN33	
NUC123ZC2AN1	36	12	4	up to 20	4x32-bit	1	3	1	1	-	-	1	-	2	3x10-bit	-	-	v	-	QFN33	
NUC123LD4AN0	68	20	4	up to 36	4x32-bit	2	3	2	1	-	1	1	1	4	8x10-bit	-	-	v	-	LQFP48	
NUC123LC2AN1	36	12	4	up to 36	4x32-bit	2	3	2	1	-	1	1	1	4	8x10-bit	-	-	v	-	LQFP48	
NUC123SD4AN0	68	20	4	up to 47	4x32-bit	2	3	2	1	-	1	1	1	4	8x10-bit	-	-	v	-	LQFP64	
NUC123SC2AN1	36	12	4	up to 47	4x32-bit	2	3	2	1	-	1	1	1	4	8x10-bit	-	-	v	-	LQFP64	

### 4.2.2 NuMicro® NUC123xxxAEx Selection Guide

Part Number	Flash (KB)	SRAM (KB)	ISP ROM (KB)	I/O	Timer	Connectivity						PS/2	I <sup>2</sup> S	Comp.	PWM	ADC	RTC	EBI	ISP\ICP\IAP	1.8V Power Pin	Package
						UART	SPI	I <sup>2</sup> C	USB	LIN											
NUC123ZD4AE0	68	20	4	Up to 20	4x32-bit	1	3	1	1	-	-	1	-	3	3x10-bit	-	-	v	-	QFN33	
NUC123ZC2AE1	36	12	4	up to 20	4x32-bit	1	3	1	1	-	-	1	-	3	3x10-bit	-	-	v	-	QFN33	
NUC123LD4AE0	68	20	4	up to 36	4x32-bit	2	3	2	1	-	1	1	1	4	8x10-bit	-	-	v	-	LQFP48	
NUC123LC2AE1	36	12	4	up to 36	4x32-bit	2	3	2	1	-	1	1	1	4	8x10-bit	-	-	v	-	LQFP48	
NUC123SD4AE0	68	20	4	up to 47	4x32-bit	2	3	2	1	-	1	1	1	4	8x10-bit	-	-	v	-	LQFP64	
NUC123SC2AE1	36	12	4	up to 47	4x32-bit	2	3	2	1	-	1	1	1	4	8x10-bit	-	-	v	-	LQFP64	

## 4.3 NuMicro® NUC123 Series Pin Configuration

### 4.3.1 NuMicro® NUC123xxxANx Pin Diagram

#### 4.3.1.1 NuMicro® NUC123SxxANx LQFP 64 pin

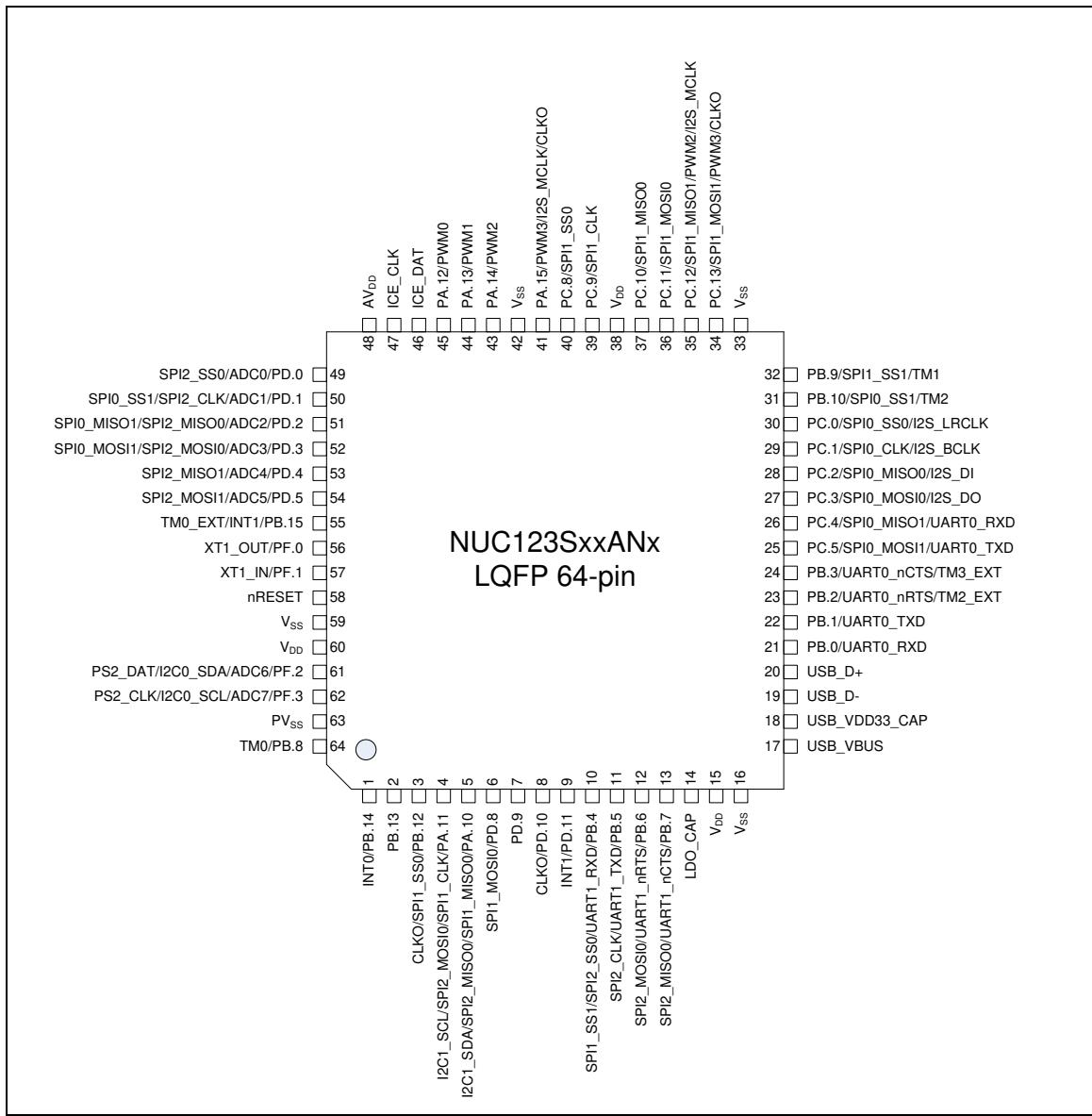


Figure 4-2 NuMicro® NUC123SxxANx LQFP 64-pin Diagram

## 4.3.1.2

## NuMicro® NUC123LxxANx LQFP 48 pin

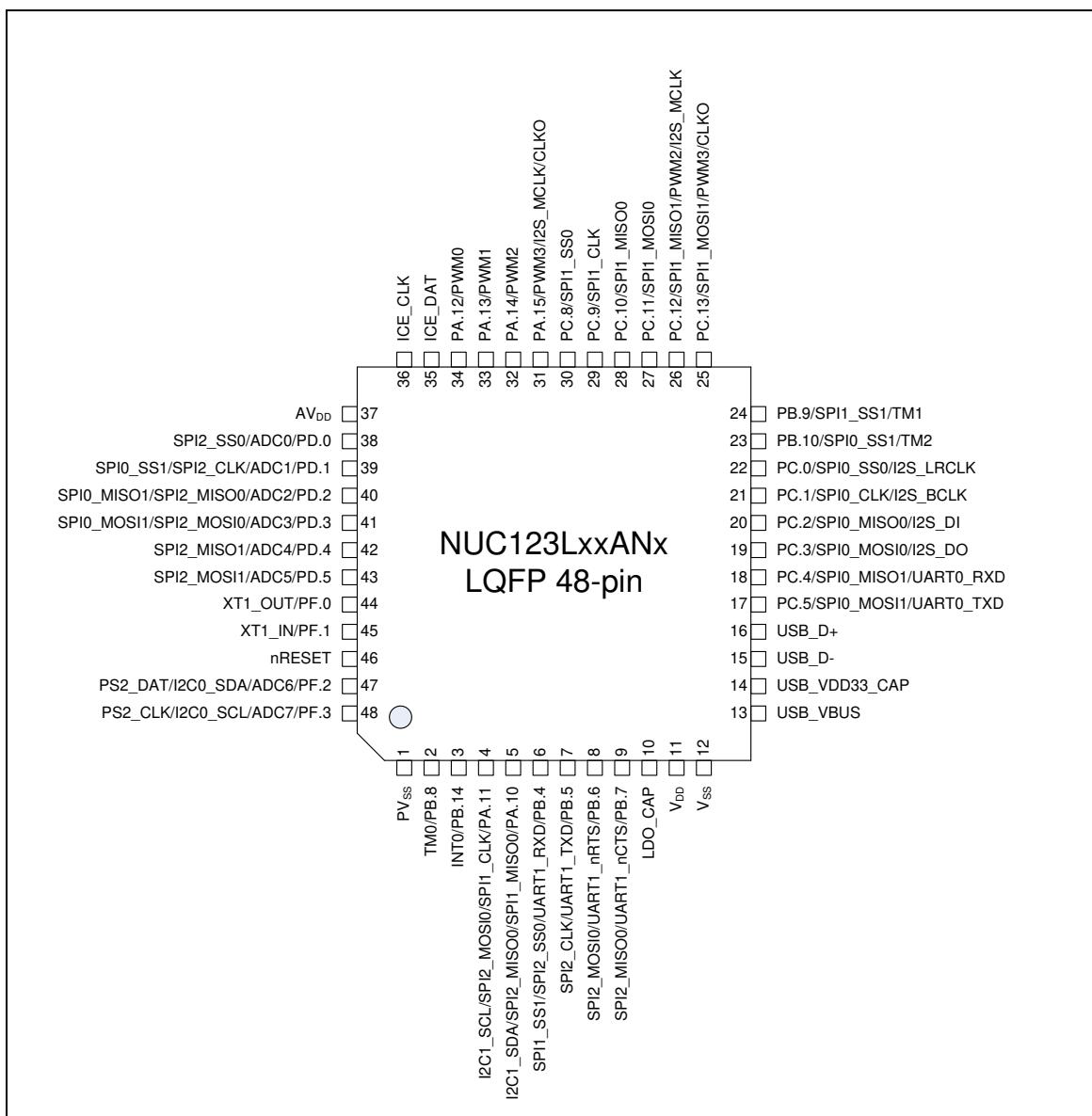


Figure 4-3 NuMicro® NUC123LxxANx LQFP 48-pin Diagram

## 4.3.1.3

## NuMicro® NUC123ZxxANx QFN 33 pin

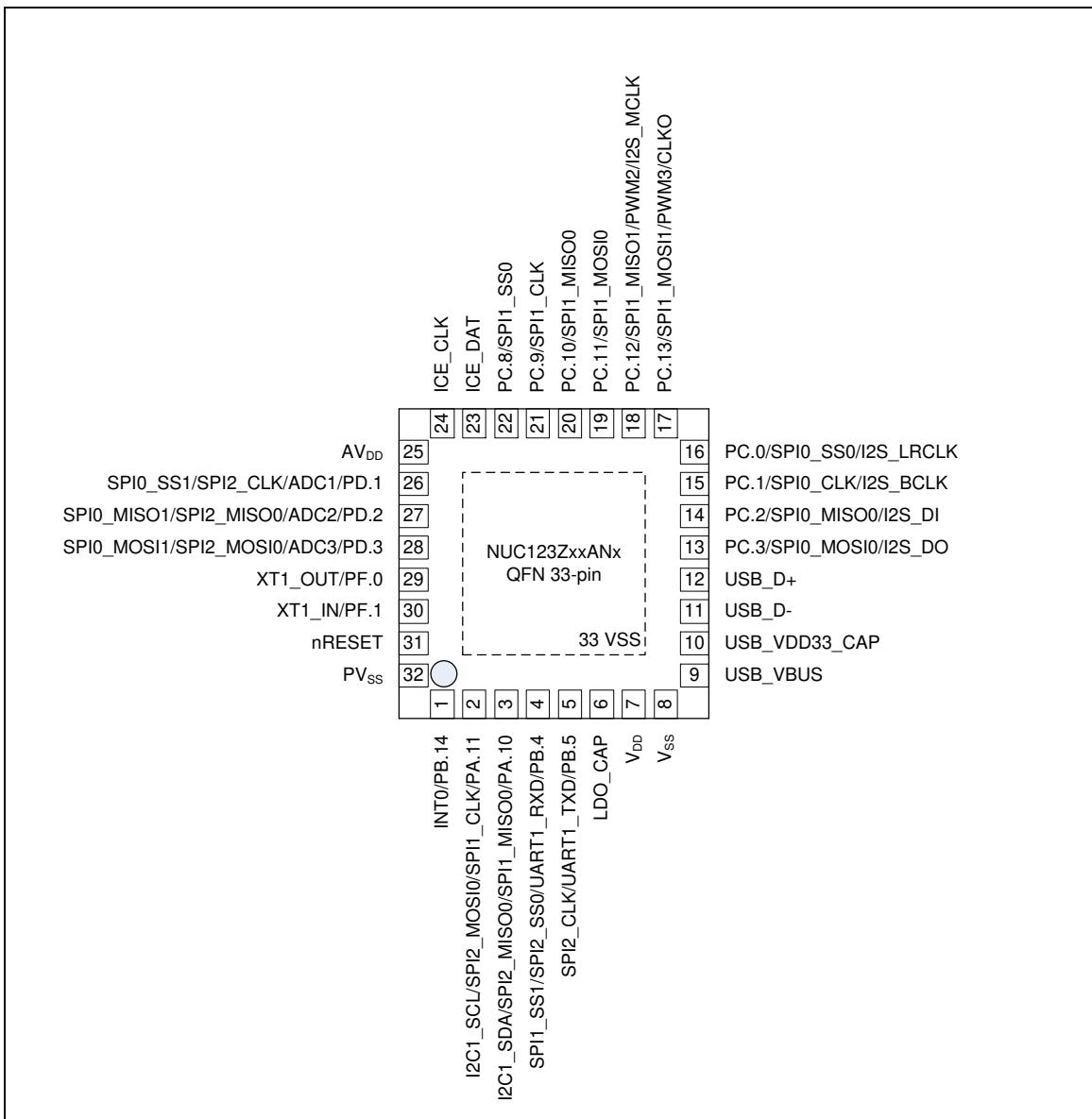


Figure 4-4 NuMicro® NUC123ZxxANx QFN 33-pin Diagram

### 4.3.2 NuMicro® NUC123xxxAEx Pin Diagram

#### 4.3.2.1 NuMicro® NUC123SxxAEx LQFP 64 pin

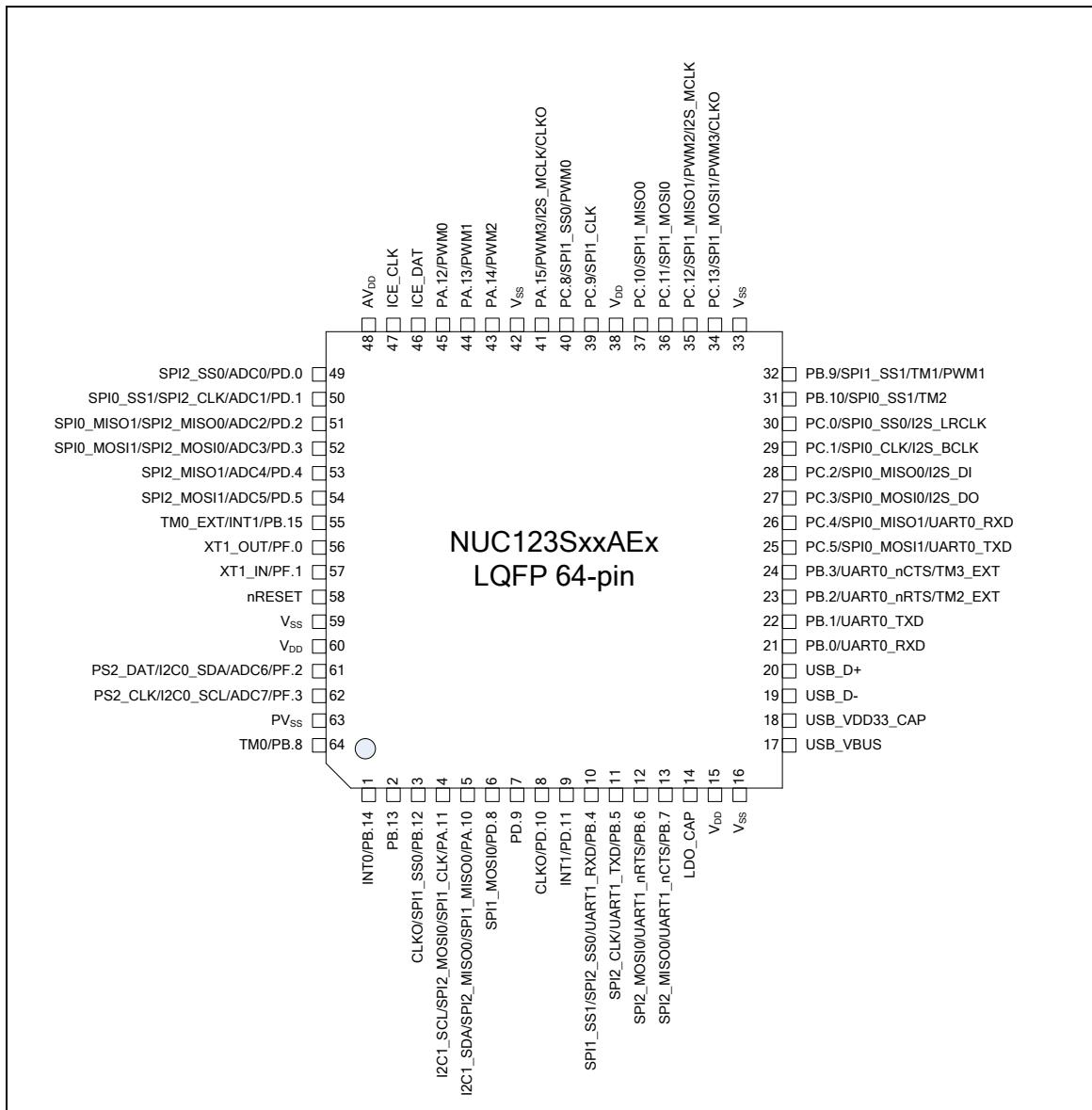


Figure 4-5 NuMicro® NUC123SxxAEx LQFP 64-pin Diagram

## 4.3.2.2

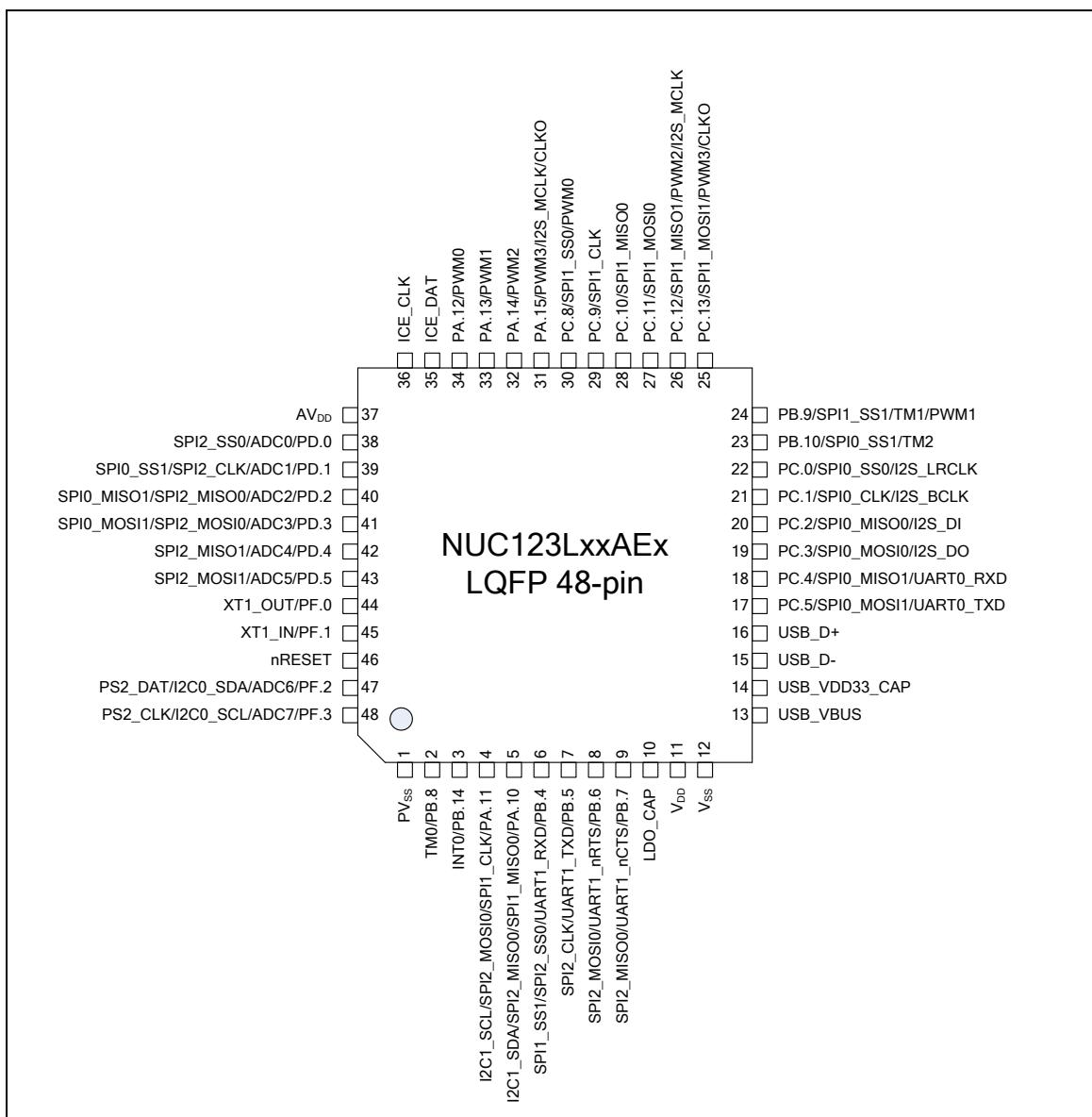
*NuMicro® NUC123LxxAEx LQFP 48 pin*

Figure 4-6 NuMicro® NUC123LxxAEx LQFP 48-pin Diagram

## 4.3.2.3

## NuMicro® NUC123ZxxAEx QFN 33 pin

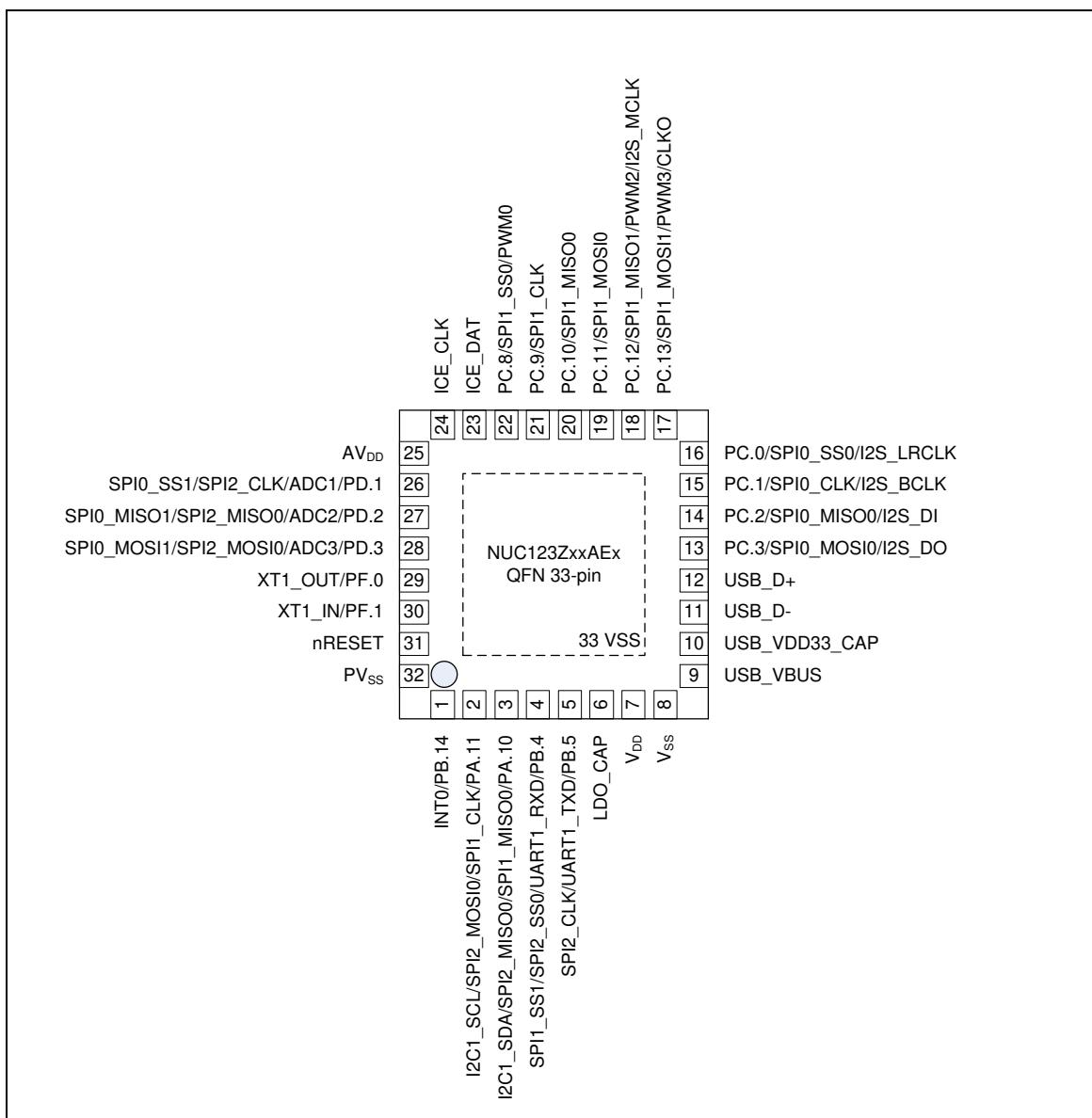


Figure 4-7 NuMicro® NUC123ZxxAEx QFN 33-pin Diagram

## 4.4 Pin Description

### 4.4.1 NuMicro® NUC123 Pin Description

Pin No			Pin Name	Type	Description
LQFP 64-pin	LQFP 48-pin	QFN 33-pin			
1	3	1	PB.14	I/O	Digital GPIO pin
			INT0	I	External interrupt 0 input pin
2			PB.13	I/O	Digital GPIO pin
3			PB.12	I/O	Digital GPIO pin
			SPI1_SS0	I/O	SPI1 1 <sup>st</sup> slave select pin
			CLKO	O	Frequency Divider output pin
4	4	2	PA.11	I/O	Digital GPIO pin
			SPI1_CLK	I/O	SPI1 serial clock pin
			SPI2_MOSI0	I/O	SPI2 1 <sup>st</sup> MOSI (Master Out, Slave In) pin
			I2C1_SCL	I/O	I <sup>2</sup> C1 clock pin
5*	5*	3*	PA.10	I/O	Digital GPIO pin
			SPI1_MISO0	I/O	SPI1 1 <sup>st</sup> MISO (Master In, Slave Out) pin
			SPI2_MISO0	I/O	SPI2 1 <sup>st</sup> MISO (Master In, Slave Out) pin
			I2C1_SDA	I/O	I <sup>2</sup> C1 data input/output pin
6			PD.8	I/O	Digital GPIO pin
			SPI1_MOSI0	I/O	SPI1 1 <sup>st</sup> MOSI (Master Out, Slave In) pin
7			PD.9	I/O	Digital GPIO pin
8			PD.10	I/O	Digital GPIO pin
			CLKO	O	Frequency Divider output pin
9			PD.11	I/O	Digital GPIO pin
			INT1	I	External interrupt 1 input pin
10	6	4	PB.4	I/O	Digital GPIO pin
			UART1_RXD	I	UART1 data receiver input pin
			SPI2_SS0	I/O	SPI2 1 <sup>st</sup> slave select pin
			SPI1_SS1	I/O	SPI1 2 <sup>nd</sup> slave select pin
11	7	5	PB.5	I/O	Digital GPIO pin
			UART1_TXD	O	UART1 data transmitter output pin
			SPI2_CLK	I/O	SPI2 serial clock pin
12	8		PB.6	I/O	Digital GPIO pin
			UART1_nRTS	O	UART1 request to send output pin

			SPI2_MOSI0	I/O	SPI2 1 <sup>st</sup> MOSI (Master Out, Slave In) pin
13	9		PB.7	I/O	Digital GPIO pin
			UART1_nCTS	I	UART1 clear to send input pin
			SPI2_MISO0	I/O	SPI2 1 <sup>st</sup> MISO (Master In, Slave Out) pin
14	10	6	LDO_CAP	P	LDO output pin
15	11	7	V <sub>DD</sub>	P	Power supply for I/O ports and LDO source for internal PLL and digital function. Voltage range is 2.5V ~ 5V.
16	12	8	V <sub>SS</sub>	P	Ground
17	13	9	USB_VBUS	USB	Power supply from USB host or hub
18	14	10	USB_VDD33_CAP	USB	Internal power regulator output 3.3V decoupling pin
19	15	11	USB_D-	USB	USB differential signal D-
20	16	12	USB_D+	USB	USB differential signal D+
21			PB.0	I/O	Digital GPIO pin
			UART0_RXD	I	UART0 data receiver input pin
22			PB.1	I/O	Digital GPIO pin
			UART0_TXD	O	UART0 data transmitter output pin
23			PB.2	I/O	Digital GPIO pin
			UART0_nRTS	O	UART0 request to send output pin
			TM2_EXT	I	Timer2 external capture input pin
24			PB.3	I/O	Digital GPIO pin
			UART0_nCTS	I	UART0 clear to send input pin
			TM3_EXT	I	Timer3 external capture input pin
25	17		PC.5	I/O	Digital GPIO pin
			SPI0_MOSI1	I/O	SPI0 2 <sup>nd</sup> MOSI (Master Out, Slave In) pin
			UART0_TXD	O	UART0 data transmitter output pin
26	18		PC.4	I/O	Digital GPIO pin
			SPI0_MISO1	I/O	SPI0 2 <sup>nd</sup> MISO (Master In, Slave Out) pin
			UART0_RXD	I	UART0 data receiver input pin
27	19	13	PC.3	I/O	Digital GPIO pin
			SPI0_MOSI0	I/O	SPI0 1 <sup>st</sup> MOSI (Master Out, Slave In) pin
			I2S_DO	O	I <sup>2</sup> S data output pin
28	20	14	PC.2	I/O	Digital GPIO pin
			SPI0_MISO0	I/O	SPI0 1 <sup>st</sup> MISO (Master In, Slave Out) pin
			I2S_DI	I	I <sup>2</sup> S data input pin
29	21	15	PC.1	I/O	Digital GPIO pin
			SPI0_CLK	I/O	SPI0 serial clock pin

			I2S_BCLK	I/O	$\text{i}^2\text{S}$ bit clock pin
30	22	16	PC.0	I/O	Digital GPIO pin
			SPI0_SS0	I/O	SPI0 1 <sup>st</sup> slave select pin
			I2S_LRCLK	I/O	$\text{i}^2\text{S}$ left/right channel clock pin
31	23		PB.10	I/O	Digital GPIO pin
			SPI0_SS1	I/O	SPI0 2 <sup>nd</sup> slave select pin
			TM2	I/O	Timer2 event counter input / toggle output pin
32	24		PB.9	I/O	Digital GPIO pin
			SPI1_SS1	I/O	SPI1 2 <sup>nd</sup> slave select pin
			TM1	I/O	Timer1 event counter input / toggle output pin
			PWM1	I/O	PWM1 PWM output / capture input pin (NUC123xxxAEx Only)
33			V <sub>SS</sub>	P	Ground
34	25	17	PC.13	I/O	Digital GPIO pin
			SPI1_MOSI1	I/O	SPI1 2 <sup>nd</sup> MOSI (Master Out, Slave In) pin
			PWM3	I/O	PWM3 PWM output / capture input pin
			CLKO	O	Frequency Divider output pin
35	26	18	PC.12	I/O	Digital GPIO pin
			SPI1_MISO1	I/O	SPI1 2 <sup>nd</sup> MISO (Master In, Slave Out) pin
			PWM2	I/O	PWM2 PWM output / capture input pin
			I2S_MCLK	O	$\text{i}^2\text{S}$ master clock output pin
36	27	19	PC.11	I/O	Digital GPIO pin
			SPI1_MOSI0	I/O	SPI1 1 <sup>st</sup> MOSI (Master Out, Slave In) pin
37	28	20	PC.10	I/O	Digital GPIO pin
			SPI1_MISO0	I/O	SPI1 1 <sup>st</sup> MISO (Master In, Slave Out) pin
38			V <sub>DD</sub>	P	Power supply for I/O ports and LDO source for internal PLL and digital function. Voltage range is 2.5V ~ 5V.
39	29	21	PC.9	I/O	Digital GPIO pin
			SPI1_CLK	I/O	SPI1 serial clock pin
40	30	22	PC.8	I/O	Digital GPIO pin
			SPI1_SS0	I/O	SPI1 1 <sup>st</sup> slave select pin
			PWM0	I/O	PWM0 PWM output / capture input pin (NUC123xxxAEx Only)
41	31		PA.15	I/O	Digital GPIO pin
			PWM3	I/O	PWM3 PWM output / capture input pin
			I2S_MCLK	O	$\text{i}^2\text{S}$ master clock output pin
			CLKO	O	Frequency Divider output pin

42			V <sub>SS</sub>	P	Ground
43	32		PA.14	I/O	Digital GPIO pin
			PWM2	I/O	PWM2 PWM output / capture input pin
44	33		PA.13	I/O	Digital GPIO pin
			PWM1	I/O	PWM1 PWM output / capture input pin
45	34		PA.12	I/O	Digital GPIO pin
			PWM0	I/O	PWM0 PWM output / capture input pin
46	35	23	ICE_DAT	I/O	Serial wired debugger data pin
47	36	24	ICE_CLK	I	Serial wired debugger clock input pin
48	37	25	AV <sub>DD</sub>	AP	Power supply for internal analog circuit
49	38		PD.0	I/O	Digital GPIO pin
			ADC0	AI	ADC channel 0 analog input pin
			SPI2_SS0	I/O	SPI2 1 <sup>st</sup> slave select pin
50	39	26	PD.1	I/O	Digital GPIO pin
			SPI2_CLK	I/O	SPI2 serial clock pin
			SPI0_SS1	I/O	SPI0 2 <sup>nd</sup> slave select pin
			ADC1	AI	ADC channel 1 analog input pin
51	40	27	PD.2	I/O	Digital GPIO pin
			SPI2_MISO0	I/O	SPI2 1 <sup>st</sup> MISO (Master In, Slave Out) pin
			SPI0_MISO1	I/O	SPI0 2 <sup>nd</sup> MISO (Master In, Slave Out) pin
			ADC2	AI	ADC channel 2 analog input pin
52	41	28	PD.3	I/O	Digital GPIO pin
			SPI2_MOSI0	I/O	SPI2 1 <sup>st</sup> MOSI (Master Out, Slave In) pin
			SPI0_MOSI1	I/O	SPI0 2 <sup>nd</sup> MOSI (Master Out, Slave In) pin
			ADC3	AI	ADC channel 3 analog input pin
53	42		PD.4	I/O	Digital GPIO pin
			ADC4	AI	ADC channel 4 analog input pin
			SPI2_MISO1	I/O	SPI2 2 <sup>nd</sup> MISO (Master In, Slave Out) pin
54	43		PD.5	I/O	Digital GPIO pin
			ADC5	AI	ADC channel 5 analog input pin
			SPI2_MOSI1	I/O	SPI2 2 <sup>nd</sup> MOSI (Master Out, Slave In) pin
55			PB.15	I/O	Digital GPIO pin
			INT1	I	External interrupt 1 input pin
			TM0_EXT	I	Timer0 external capture input pin
56	44	29	PF.0	I/O	Digital GPIO pin