



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





ARM Cortex™-M0
32-BIT MICROCONTROLLER

NuMicro™ Family
NUC130 Data Sheet

The information described in this document is the exclusive intellectual property of Nuvoton Technology Corporation and shall not be reproduced without permission from Nuvoton.

Nuvoton is providing this document only for reference purposes of NuMicro microcontroller based system design. Nuvoton assumes no responsibility for errors or omissions.

All data and specifications are subject to change without notice.

For additional information or questions, please contact: Nuvoton Technology Corporation.

Contents

1	GENERAL DESCRIPTION	7
2	FEATURES	8
2.1	NuMicro™ NUC130 Features – Automotive Line.....	8
3	PARTS INFORMATION LIST AND PIN CONFIGURATION	12
3.1	NuMicro™ NUC130 Products Selection Guide.....	12
3.1.1	NuMicro™ NUC130 Automotive Line Selection Guide.....	12
3.2	Pin Configuration	13
3.2.1	NuMicro™ NUC130/NUC140 Pin Diagram	13
4	BLOCK DIAGRAM	16
4.1	NuMicro™NUC130 Block Diagram	16
4.1.1	NuMicro™ NUC130 Block Diagram	16
5	FUNCTIONAL DESCRIPTION.....	17
5.1	ARM® Cortex™-M0 Core	17
5.2	System Manager.....	19
5.2.1	Overview	19
5.2.2	System Reset	19
5.2.3	System Power Distribution	20
5.2.4	System Memory Map.....	21
5.2.5	System Timer (SysTick)	23
5.2.6	Nested Vectored Interrupt Controller (NVIC).....	24
5.3	Clock Controller	28
5.3.1	Overview	28
5.3.2	Clock Generator	30
5.3.3	System Clock and SysTick Clock.....	31
5.3.4	Peripherals Clock	32
5.3.5	Power Down Mode Clock	32
5.3.6	Frequency Divider Output.....	33
5.4	General Purpose I/O (GPIO)	34
5.4.1	Overview	34
5.4.2	Features	34
5.5	I ² C Serial Interface Controller (Master/Slave) (I ² C)	35
5.5.1	Overview	35
5.5.2	Features	36
5.6	PWM Generator and Capture Timer (PWM)	37
5.6.1	Overview	37
5.6.2	Features	38
5.7	Real Time Clock (RTC).....	39
5.7.1	Overview	39
5.7.2	Features	39
5.8	Serial Peripheral Interface (SPI).....	40

5.8.1	Overview	40
5.8.2	Features	40
5.9	Timer Controller (TMR).....	41
5.9.1	Overview	41
5.9.2	Features	41
5.10	Watchdog Timer (WDT).....	42
5.10.1	Overview	42
5.10.2	Features	44
5.11	UART Interface Controller (UART).....	45
5.11.1	Overview	45
5.11.2	Features	47
5.12	Controller Area Network (CAN)	48
5.12.1	Overview	48
5.12.2	Features	48
5.13	PS/2 Device Controller (PS2D).....	49
5.13.1	Overview	49
5.13.2	Features	49
5.14	I ² S Controller (I ² S).....	50
5.14.1	Overview	50
5.14.2	Features	50
5.15	Analog-to-Digital Converter (ADC)	51
5.15.1	Overview	51
5.15.2	Features	51
5.16	Analog Comparator (CMP)	52
5.16.1	Overview	52
5.16.2	Features	52
5.17	PDMA Controller (PDMA).....	53
5.17.1	Overview	53
5.17.2	Features	53
5.18	External Bus Interface (EBI)	54
5.18.1	Overview	54
5.18.2	Features	54
6	FLASH MEMORY CONTROLLER (FMC)	55
6.1	Overview	55
6.2	Features	55
7	ELECTRICAL CHARACTERISTICS.....	56
7.1	Absolute Maximum Ratings	56
7.2	DC Electrical Characteristics	57
7.2.1	NuMicro™ NUC130/NUC140 DC Electrical Characteristics.....	57
7.3	AC Electrical Characteristics	62
7.3.1	External 4~24 MHz High Speed Oscillator	62
7.3.2	External 4~24 MHz High Speed Crystal	62

7.3.3	External 32.768 kHz Low Speed Crystal	63
7.3.4	Internal 22.1184 MHz High Speed Oscillator.....	63
7.3.5	Internal 10 kHz Low Speed Oscillator.....	63
7.4	Analog Characteristics	64
7.4.1	Specification of 12-bit SARADC	64
7.4.2	Specification of LDO and Power management.....	65
7.4.3	Specification of Low Voltage Reset	66
7.4.4	Specification of Brown-Out Detector.....	66
7.4.5	Specification of Power-On Reset (5 V).....	66
7.4.6	Specification of Temperature Sensor	67
7.4.7	Specification of Comparator	67
7.5	Flash DC Electrical Characteristics	68
7.6	SPI Dynamic Characteristics	69
8	PACKAGE DIMENSIONS	71
8.1	100L LQFP (14x14x1.4 mm footprint 2.0mm)	71
8.2	64L LQFP (10x10x1.4mm footprint 2.0 mm)	72
8.3	48L LQFP (7x7x1.4mm footprint 2.0mm)	73
9	REVISION HISTORY	74

Figures

Figure 3-1 NuMicro™ NUC100 Series selection code	12
Figure 3-2 NuMicro™ NUC130 LQFP 100-pin Pin Diagram	13
Figure 3-3 NuMicro™ NUC130 LQFP 64-pin Pin Diagram	14
Figure 3-4 NuMicro™ NUC130 LQFP 48-pin Pin Diagram	15
Figure 4-1 NuMicro™ NUC130 Block Diagram	16
Figure 5-1 Functional Controller Diagram	17
Figure 5-3 NuMicro™ NUC130 Power Distribution Diagram	20
Figure 5-4 Clock generator global view diagram	29
Figure 5-5 Clock generator block diagram	30
Figure 5-6 System Clock Block Diagram	31
Figure 5-7 SysTick Clock Control Block Diagram	31
Figure 5-8 Clock Source of Frequency Divider	33
Figure 5-9 Block Diagram of Frequency Divider	33
Figure 5-10 I ² C Bus Timing	35
Figure 5-11 Timing of Interrupt and Reset Signal	43
Figure 7-1 Typical Crystal Application Circuit	63
Figure 7-2 SPI Master dynamic characteristics tiMING	70
Figure 7-3 SPI Slave dynamic characteristics timing	70

Tables

Table 1-1 Connectivity Supported Table.....	7
Table 5-1 Address Space Assignments for On-Chip Controllers.....	22
Table 5-2 Exception Model	25
Table 5-3 System Interrupt Map.....	26
Table 5-4 Vector Table Format	27
Table 5-5 Watchdog Timeout Interval Selection	43
Table 5-6 UART Baud Rate Equation.....	45
Table 5-7 UART Baud Rate Setting Table.....	46

1 GENERAL DESCRIPTION

The NuMicro™ NUC100 Series is 32-bit microcontrollers with embedded ARM® Cortex™-M0 core for industrial control and applications which need rich communication interfaces. The Cortex™-M0 is the newest ARM® embedded processor with 32-bit performance and at a cost equivalent to traditional 8-bit microcontroller. NuMicro™ NUC100 Series includes NUC100, NUC120, NUC130 and NUC140 product line.

The NuMicro™ NUC130 Automotive Line with CAN function embeds Cortex™-M0 core running up to 50 MHz with 32K/64K/128K-byte embedded flash, 4K/8K/16K-byte embedded SRAM, and 4K-byte loader ROM for the ISP. It also equips with plenty of peripheral devices, such as Timers, Watchdog Timer, RTC, PDMA, UART, SPI, I²C, I²S, PWM Timer, GPIO, LIN, CAN, PS/2, 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-out Detector.

Product Line	UART	SPI	I ² C	USB	LIN	CAN	PS/2	I ² S
NUC100	•	•	•				•	•
NUC120	•	•	•	•			•	•
NUC130	•	•	•		•	•	•	•
NUC140	•	•	•	•	•	•	•	•

Table 1-1 Connectivity Supported Table

2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 NuMicro™ NUC130 Features – Automotive Line

- Core
 - ARM® Cortex™-M0 core runs up to 50 MHz
 - One 24-bit system timer
 - Supports low power sleep mode
 - Single-cycle 32-bit hardware multiplier
 - NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Build-in LDO for wide operating voltage ranges from 2.5 V to 5.5 V
- Flash Memory
 - 32K/64K/128K bytes Flash for program code
 - 4KB flash for ISP loader
 - Support In-system program (ISP) application code update
 - 512 byte page erase for flash
 - Configurable data flash address and size for 128KB system, fixed 4KB data flash for the 32KB and 64KB system
 - Support 2 wire ICP update through SWD/ICE interface
 - Support fast parallel programming mode by external programmer
- SRAM Memory
 - 4K/8K/16K bytes embedded SRAM
 - Support PDMA mode
- PDMA (Peripheral DMA)
 - Support 9 channels PDMA for automatic data transfer between SRAM and peripherals
- Clock Control
 - Flexible selection for different applications
 - Built-in 22.1184 MHz high speed OSC for system operation
 - ◆ Trimmed to $\pm 1\%$ at $+25\text{ }^\circ\text{C}$ and $V_{DD} = 5\text{ V}$
 - ◆ Trimmed to $\pm 3\%$ at $-40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$ and $V_{DD} = 2.5\text{ V} \sim 5.5\text{ V}$
 - Built-in 10 kHz low speed OSC for Watchdog Timer and Wake-up operation
 - Support one PLL, up to 50 MHz, for high performance system operation
 - External 4~24 MHz high speed crystal input for precise timing operation
 - External 32.768 kHz low speed crystal input for RTC function and low power system operation
- GPIO
 - Four I/O modes:
 - ◆ Quasi bi-direction
 - ◆ Push-Pull output
 - ◆ Open-Drain output
 - ◆ Input only with high impedance
 - TTL/Schmitt trigger input selectable
 - I/O pin can be configured as interrupt source with edge/level setting
 - High driver and high sink IO mode support

- Timer
 - Support 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
 - Independent clock source for each timer
 - Provides one-shot, periodic, toggle and continuous counting operation modes
 - Support event counting function
 - Support input capture function
- Watchdog Timer
 - Multiple clock sources
 - 8 selectable time out period from 1.6ms ~ 26.0sec (depends on clock source)
 - WDT can wake-up from power down or idle mode
 - Interrupt or reset selectable on watchdog time-out
- RTC
 - Support software compensation by setting frequency compensate register (FCR)
 - Support RTC counter (second, minute, hour) and calendar counter (day, month, year)
 - Support Alarm registers (second, minute, hour, day, month, year)
 - Selectable 12-hour or 24-hour mode
 - Automatic leap year recognition
 - Support periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
 - Support wake-up function
- PWM/Capture
 - Built-in up to four 16-bit PWM generators provide eight PWM outputs or four complementary paired PWM outputs
 - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
 - Up to eight 16-bit digital Capture timers (shared with PWM timers) provide eight rising/falling capture inputs
 - Support Capture interrupt
- UART
 - Up to three UART controllers
 - UART ports with flow control (TXD, RXD, CTS and RTS)
 - UART0 with 64-byte FIFO is for high speed
 - UART1/2(optional) with 16-byte FIFO for standard device
 - Support IrDA (SIR) and LIN function
 - Support RS-485 9-bit mode and direction control.
 - Programmable baud-rate generator up to 1/16 system clock
 - Support PDMA mode
- SPI
 - Up to four sets of SPI controller
 - Master up to 32 MHz, and Slave up to 10 MHz (chip working @ 5V)
 - Support SPI master/slave mode
 - Full duplex synchronous serial data transfer
 - Variable length of transfer data from 1 to 32 bits
 - MSB or LSB first data transfer
 - Rx and Tx on both rising or falling edge of serial clock independently
 - 2 slave/device select lines when it is as the master, and 1 slave/device select line when it is as the slave
 - Support byte suspend mode in 32-bit transmission
 - Support PDMA mode
 - Support three wire, no slave select signal, bi-direction interface

- I²C
 - Up to two sets of I²C device
 - Master/Slave mode
 - Bidirectional data transfer between masters and slaves
 - Multi-master bus (no central master)
 - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
 - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
 - Programmable clocks allow versatile rate control
 - Support multiple address recognition (four slave address with mask option)
- I²S
 - Interface with external audio CODEC
 - Operate as either master or slave mode
 - Capable of handling 8-, 16-, 24- and 32-bit word sizes
 - Mono and stereo audio data supported
 - I²S and MSB justified data format supported
 - Two 8 word FIFO data buffers are provided, one for transmit and one for receive
 - Generates interrupt requests when buffer levels cross a programmable boundary
 - Support two DMA requests, one for transmit and one for receive
- PS/2 Device Controller
 - Host communication inhibit and request to send detection
 - Reception frame error detection
 - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
 - Double buffer for data reception
 - S/W override bus
- CAN 2.0
 - Supports CAN protocol version 2.0 part A and B
 - Bit rates up to 1M bit/s
 - 32 Message Objects
 - Each Message Object has its own identifier mask
 - Programmable FIFO mode (concatenation of Message Object)
 - Maskable interrupt
 - Disabled Automatic Re-transmission mode for Time Triggered CAN applications
 - Support power down wake-up function
- EBI (External bus interface) support (100-pin and 64-pin Package Only)
 - Accessible space: 64KB in 8-bit mode or 128KB in 16-bit mode
 - Support 8-/16-bit data width
 - Support byte write in 16-bit data width mode
- ADC
 - 12-bit SAR ADC with 700K SPS
 - Up to 8-ch single-end input or 4-ch differential input
 - Single scan/single cycle scan/continuous scan
 - Each channel with individual result register
 - Scan on enabled channels
 - Threshold voltage detection
 - Conversion start by software programming or external input

- Support PDMA mode
- Analog Comparator
 - Up to two analog comparator
 - External input or internal bandgap voltage selectable at negative node
 - Interrupt when compare result change
 - Power down wake-up
- One built-in temperature sensor with 1°C resolution
- Brown-Out detector
 - With 4 levels: 4.5 V/3.8 V/2.7 V/2.2 V
 - Support Brown-Out Interrupt and Reset option
- Low Voltage Reset
 - Threshold voltage levels: 2.0 V
- Operating Temperature: -40°C~85°C
- Packages:
 - All Green package (RoHS)
 - LQFP 100-pin / 64-pin / 48-pin

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ NUC130 Products Selection Guide

3.1.1 NuMicro™ NUC130 Automotive Line Selection Guide

Part number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity					i ² S	Comp.	PWM	ADC	RTC	EBI	ISP ICP	Package	
							UART	SPI	I ² C	USB	LIN									CAN
NUC130LC1CN	32 KB	4 KB	4 KB	4 KB	up to 35	4x32-bit	3	1	2	-	2	1	1	1	4	8x12-bit	v	-	v	LQFP48
NUC130LD2CN	64 KB	8 KB	4 KB	4 KB	up to 35	4x32-bit	3	1	2	-	2	1	1	1	4	8x12-bit	v	-	v	LQFP48
NUC130LE3CN	128 KB	16 KB	Definable	4 KB	up to 35	4x32-bit	3	1	2	-	2	1	1	1	4	8x12-bit	v	-	v	LQFP48
NUC130RC1CN	32 KB	4 KB	4 KB	4 KB	up to 49	4x32-bit	3	2	2	-	2	1	1	2	6	8x12-bit	v	v	v	LQFP64
NUC130RD2CN	64 KB	8 KB	4 KB	4 KB	up to 49	4x32-bit	3	2	2	-	2	1	1	2	6	8x12-bit	v	v	v	LQFP64
NUC130RD3CN	128 KB	16 KB	Definable	4 KB	up to 49	4x32-bit	3	2	2	-	2	1	1	2	6	8x12-bit	v	v	v	LQFP64
NUC130VE3CN	128 KB	16 KB	Definable	4 KB	up to 80	4x32-bit	3	4	2	-	2	1	1	2	8	8x12-bit	v	v	v	LQFP100

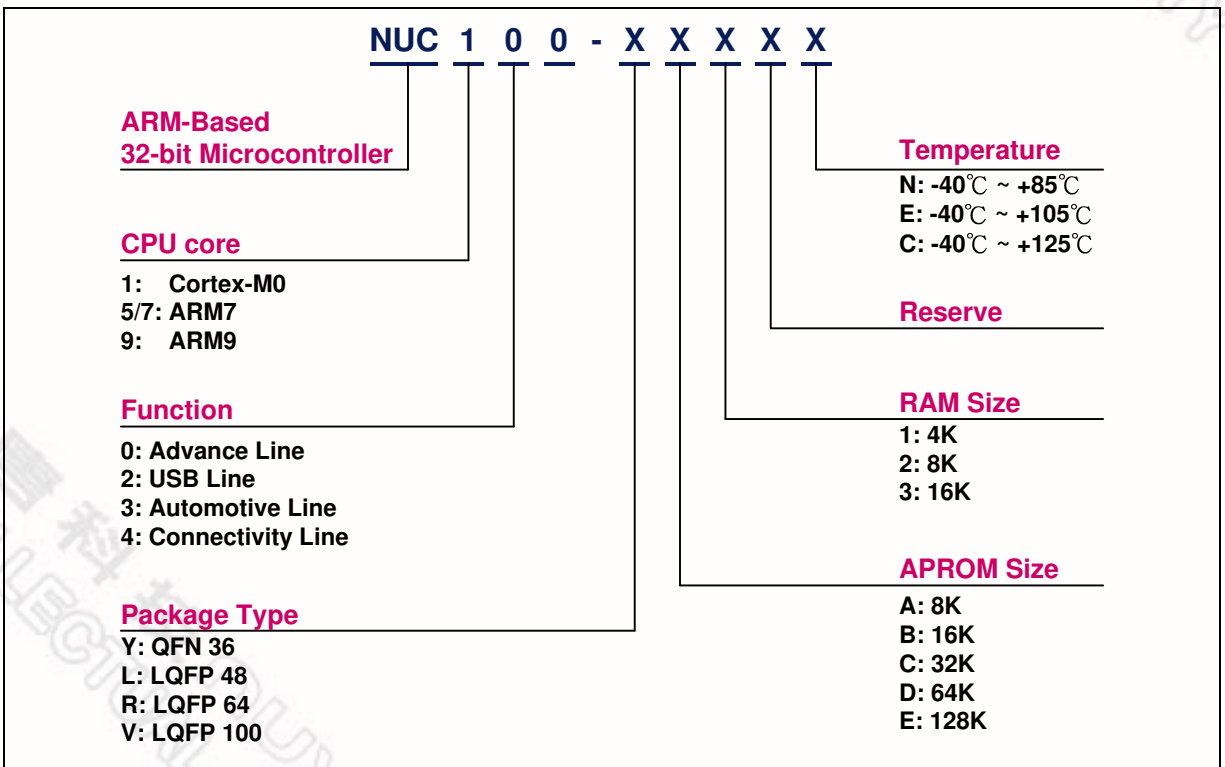


Figure 3-1 NuMicro™ NUC100 Series selection code

3.2 Pin Configuration

3.2.1 NuMicro™ NUC130/NUC140 Pin Diagram

3.2.1.1 NuMicro™ NUC130 LQFP 100 pin

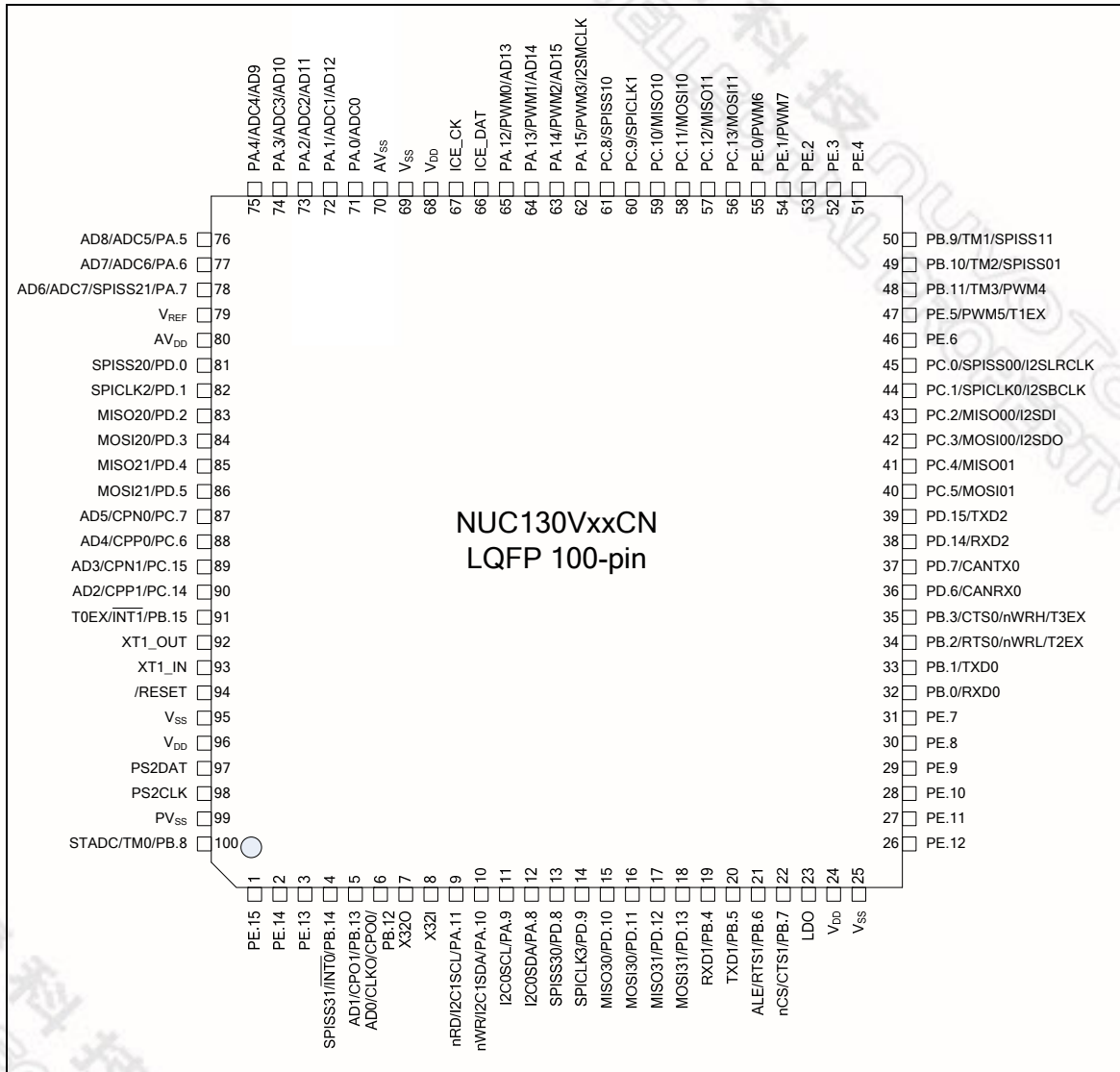


Figure 3-2 NuMicro™ NUC130 LQFP 100-pin Pin Diagram



3.2.1.2 NuMicro™ NUC130 LQFP 64 pin

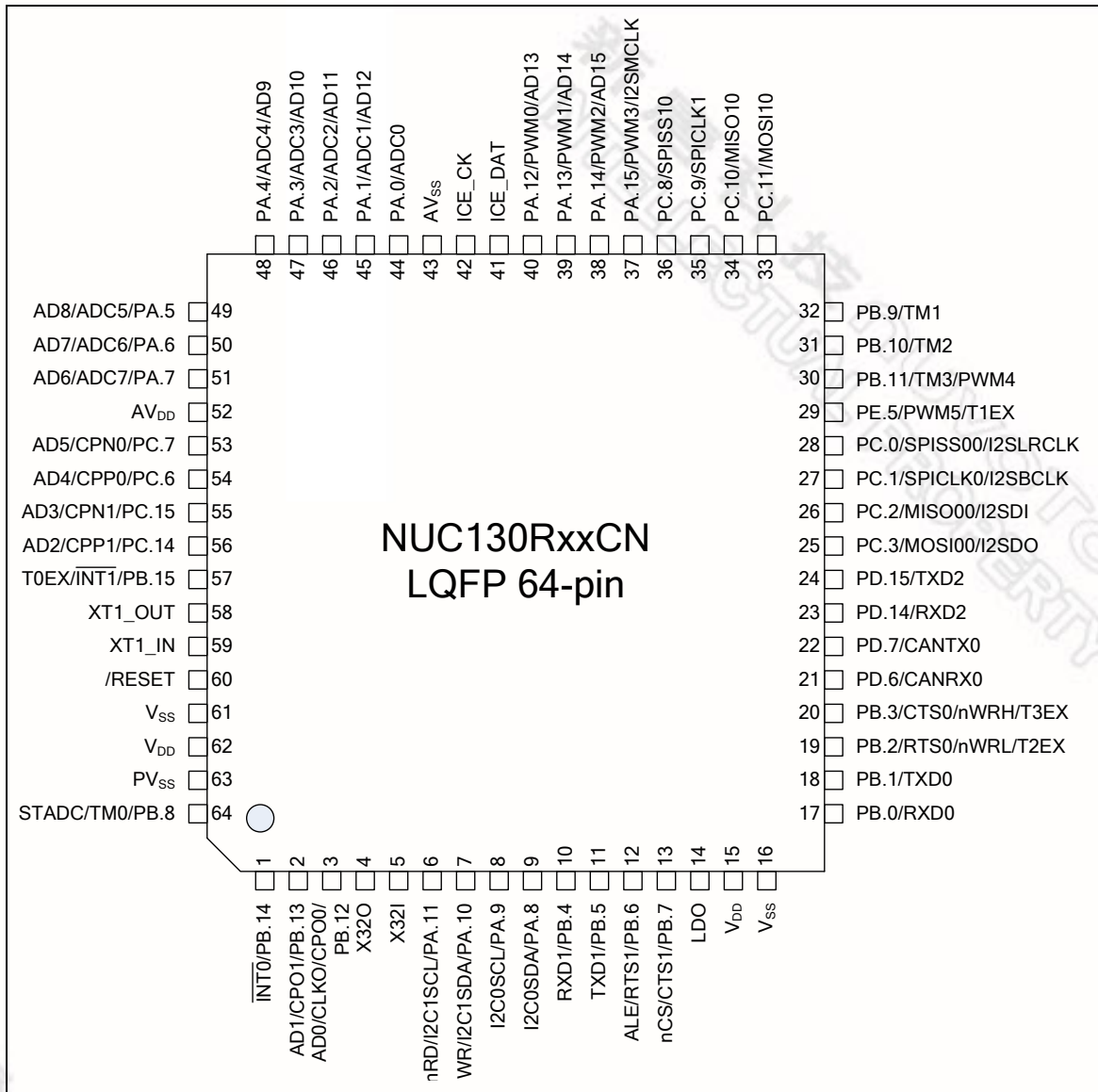


Figure 3-3 NuMicro™ NUC130 LQFP 64-pin Pin Diagram

3.2.1.3 NuMicro™ NUC130 LQFP 48 pin

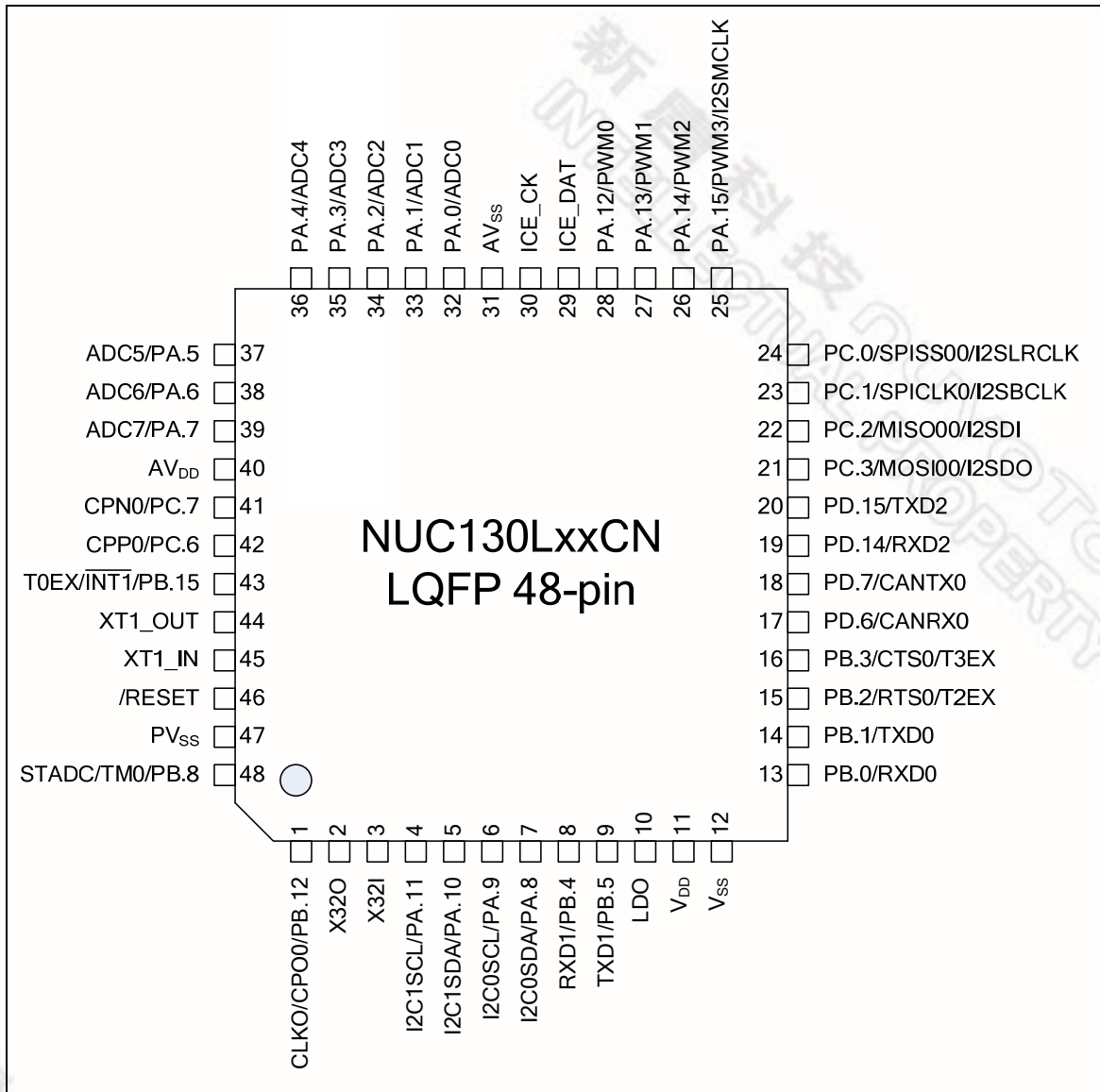


Figure 3-4 NuMicro™ NUC130 LQFP 48-pin Pin Diagram

4 BLOCK DIAGRAM

4.1 NuMicro™ NUC130 Block Diagram

4.1.1 NuMicro™ NUC130 Block Diagram

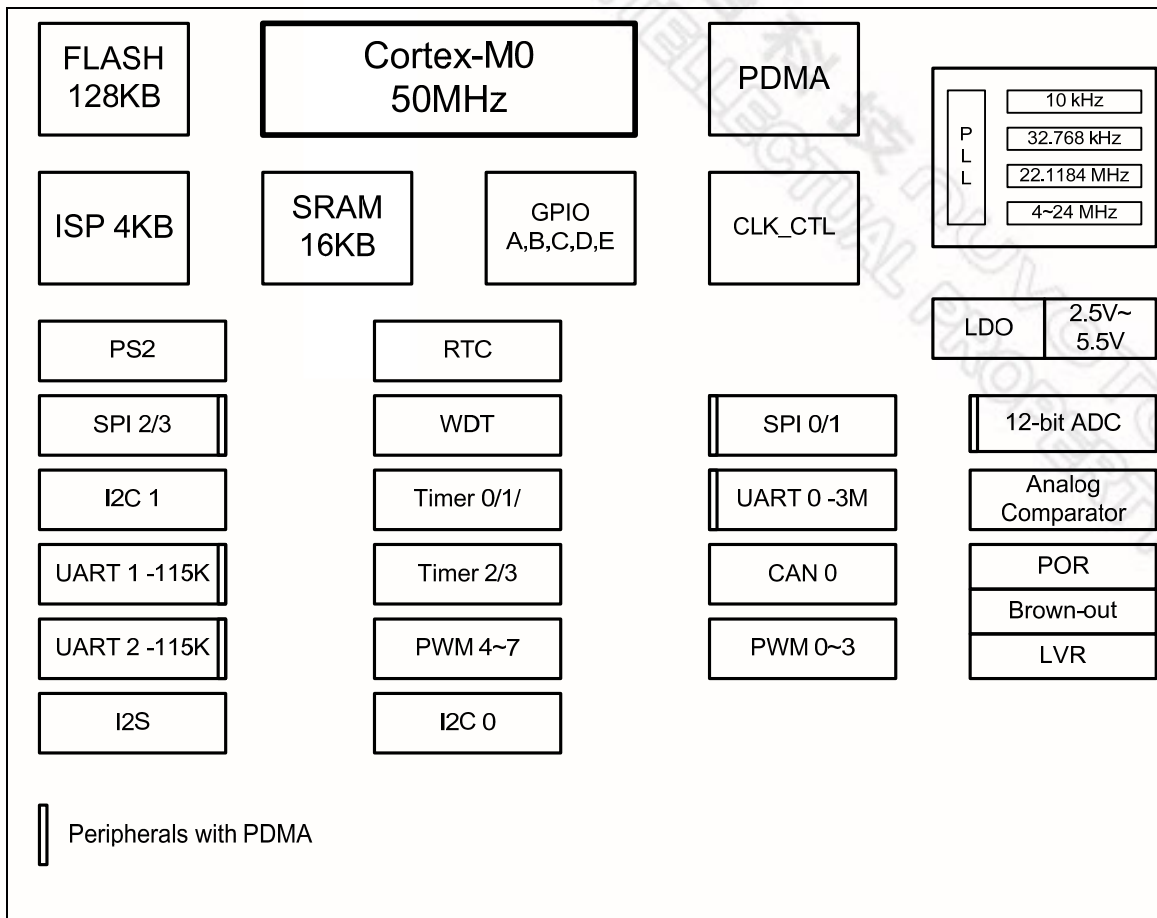


Figure 4-1 NuMicro™ NUC130 Block Diagram

5 FUNCTIONAL DESCRIPTION

5.1 ARM® Cortex™-M0 Core

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 5-1 shows the functional controller of processor.

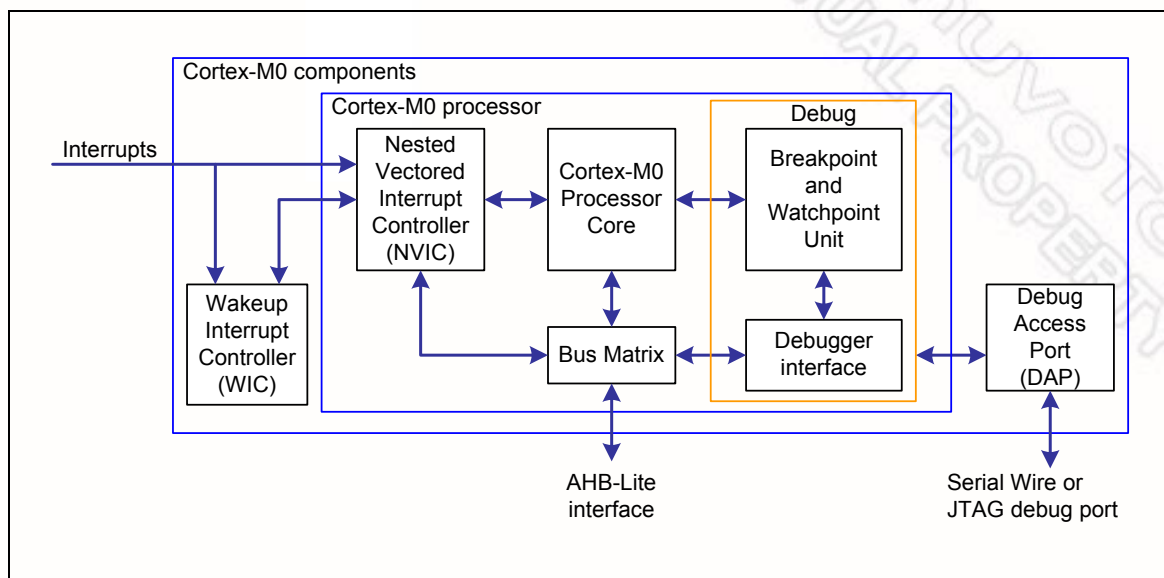


Figure 5-1 Functional Controller Diagram

The implemented device provides:

- A low gate count processor that features:
 - ◆ The ARMv6-M Thumb® instruction set
 - ◆ Thumb-2 technology
 - ◆ ARMv6-M compliant 24-bit SysTick timer
 - ◆ A 32-bit hardware multiplier
 - ◆ The system interface supports little-endian data accesses
 - ◆ The ability to have deterministic, fixed-latency, interrupt handling
 - ◆ Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
 - ◆ C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers

- ◆ Low power sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC that features:
 - ◆ 32 external interrupt inputs, each with four levels of priority
 - ◆ Dedicated Non-Maskable Interrupt (NMI) input.
 - ◆ Support for both level-sensitive and pulse-sensitive interrupt lines
 - ◆ Wake-up Interrupt Controller (WIC), providing ultra-low power sleep mode support.
- Debug support
 - ◆ Four hardware breakpoints.
 - ◆ Two watchpoints.
 - ◆ Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
 - ◆ Single step and vector catch capabilities.
- Bus interfaces:
 - ◆ Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
 - ◆ Single 32-bit slave port that supports the DAP (Debug Access Port).

5.2 System Manager

5.2.1 Overview

System management includes these following sections:

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

5.2.2 System Reset

The system reset can be issued by one of the below listed events. For these reset event flags can be read by RSTSRC register.

- The Power-On Reset
- The low level on the /RESET pin
- Watchdog Time Out Reset
- Low Voltage Reset
- Brown-Out Detector Reset
- CPU Reset
- System Reset

System Reset and Power-On Reset all reset the whole chip including all peripherals. The difference between System Reset and Power-On Reset is external crystal circuit and ISPCON.BS bit. System Reset doesn't reset external crystal circuit and ISPCON.BS bit, but Power-On Reset does.

5.2.3 System Power Distribution

In this chip, the power distribution is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 2.5 V power for digital operation and I/O pins.

The outputs of internal voltage regulators, LDO and V_{DD33} , require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 5-2 shows the power distribution of NuMicro™ NUC130.

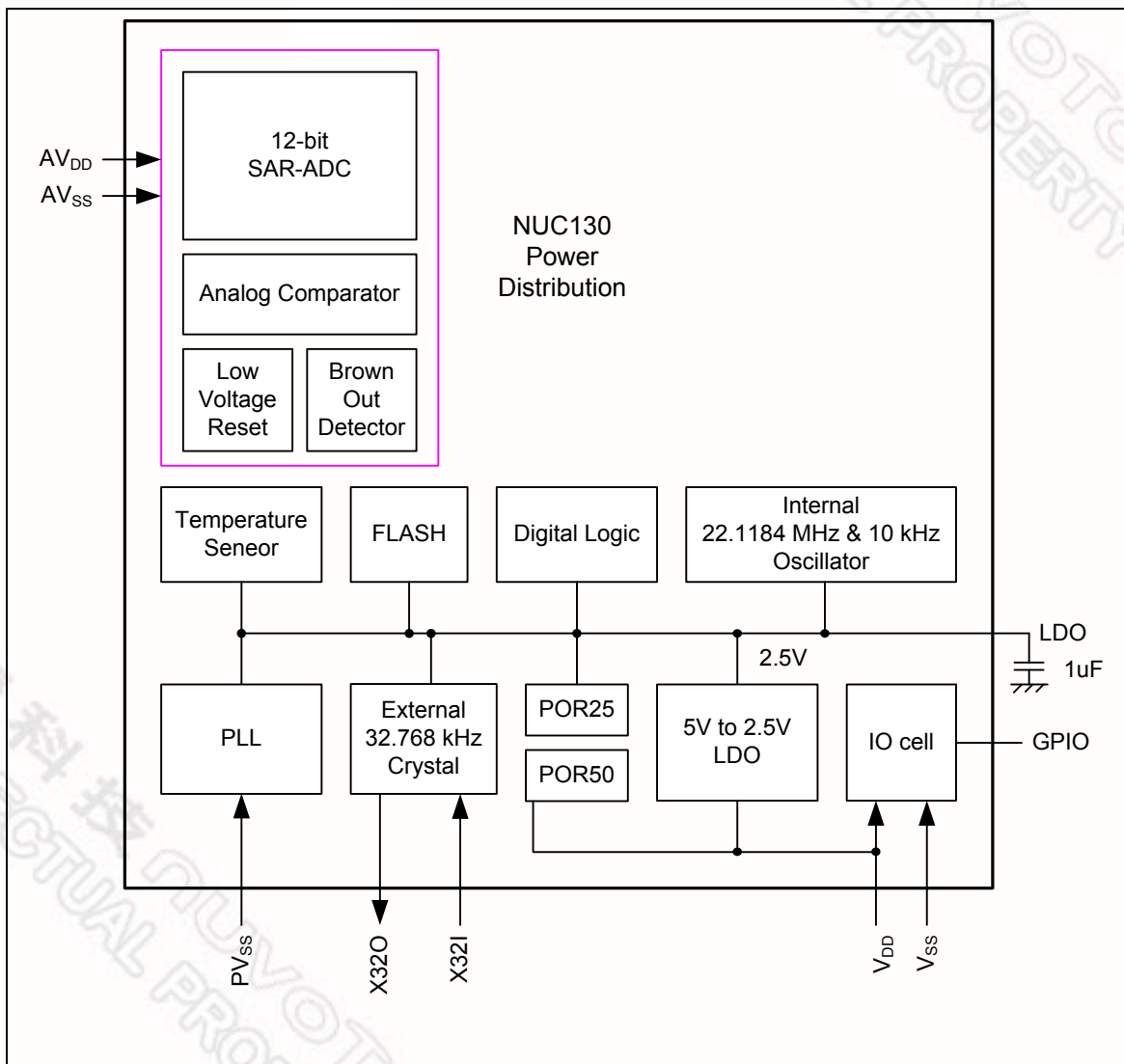


Figure 5-2 NuMicro™ NUC130 Power Distribution Diagram

5.2.4 System Memory Map

NuMicro™ NUC100 Series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in the following table. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip peripherals. NuMicro™ NUC100 Series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	FLASH Memory Space (128KB)
0x2000_0000 – 0x2000_3FFF	SRAM_BA	SRAM Memory Space (16KB)
0x6000_0000 – 0x6001_FFFF	EXTMEM_BA	External Memory Space (128KB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	PDMA_BA	Peripheral DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_03FF	EBI_BA	External Bus Interface Control Registers
APB1 Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4000_8000 – 0x4000_BFFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I ² C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWMA_BA	PWM0/1/2/3 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4006_0000 – 0x4006_3FFF	USBD_BA	USB 2.0 FS device Controller Registers

Address Space	Token	Controllers
0x400D_0000 – 0x400D_3FFF	ACMP_BA	Analog Comparator Control Registers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
APB2 Controllers Space (0x4010_0000 ~ 0x401F_FFFF)		
0x4010_0000 – 0x4010_3FFF	PS2_BA	PS/2 Interface Control Registers
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I ² C1 Interface Control Registers
0x4013_0000 – 0x4013_3FFF	SPI2_BA	SPI2 with master/slave function Control Registers
0x4013_4000 – 0x4013_7FFF	SPI3_BA	SPI3 with master/slave function Control Registers
0x4014_0000 – 0x4014_3FFF	PWMB_BA	PWM4/5/6/7 Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4015_4000 – 0x4015_7FFF	UART2_BA	UART2 Control Registers
0x4018_0000 – 0x4018_3FFF	CAN0_BA	CAN0 Bus Control Registers
0x401A_0000 – 0x401A_3FFF	I2S_BA	I ² S Interface Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 5-1 Address Space Assignments for On-Chip Controllers

5.2.5 System Timer (SysTick)

The Cortex-M0 includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the documents “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

5.2.6 Nested Vectored Interrupt Controller (NVIC)

Cortex-M0 provides an interrupt controller as an integral part of the exception mode, named as “Nested Vectored Interrupt Controller (NVIC)”. It is closely coupled to the processor kernel and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in “Handler Mode”. This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one’s priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When any interrupts is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers “PC, PSR, LR, R0~R3, R12” to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports “Tail Chaining” which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports “Late Arrival” which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the documents “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.



5.2.6.1 Exception Model and System Interrupt Map

Table 5-2 lists the exception model supported by NuMicro™ NUC100 Series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0” and the lowest priority is denoted as “3”. The default priority of all the user-configurable interrupts is “0”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCAll	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 5-2 Exception Model

Vector Number	Interrupt Number (Bit in Interrupt Registers)	Interrupt Name	Source IP	Interrupt description
0 ~ 15	-	-	-	System exceptions
16	0	BOD_OUT	Brown-Out	Brown-Out low voltage detected interrupt
17	1	WDT_INT	WDT	Watchdog Timer interrupt
18	2	EINT0	GPIO	External signal interrupt from PB.14 pin
19	3	EINT1	GPIO	External signal interrupt from PB.15 pin
20	4	GPAB_INT	GPIO	External signal interrupt from PA[15:0]/PB[13:0]
21	5	GPCDE_INT	GPIO	External interrupt from PC[15:0]/PD[15:0]/PE[15:0]
22	6	PWMA_INT	PWM0~3	PWM0, PWM1, PWM2 and PWM3 interrupt
23	7	PWMB_INT	PWM4~7	PWM4, PWM5, PWM6 and PWM7 interrupt
24	8	TMR0_INT	TMR0	Timer 0 interrupt
25	9	TMR1_INT	TMR1	Timer 1 interrupt