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NuMicro™ NUC131 Series Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The NuMicro™ NUC131 CAN Line is embedded with the Cortex™-M0 core running up to 50 MHz and features 36K/68K bytes flash, 8K bytes SRAM, and 4 Kbytes loader ROM for the ISP. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timer (WDT), Window Watchdog Timer (WWDT), UART, SPI, I^2C, PWM, GPIO, LIN, CAN, 800 kSPS high speed 12-bit ADC, Low Voltage Reset Controller and Brown-out Detector.

2 FEATURES

- ARM® Cortex™-M0 core
  - Runs up to 50 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5 V to 5.5 V
- Flash Memory
  - 36K/68K bytes Flash for program code
  - Configurable Flash memory for data memory (Data Flash), 4 KB flash for ISP loader
  - Supports In-System-Program (ISP) and In-Application-Program (IAP) application code update
  - 512 byte page erase for flash
  - Supports 2-wired ICP update through SWD/ICE interface
  - Supports fast parallel programming mode by external programmer
- SRAM Memory
  - 8KB embedded SRAM
- Clock Control
  - Flexible selection for different applications
  - Built-in 22.1184 MHz high speed oscillator for system operation
    - Trimmed to ±1 % at +25 ℃ and V_{DD} = 5 V
    - Trimmed to ±2 % at -40 ℃ ~ +105 ℃ and V_{DD} = 2.5 V ~ 5.5 V
  - Built-in 10 kHz low speed oscillator for Watchdog Timer and Wake-up operation
  - Supports one PLL output frequency up to 200 MHz, BPWM/PWM clock frequency up to 100 MHz, and System operation frequency up to 50 MHz
  - External 4~24 MHz high speed crystal input for precise timing operation
- GPIO
  - Four I/O modes:
    - Quasi-bidirectional
    - Push-pull output
    - Open-drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin configured as interrupt source with edge/level setting
- Timer
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
  - Independent clock source for each timer
  - Provides one-shot, periodic, toggle and continuous counting operation modes
  - Supports event counting function
  - Supports input capture function
- Watchdog Timer
  - Multiple clock sources
    - System clock (HCLK)
    - Internal 10 kHz oscillator (LIRC)
  - 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
  - Wake-up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
- Window Watchdog Timer
  - 6-bit down counter with 11-bit prescale for wide range window selected
- BPWM/Capture
  - Supports maximum clock frequency up to 100MHz
  - Supports up to two BPWM modules, each module provides one 16-bit timer and 6 output

channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit pre-scalar from 1 to 4096
- Supports 16-bit resolution BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt on the following events:
  - BPWM counter match zero, period value or compared value
- Supports trigger ADC on the following events:
  - BPWM counter match zero, period value or compared value
- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising edges, falling edges or both edges capture condition
- Supports input rising edges, falling edges or both edges capture interrupt
- Supports rising edges, falling edges or both edges capture with counter reload option

- PWM/Capture
  - Supports maximum clock frequency up to 100MHz
  - Supports up to two PWM modules, each module provides three 16-bit timers and 6 output channels
  - Supports independent mode for PWM output/Capture input channel
  - Supports complementary mode for 3 complementary paired PWM output channel
    - Dead-time insertion with 12-bit resolution
    - Two compared values during one period
  - Supports 12-bit pre-scalar from 1 to 4096
  - Supports 16-bit resolution PWM counter
    - Up, down and up/down counter operation type
  - Supports mask function and tri-state enable for each PWM pin
  - Supports brake function
    - Brake source from pin and system safety events (clock failed, Brown-out detection and CPU lockup)
    - Noise filter for brake source from pin
    - Edge detect brake source to control brake state until brake interrupt cleared
    - Level detect brake source to auto recover function after brake condition removed
  - Supports interrupt on the following events:
    - PWM counter match zero, period value or compared value
    - Brake condition happened
  - Supports trigger ADC on the following events:
    - PWM counter match zero, period value or compared value
  - Supports up to 12 capture input channels with 16-bit resolution
  - Supports rising edges, falling edges or both edges capture condition
  - Supports input rising edges, falling edges or both edges capture interrupt
  - Supports rising edges, falling edges or both edges capture with counter reload option
- UART
  - Up to six UART controllers
  - UART0 and UART1 ports with flow control (TXD, RXD, nCTS and nRTS)
  - UART0, UART1 and UART2 with 16-byte FIFO for standard device
  - Supports IrDA (SIR) and LIN function
  - Supports RS-485 9-bit mode and direction control
  - Supports auto baud-rate generator
- SPI
  - One set of SPI controller
  - Supports SPI Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently

- Supports Byte Suspend mode in 32-bit transmission
- Supports three wire, no slave select signal, bi-direction interface

- I^2C
  - Up to two sets of I^2C devices
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allowing for versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports wake-up function
- CAN 2.0
  - One set of CAN device
  - Supports CAN protocol version 2.0 part A and B
  - Bit rates up to 1M bit/s
  - 32 Message Objects
  - Each Message Object has its own identifier mask
  - Programmable FIFO mode (concatenation of Message Object)
  - Maskable interrupt
  - Disabled Automatic Re-transmission mode for Time Triggered CAN applications
  - Support power-down wake-up function
- ADC
  - 12-bit SAR ADC with 800 kSPS
  - Up to 8-ch single-end input or 4-ch differential input
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion started by software programming or external input
- 96-bit unique ID (UID)
- 128-bit unique customer ID(UCID)
- Brown-out Detector
  - With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage level: 2.0 V
- Operating Temperature: -40℃ ~ +105℃
- Packages:
  - All Green package (RoHS)
  - LQFP 64-pin / 48-pin (7mm x 7mm)

3 ABBREVIATIONS

Acronym	Description
ADC	Analog-to-Digital Converter
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
BPWM	Basic Pulse Width Modulation
CAN	Controller Area Network
DAP	Debug Access Port
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro™ MUC131 Series Selection Code

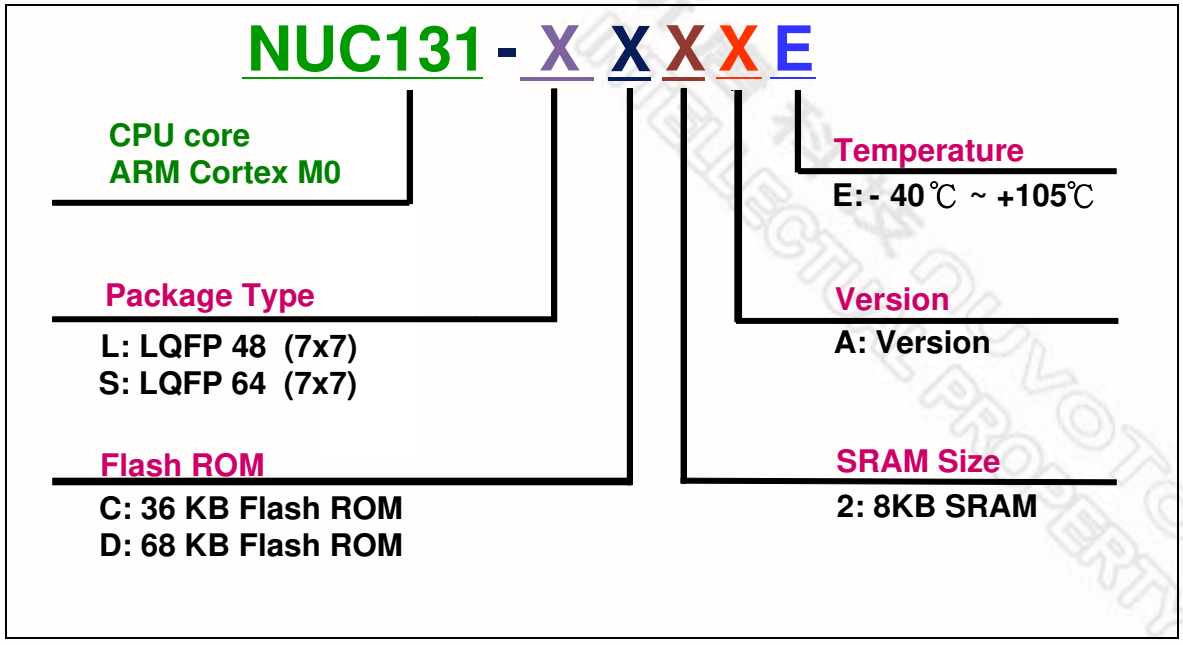

Figure 4-1 NuMicro™ NUC131 Series Selection Code

4.2 NuMicro™ NUC131 Series Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-Bit)	Connectivity					PWM (16-Bit)	ADC (12-Bit)	ISP/ICP/IAP	Package
							UART	SPI	I^2C	LIN	CAN				
NUC131LC2AE	36	8	Configurable	4	42	4	6	1	2	3	1	24	8 ch	√	LQFP48
NUC131LD2AE	68	8	Configurable	4	42	4	6	1	2	3	1	24	8 ch	√	LQFP48
NUC131SC2AE	36	8	Configurable	4	56	4	6	1	2	3	1	24	8 ch	√	LQFP64
NUC131SD2AE	68	8	Configurable	4	56	4	6	1	2	3	1	24	8 ch	√	LQFP64

4.3 Pin Configuration

4.3.1 NuMicro™ NUC131 Pin Diagram

*4.3.1.1 NuMicro™ NUC131SxxAE LQFP 64 pin (7 mm * 7mm)*

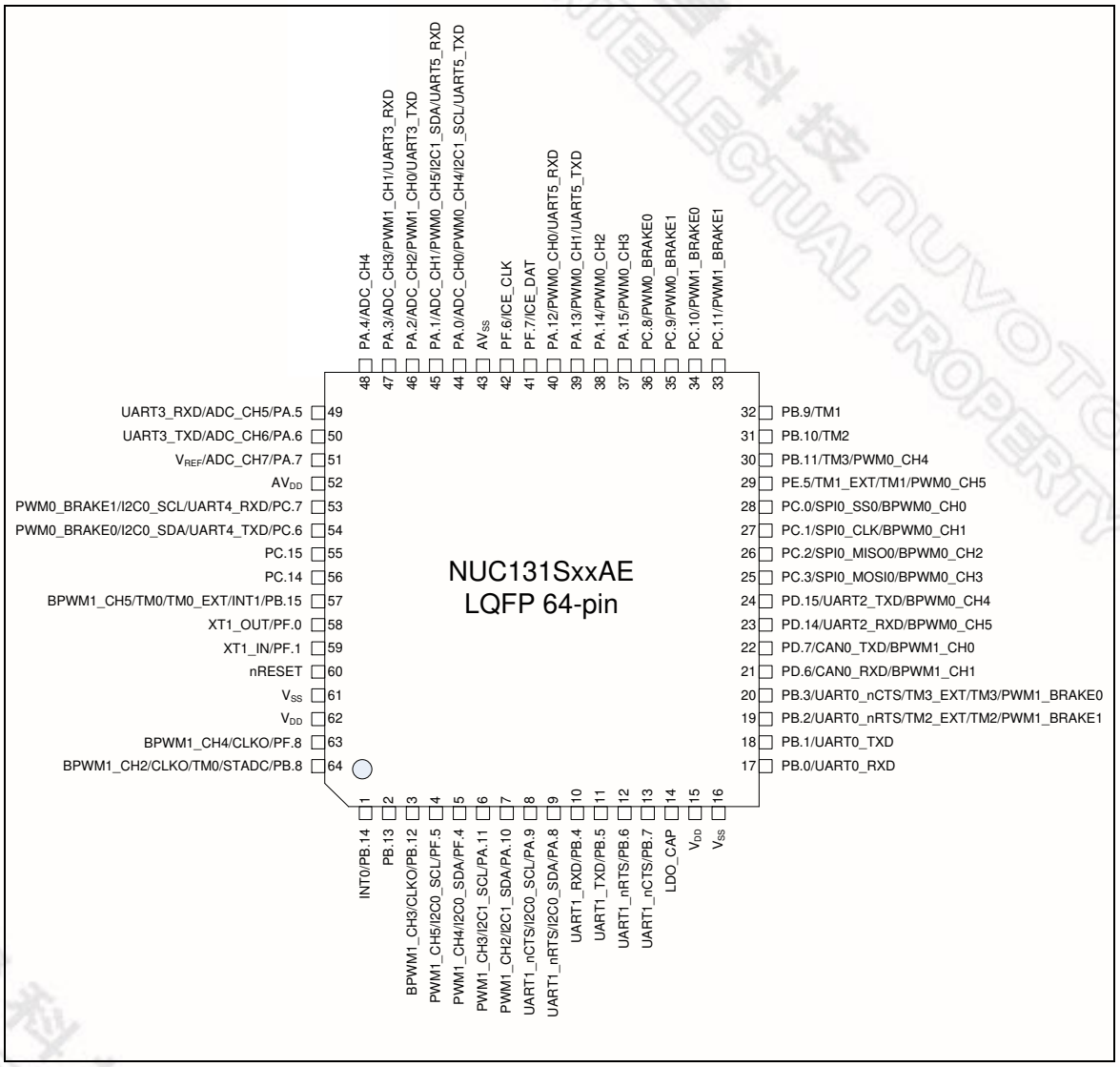

Figure 4-2 NuMicro™ NUC131SxxAE LQFP 64-pin Diagram

4.3.1.2 NuMicro™ NUC131LxxAE LQFP 48 pin

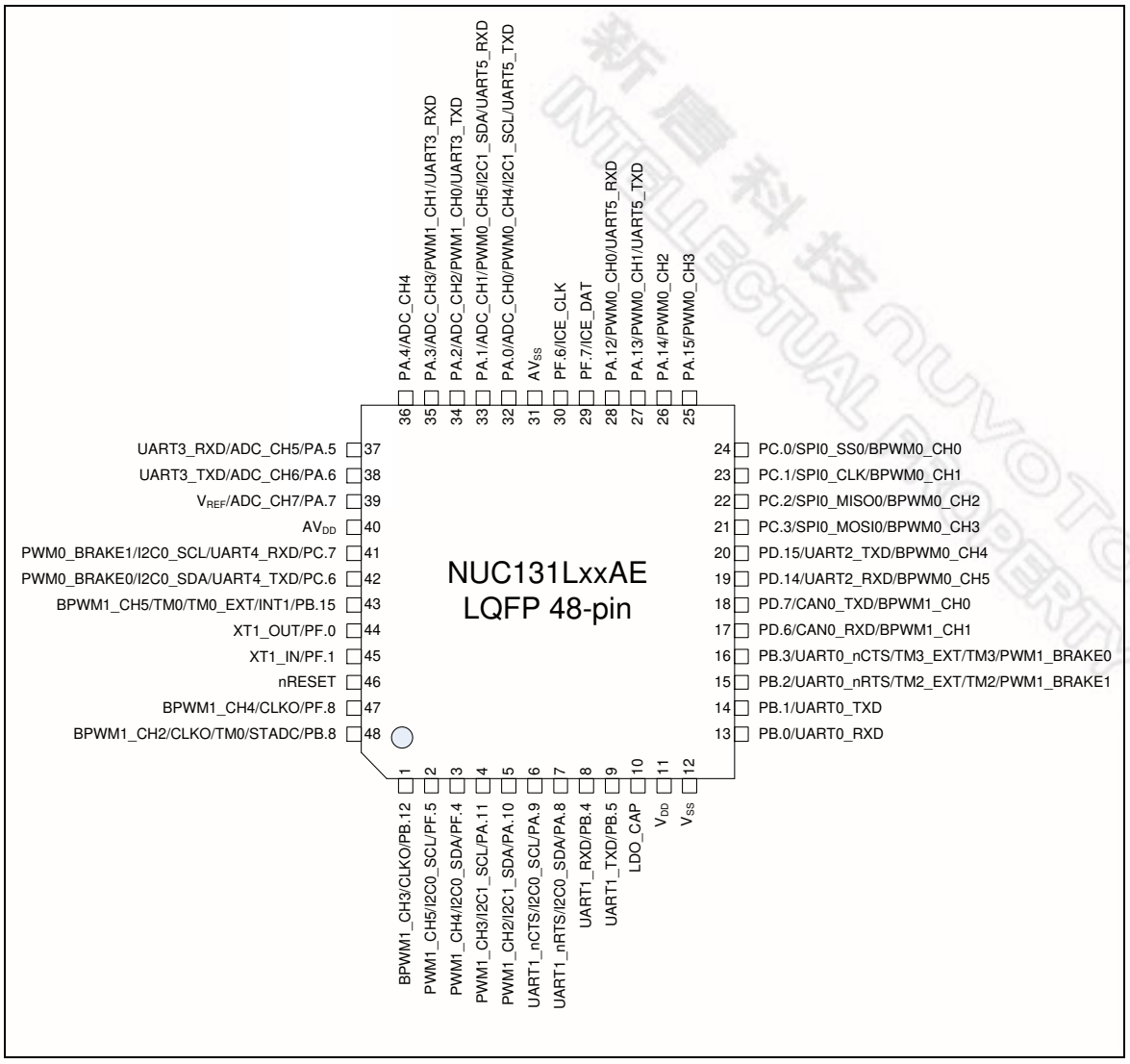

Figure 4-3 NuMicro™ NUC131LxxAE LQFP 48-pin Diagram

4.4 Pin Description

4.4.1 NuMicro™ NUC131 Pin Description

Pin No.		Pin Name	Pin Type	Description
LQFP 64-pin	LQFP 48-pin			
1		PB.14	I/O	General purpose digital I/O pin.
		INT0	I	External interrupt0 input pin.
2		PB.13	I/O	General purpose digital I/O pin.
3	1	PB.12	I/O	General purpose digital I/O pin.
		CLKO	O	Frequency divider clock output pin.
		BPWM1_CH3	I/O	BPWM1 CH3 output/Capture input.
4	2	PF.5	I/O	General purpose digital I/O pin.
		I2C0_SCL	I/O	I^2C0 clock pin.
		PWM1_CH5	I/O	PWM1 CH5 output/Capture input.
5	3	PF.4	I/O	General purpose digital I/O pin.
		I2C0_SDA	I/O	I^2C0 data input/output pin.
		PWM1_CH4	I/O	PWM1 CH4 output/Capture input.
6	4	PA.11	I/O	General purpose digital I/O pin.
		I2C1_SCL	I/O	I^2C1 clock pin.
		PWM1_CH3	I/O	PWM1 CH3 output/Capture input.
7	5	PA.10	I/O	General purpose digital I/O pin.
		I2C1_SDA	I/O	I^2C1 data input/output pin.
		PWM1_CH2	I/O	PWM1 CH2 output/Capture input.
8	6	PA.9	I/O	General purpose digital I/O pin.
		I2C0_SCL	I/O	I^2C0 clock pin.
		UART1_nCTS	I	Clear to Send input pin for UART1.
9	7	PA.8	I/O	General purpose digital I/O pin.
		I2C0_SDA	I/O	I^2C0 data input/output pin.
		UART1_nRTS	O	Request to Send output pin for UART1.
10	8	PB.4	I/O	General purpose digital I/O pin.
		UART1_RXD	I	Data receiver input pin for UART1.
11	9	PB.5	I/O	General purpose digital I/O pin.
		UART1_TXD	O	Data transmitter output pin for UART1.
12		PB.6	I/O	General purpose digital I/O pin.

Pin No.		Pin Name	Pin Type	Description
LQFP 64-pin	LQFP 48-pin			
		UART1_nRTS	O	Request to Send output pin for UART1.
13		PB.7	I/O	General purpose digital I/O pin.
		UART1_nCTS	I	Clear to Send input pin for UART1.
14	10	LDO_CAP	P	LDO output pin.
15	11	V_{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
16	12	V_{SS}	P	Ground pin for digital circuit.
17	13	PB.0	I/O	General purpose digital I/O pin.
		UART0_RXD	I	Data receiver input pin for UART0.
18	14	PB.1	I/O	General purpose digital I/O pin.
		UART0_TXD	O	Data transmitter output pin for UART0.
19	15	PB.2	I/O	General purpose digital I/O pin.
		UART0_nRTS	O	Request to Send output pin for UART0.
		TM2_EXT	I	Timer2 external capture input pin.
		TM2	O	Timer2 toggle output pin.
		PWM1_BRAKE1	I	PWM1 brake input pin.
20	16	PB.3	I/O	General purpose digital I/O pin.
		UART0_nCTS	I	Clear to Send input pin for UART0.
		TM3_EXT	I	Timer3 external capture input pin.
		TM3	O	Timer3 toggle output pin.
		PWM1_BRAKE0	I	PWM1 brake input pin.
21	17	PD.6	I/O	General purpose digital I/O pin.
		CAN0_RXD	I	Data receiver input pin for CAN0.
		BPWM1_CH1	I/O	BPWM1 CH1 output/Capture input.
22	18	PD.7	I/O	General purpose digital I/O pin.
		CAN0_TXD	O	Data transmitter output pin for CAN0.
		BPWM1_CH0	I/O	BPWM1 CH0 output/Capture input.
23	19	PD.14	I/O	General purpose digital I/O pin.
		UART2_RXD	I	Data receiver input pin for UART2.
		BPWM0_CH5	I/O	BPWM0 CH5 output/Capture input.
24	20	PD.15	I/O	General purpose digital I/O pin.
		UART2_TXD	O	Data transmitter output pin for UART2.

Pin No.		Pin Name	Pin Type	Description
LQFP 64-pin	LQFP 48-pin			
		BPWM0_CH4	I/O	BPWM0 CH4 input/Capture input.
25	21	PC.3	I/O	General purpose digital I/O pin.
		SPI0_MOSI0	I/O	SPI0 MOSI (Master Out, Slave In) pin.
		BPWM0_CH3	O	BPWM0 CH3 input/Capture input.
26	22	PC.2	I/O	General purpose digital I/O pin.
		SPI0_MISO0	I/O	SPI0 MISO (Master In, Slave Out) pin.
		BPWM0_CH2	I	BPWM0 CH2 input/Capture input.
27	23	PC.1	I/O	General purpose digital I/O pin.
		SPI0_CLK	I/O	SPI0 serial clock pin.
		BPWM0_CH1	I/O	BPWM0 CH1 input/Capture input.
28	24	PC.0	I/O	General purpose digital I/O pin.
		SPI0_SS0	I/O	SPI0 slave select pin.
		BPWM0_CH0	I/O	BPWM0 CH0 input/Capture input.
29		PE.5	I/O	General purpose digital I/O pin.
		PWM0_CH5	I/O	PWM0 CH5 output/Capture input.
		TM1_EXT	I	Timer1 external capture input pin.
		TM1	O	Timer1 toggle output pin.
30		PB.11	I/O	General purpose digital I/O pin.
		TM3	I/O	Timer3 event counter input / toggle output.
		PWM0_CH4	I/O	PWM0 CH4 output/Capture input.
31		PB.10	I/O	General purpose digital I/O pin.
		TM2	I/O	Timer2 event counter input / toggle output.
32		PB.9	I/O	General purpose digital I/O pin.
		TM1	I/O	Timer1 event counter input / toggle output.
33		PC.11	I/O	General purpose digital I/O pin.
		PWM1_BRAKE1	I	PWM1 brake input pin.
34		PC.10	I/O	General purpose digital I/O pin.
		PWM1_BRAKE0	I	PWM1 brake input pin.
35		PC.9	I/O	General purpose digital I/O pin.
		PWM0_BRAKE1	I	PWM0 brake input pin.
36		PC.8	I/O	General purpose digital I/O pin.

Pin No.		Pin Name	Pin Type	Description
LQFP 64-pin	LQFP 48-pin			
		PWM0_BRAKE0	I	PWM0 brake input pin.
37	25	PA.15	I/O	General purpose digital I/O pin.
		PWM0_CH3	I/O	PWM0 CH3 output/Capture input.
38	26	PA.14	I/O	General purpose digital I/O pin.
		PWM0_CH2	I/O	PWM0 CH2 output/Capture input.
39	27	PA.13	I/O	General purpose digital I/O pin.
		PWM0_CH1	I/O	PWM0 CH1 output/Capture input.
		UART5_TXD	O	Data transmitter output pin for UART5.
40	28	PA.12	I/O	General purpose digital I/O pin.
		PWM0_CH0	I/O	PWM0 CH0 output/Capture input.
		UART5_RXD	I	Data receiver input pin for UART5.
41	29	PF.7	I/O	General purpose digital I/O pin.
		ICE_DAT	I/O	Serial wire debugger data pin.
42	30	PF.6	I/O	General purpose digital I/O pin.
		ICE_CLK	I	Serial wire debugger clock pin.
43	31	AV_{SS}	AP	Ground pin for analog circuit.
44	32	PA.0	I/O	General purpose digital I/O pin.
		ADC_CH0	AI	ADC_CH0 analog input.
		PWM0_CH4	I/O	PWM0 CH4 output/Capture input.
		I2C1_SCL	I/O	I^2C1 clock pin.
		UART5_TXD	O	Data transmitter output pin for UART5.
45	33	PA.1	I/O	General purpose digital I/O pin.
		ADC_CH1	AI	ADC_CH1 analog input.
		PWM0_CH5	I/O	PWM0 CH5 output/Capture input.
		I2C1_SDA	I/O	I^2C1 data input/output pin.
		UART5_RXD	I	Data receiver input pin for UART5.
46	34	PA.2	I/O	General purpose digital I/O pin.
		ADC_CH2	AI	ADC_CH2 analog input.
		PWM1_CH0	I/O	PWM1 CH0 output/Capture input.
		UART3_TXD	O	Data transmitter output pin for UART3.
47	35	PA.3	I/O	General purpose digital I/O pin.
		ADC_CH3	AI	ADC_CH3 analog input.

Pin No.		Pin Name	Pin Type	Description
LQFP 64-pin	LQFP 48-pin			
		PWM1_CH1	I/O	PWM1 CH1 output/Capture input.
		UART3_RXD	I	Data receiver input pin for UART3.
48	36	PA.4	I/O	General purpose digital I/O pin.
		ADC_CH4	AI	ADC_CH4 analog input.
49	37	PA.5	I/O	General purpose digital I/O pin.
		ADC_CH5	AI	ADC_CH5 analog input.
		UART3_RXD	I	Data receiver input pin for UART3.
50	38	PA.6	I/O	General purpose digital I/O pin.
		ADC_CH6	AI	ADC_CH6 analog input.
		UART3_TXD	O	Data transmitter output pin for UART3.
51	39	PA.7	I/O	General purpose digital I/O pin.
		ADC_CH7	AI	ADC_CH7 analog input.
		V_{REF}	AP	Voltage reference input for ADC.
52	40	AV_{DD}	AP	Power supply for internal analog circuit.
53	41	PC.7	I/O	General purpose digital I/O pin.
		UART4_RXD	I	Data reveiver input pin for UART4.
		I2C0_SCL	I/O	I^2C0 clock pin.
		PWM0_BRAKE1	I	PWM0 brake input pin.
54	42	PC.6	I/O	General purpose digital I/O pin.
		UART4_TXD	O	Data transmitter output pin for UART4.
		I2C0_SDA	I/O	I^2C0 data input/output pin.
		PWM0_BRAKE0	I	PWM0 brake input pin.
55		PC.15	I/O	General purpose digital I/O pin.
56		PC.14	I/O	General purpose digital I/O pin.
57	43	PB.15	I/O	General purpose digital I/O pin.
		INT1	I	External interrupt1 input pin.
		TM0_EXT	I	Timer0 external capture input pin.
		TM0	O	Timer0 toggle output pin.
		BPWM1_CH5	I/O	BPWM1 CH5 output/Capture input.
58	44	PF.0	I/O	General purpose digital I/O pin.
		XT1_OUT	O	External 4~24 MHz (high speed) crystal output pin.
59	45	PF.1	I/O	General purpose digital I/O pin.

Pin No.		Pin Name	Pin Type	Description
LQFP 64-pin	LQFP 48-pin			
		XT1_IN	**I**	External 4~24 MHz (high speed) crystal input pin.
60	46	nRESET	**I**	External reset input: active LOW, with an internal pull-up. Set this pin low reset chip to initial state.
61		V_{SS}	**P**	Ground pin for digital circuit.
62		V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
63	47	PF.8	**I/O**	General purpose digital I/O pin.
		CLKO	**O**	Frequency divider clock output pin.
		BPWM1_CH4	**I/O**	BPWM1 CH4 output/Capture input.
64	48	PB.8	**I/O**	General purpose digital I/O pin.
		STADC	**I**	ADC external trigger input.
		TM0	**I/O**	Timer0 event counter input / toggle output.
		CLKO	**O**	Frequency divider clock output pin.
		BPWM1_CH2	**I/O**	BPWM1 CH2 output/Capture input.

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

5 BLOCK DIAGRAM

5.1 NuMicro™ NUC131 Block Diagram

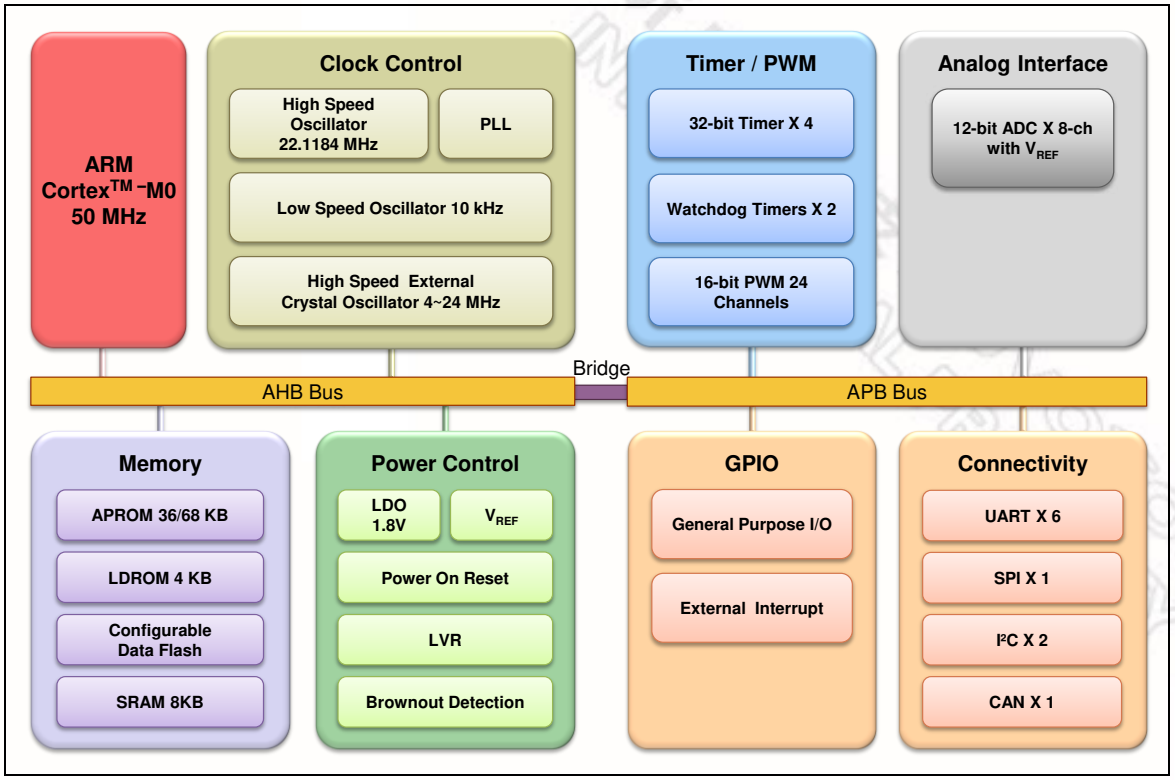

Figure 5-1 NuMicro™ NUC131 Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex™-M0 Core

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex™-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return.

Figure 6-1 shows the functional controller of processor.

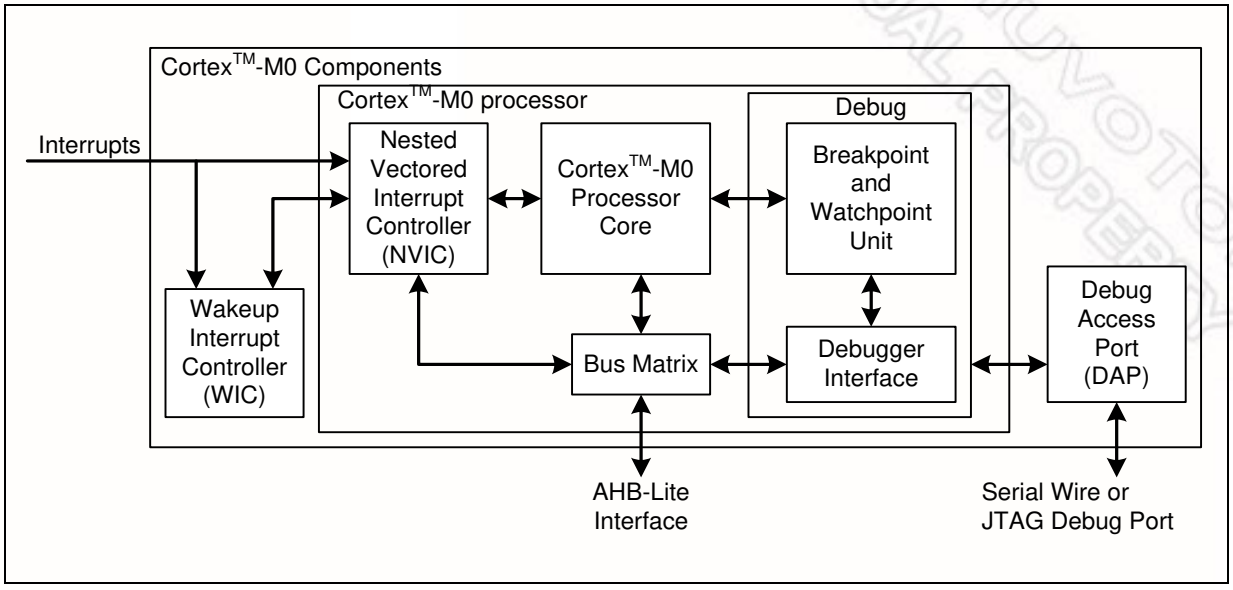

Figure 6-1 Functional Controller Diagram

The implemented device provides the following components and features:

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using Wait For Interrupt (WFI), Wait For Event

(WFE) instructions, or the return from interrupt sleep-on-exit feature

- NVIC:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode
- Debug support
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the following listed events. For these reset event flags can be read by RSTSRC register.

- Power-on Reset
- Low level on the nRESET pin
- Watchdog Time-out Reset
- Low Voltage Reset
- Brown-out Detector Reset
- CPU Reset
- System Reset

System Reset and Power-on Reset all reset the whole chip including all peripherals. The difference between System Reset and Power-on Reset is external crystal circuit and BS (ISPCON[1]) bit. System Reset does not reset external crystal circuit and BS (ISPCON[1]) bit, but Power-on Reset does.