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# NuMicro™ NUC230/240 Series DataSheet

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## 1 GENERAL DESCRIPTION

The NuMicro™ NUC230/240 series 32-bit microcontrollers are embedded with the ARM® Cortex™-M0 core with a cost equivalent to traditional 8-bit MCU for industrial control and applications requiring rich communication interfaces. The NuMicro™ NUC230/240 series includes NUC230 and NUC240 product lines.

The NuMicro™ NUC230 CAN Line is embedded with the Cortex™-M0 core running up to 72 MHz and features 32K/64K/128K bytes flash, 8K/16K bytes embedded SRAM, and 8 Kbytes loader ROM for the ISP. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timer, Window Watchdog Timer, RTC, PDMA with CRC calculation unit, UART, SPI, I<sup>2</sup>C, I<sup>2</sup>S, PWM Timer, GPIO, LIN, CAN, PS/2, Smart Card Host, 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-out Detector.

The NuMicro™ NUC240 Connectivity Line with USB 2.0 full-speed and CAN functions is embedded with the Cortex™-M0 core running up to 72 MHz and features 32K/64K/128K bytes flash, 8K/16K bytes embedded SRAM, and 8 Kbytes loader ROM for the ISP. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timer, Window Watchdog Timer, RTC, PDMA with CRC calculation unit, UART, SPI, I<sup>2</sup>C, I<sup>2</sup>S, PWM Timer, GPIO, LIN, CAN, PS/2, USB 2.0 FS Device, Smart Card Host, 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-out Detector.

Product Line	UART	SPI	I <sup>2</sup> C	USB	LIN	CAN	PS/2	I <sup>2</sup> S	SC
NUC230	●	●	●		●	●	●	●	●
NUC240	●	●	●	●	●	●	●	●	●

Table 1-1 NuMicro™ NUC230/240 Series Connectivity Support Table



## 2 FEATURES

The equipped features are dependent on the product line and their sub products.

### 2.1 NuMicro™ NUC230 Features – Automotive Line

- ARM® Cortex™-M0 core
  - Runs up to 72 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5 V to 5.5 V
- Flash Memory
  - 32K/64K/128K bytes Flash for program code
  - 8 KB flash for ISP loader
  - Supports In-System-Program (ISP) and In-Application-Program (IAP) application code update
  - 512 byte page erase for flash
  - Configurable Data Flash address and size for 128 KB system, fixed 4 KB Data Flash for the 32 KB and 64 KB system
  - Supports 2-wired ICP update through SWD/ICE interface
  - Supports fast parallel programming mode by external programmer
- SRAM Memory
  - 8K/16K bytes embedded SRAM
  - Supports PDMA mode
- PDMA (Peripheral DMA)
  - Supports 9 channels PDMA for automatic data transfer between SRAM and peripherals
  - Supports CRC calculation with four common polynomials, CRC-CCITT, CRC-8, CRC-16 and CRC-32
- Clock Control
  - Flexible selection for different applications
  - Built-in 22.1184 MHz high speed oscillator for system operation
    - Trimmed to  $\pm 1\%$  at  $+25\text{ }^{\circ}\text{C}$  and  $V_{DD} = 5\text{ V}$
    - Trimmed to  $\pm 3\%$  at  $-40\text{ }^{\circ}\text{C} \sim +105\text{ }^{\circ}\text{C}$  and  $V_{DD} = 2.5\text{ V} \sim 5.5\text{ V}$
  - Built-in 10 kHz low speed oscillator for Watchdog Timer and Wake-up operation
  - Supports one PLL, up to 72 MHz, for high performance system operation
  - External 4~24 MHz high speed crystal input for precise timing operation
  - External 32.768 kHz low speed crystal input for RTC function and low power system operation
- GPIO
  - Four I/O modes:
    - Quasi-bidirectional
    - Push-pull output
    - Open-drain output
    - Input only with high impedance
  - TTL/Schmitt trigger input selectable
  - I/O pin configured as interrupt source with edge/level setting
- Timer
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
  - Independent clock source for each timer
  - Provides one-shot, periodic, toggle and continuous counting operation modes
  - Supports event counting function
  - Supports input capture function
- Watchdog Timer
  - Multiple clock sources



- 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
- Wake-up from Power-down or Idle mode
- Interrupt or reset selectable on watchdog time-out
- Supports 4 selectable Watchdog Timer reset delay period(1026, 130, 18 or 3 WDT\_CLK)
- Window Watchdog Timer
  - 6-bit down counter with 11-bit prescale for wide range window selected
- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Supports battery power pin (VBAT)
  - Supports wake-up function
- PWM/Capture
  - Up to four built-in 16-bit PWM generators providing eight PWM outputs or four complementary paired PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
  - Supports One-shot or Auto-reload mode
  - Up to eight 16-bit digital capture timers (shared with PWM timers) providing eight rising/falling capture inputs
  - Supports Capture interrupt
- UART
  - Up to six UART controllers (three UART controllers are shared with SC)
  - UART ports with flow control (TXD, RXD, nCTS and nRTS)
  - UART0 with 64-byte FIFO is for high speed
  - UART1/2(optional) with 16-byte FIFO for standard device
  - Supports IrDA (SIR) and LIN function
  - Supports RS-485 9-bit mode and direction control
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports CTS wake-up function (UART0 and UART1 support)
  - Supports PDMA mode
- Smart Card Host (SC)
  - Supports up to three ISO-7816-3 ports
    - Compliant to ISO-7816-3 T=0, T=1
    - Separate receive / transmit 4 bytes entry FIFO for data payloads
    - Programmable transmission clock frequency
    - Programmable receiver buffer trigger level
    - Programmable guard time selection (11 ETU ~ 266 ETU)
    - One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
    - Supports auto inverse convention function
    - Supports transmitter and receiver error retry and error limit function
    - Supports hardware activation sequence process
    - Supports hardware warm reset sequence process
    - Supports hardware deactivation sequence process
    - Supports hardware auto deactivation sequence when detecting the card is removal
  - Supports up to three UART ports
    - Full duplex, asynchronous communications
    - Supports receiving / transmitting 4-bytes FIFO
    - Supports programmable baud rate generator for each channel
    - Programmable even, odd or no parity bit generation and detection
    - Programmable stop bit, 1 or 2 stop bit generation



- SPI
  - Up to four sets of SPI controllers
  - The maximum SPI clock rate of Master can up to 36 MHz (chip working at 5V)
  - The maximum SPI clock rate of Slave can up to 18 MHz (chip working at 5V)
  - Supports SPI Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - Two slave/device select lines in Master mode, and one slave/device select line in Slave mode
  - Supports Byte Suspend mode in 32-bit transmission
  - Supports PDMA mode
  - Supports three wire, no slave select signal, bi-direction interface
- I<sup>2</sup>C
  - Up to two sets of I<sup>2</sup>C devices
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allowing for versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports wake-up function
- I<sup>2</sup>S
  - Interface with external audio CODEC
  - Operate as either Master or Slave mode
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Supports mono and stereo audio data
  - Supports I<sup>2</sup>S and MSB justified data format
  - Provides two 8 word FIFO data buffers, one for transmitting and the other for receiving
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports two DMA requests, one for transmitting and the other for receiving
- PS/2 Device
  - Host communication inhibit and request to send detection
  - Reception frame error detection
  - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
  - Double buffer for data reception
  - Software override bus
- CAN 2.0
  - Supports CAN protocol version 2.0 part A and B
  - Bit rates up to 1M bit/s
  - 32 Message Objects
  - Each Message Object has its own identifier mask
  - Programmable FIFO mode (concatenation of Message Object)
  - Maskable interrupt
  - Disabled Automatic Re-transmission mode for Time Triggered CAN applications
  - Support wake-up function
- ADC
  - 12-bit SAR ADC with 1 MSPS (chip working at 5V)
  - Up to 8-ch single-end input or 4-ch differential input
  - Single scan/single cycle scan/continuous scan





- Each channel with individual result register
- Scan on enabled channels
- Threshold voltage detection
- Conversion started by software programming, external input or PWM Center-aligned trigger
- Supports PDMA mode
- Analog Comparator
  - Up to two analog comparators
  - External input or internal Band-gap voltage selectable at negative node
  - Interrupt when compare result change
  - Supports Power-down wake-up
- EBI (External bus interface)
  - Accessible space: 64 KB in 8-bit mode or 128 KB in 16-bit mode
  - Supports 8-/16-bit data width
  - Supports byte write in 16-bit data width mode
- 96-bit unique ID (UID)
- 128-bit unique customer ID(UCID)
- One built-in temperature sensor with 1°C resolution
- Brown-out Detector
  - With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage level: 2.0 V
- Operating Temperature: -40°C ~ 105°C
- Packages:
  - All Green package (RoHS)
  - LQFP 100-pin / 64-pin / 48-pin



## 2.2 NuMicro™ NUC240 Features – Connectivity Line

- ARM® Cortex™-M0 core
  - Runs up to 72 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Built-in LDO for wide operating voltage ranges from 2.5 V to 5.5 V
- Flash Memory
  - 32K/64K/128K bytes Flash for program code
  - 8 KB flash for ISP loader
  - Supports In-System-Program (ISP) and In-Application-Program (IAP) application code update
  - 512 byte page erase for flash
  - Configurable Data Flash address and size for 128 KB system, fixed 4 KB Data Flash for the 32 KB and 64 KB system
  - Supports 2-wired ICP update through SWD/ICE interface
- SRAM Memory
  - 8K/16K bytes embedded SRAM
  - Supports PDMA mode
- PDMA (Peripheral DMA)
  - Supports 9 channels PDMA for automatic data transfer between SRAM and peripherals
  - Supports CRC calculation with four common polynomials, CRC-CCITT, CRC-8, CRC-16 and CRC-32
- Clock Control
  - Flexible selection for different applications
  - Built-in 22.1184 MHz high speed oscillator for system operation
    - Trimmed to  $\pm 1\%$  at  $+25\text{ }^\circ\text{C}$  and  $V_{DD} = 5\text{ V}$
    - Trimmed to  $\pm 3\%$  at  $-40\text{ }^\circ\text{C} \sim +105\text{ }^\circ\text{C}$  and  $V_{DD} = 2.5\text{ V} \sim 5.5\text{ V}$
  - Built-in 10 kHz low speed oscillator for Watchdog Timer and Wake-up operation
  - Supports one PLL, up to 72 MHz, for high performance system operation
  - External 4~24 MHz high speed crystal input for USB and precise timing operation
  - External 32.768 kHz low speed crystal input for RTC function and low power system operation
- GPIO
  - Four I/O modes:
    - Quasi-bidirectional
    - Push-pull output
    - Open-drain output
    - Input only with high impedance
  - TTL/Schmitt trigger input selectable
  - I/O pin configured as interrupt source with edge/level setting
- Timer
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
  - Independent clock source for each timer
  - Provides one-shot, periodic, toggle and continuous counting operation modes
  - Supports event counting function
  - Supports input capture function
- Watchdog Timer
  - Multiple clock sources
  - 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
  - Wake-up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
  - Supports 4 selectable Watchdog Timer reset delay period(1026, 130, 18 or 3 WDT\_CLK)



- Window Watchdog Timer
  - 6-bit down counter with 11-bit prescale for wide range window selected
- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Supports battery power pin (VBAT)
  - Supports wake-up function
- PWM/Capture
  - Up to four built-in 16-bit PWM generators providing eight PWM outputs or four complementary paired PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
  - Supports One-shot or Auto-reload mode
  - Up to eight 16-bit digital capture timers (shared with PWM timers) providing eight rising/falling capture inputs
  - Supports Capture interrupt
- UART
  - Up to six UART controllers (three UART controllers are shared with SC)
  - UART ports with flow control (TXD, RXD, nCTS and nRTS)
  - UART0 with 64-byte FIFO is for high speed
  - UART1/2(optional) with 16-byte FIFO for standard device
  - Supports IrDA (SIR) and LIN function
  - Supports RS-485 9-bit mode and direction control
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports CTS wake-up function (UART0 and UART1 support)
  - Supports PDMA mode
- Smart Card Host (SC)
  - Supports up to three ISO-7816-3 ports
    - Compliant to ISO-7816-3 T=0, T=1
    - Separate receive / transmit 4 bytes entry FIFO for data payloads
    - Programmable transmission clock frequency
    - Programmable receiver buffer trigger level
    - Programmable guard time selection (11 ETU ~ 266 ETU)
    - One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
    - Supports auto inverse convention function
    - Supports transmitter and receiver error retry and error limit function
    - Supports hardware activation sequence process
    - Supports hardware warm reset sequence process
    - Supports hardware deactivation sequence process
    - Supports hardware auto deactivation sequence when detecting the card is removal
  - Supports up to three UART ports
    - Full duplex, asynchronous communications
    - Supports receiving / transmitting 4-bytes FIFO
    - Supports programmable baud rate generator for each channel
    - Programmable even, odd or no parity bit generation and detection
    - Programmable stop bit, 1 or 2 stop bit generation
- SPI
  - Up to four sets of SPI controllers
  - The maximum SPI clock rate of Master can up to 36 MHz (chip working at 5V)
  - The maximum SPI clock rate of Slave can up to 18 MHz (chip working at 5V)



- Supports SPI Master/Slave mode
- Full duplex synchronous serial data transfer
- Variable length of transfer data from 8 to 32 bits
- MSB or LSB first data transfer
- Rx and Tx on both rising or falling edge of serial clock independently
- Two slave/device select lines in Master mode, and one slave/device select line in Slave mode
- Supports Byte Suspend mode in 32-bit transmission
- Supports PDMA mode
- Supports three wire, no slave select signal, bi-direction interface
- I<sup>2</sup>C
  - Up to two sets of I<sup>2</sup>C devices
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allowing for versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports wake-up function
- I<sup>2</sup>S
  - Interface with external audio CODEC
  - Operate as either Master or Slave mode
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Supports mono and stereo audio data
  - Supports I<sup>2</sup>S and MSB justified data format
  - Provides two 8 word FIFO data buffers, one for transmitting and the other for receiving
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports two DMA requests, one for transmitting and the other for receiving
- PS/2 Device
  - Host communication inhibit and request to send detection
  - Reception frame error detection
  - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
  - Double buffer for data reception
  - Software override bus
- CAN 2.0
  - Supports CAN protocol version 2.0 part A and B
  - Bit rates up to 1M bit/s
  - 32 Message Objects
  - Each Message Object has its own identifier mask
  - Programmable FIFO mode (concatenation of Message Object)
  - Maskable interrupt
  - Disabled Automatic Re-transmission mode for Time Triggered CAN applications
  - Supports Power-down wake-up function
- USB 2.0 Full-Speed Device
  - One set of USB 2.0 FS Device 12 Mbps
  - On-chip USB Transceiver
  - Provides 1 interrupt source with 4 interrupt events
  - Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provides 8 programmable endpoints
  - Includes 512 Bytes internal SRAM as USB buffer





- Provides remote wake-up capability
- ADC
  - 12-bit SAR ADC with 1 MSPS(chip working at 5V)
  - Up to 8-ch single-end input or 4-ch differential input
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion started by software programming, external input or PWM Center-aligned trigger
  - Supports PDMA mode
- Analog Comparator
  - Up to two analog comparators
  - External input or internal Band-gap voltage selectable at negative node
  - Interrupt when compare result change
  - Supports Power-down wake-up
- EBI (External bus interface)
  - Accessible space: 64 KB in 8-bit mode or 128 KB in 16-bit mode
  - Supports 8-/16-bit data width
  - Supports byte write in 16-bit data width mode
- 96-bit unique ID (UID)
- 128-bit unique customer ID(UCID)
- One built-in temperature sensor with 1°C resolution
- Brown-out Detector
  - With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage level: 2.0 V
- Operating Temperature: -40°C ~ 105°C
- Packages:
  - All Green package (RoHS)
  - LQFP 100-pin / 64-pin / 48-pin

### 3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SDIO	Secure Digital Input/Output
SPI	Serial Peripheral Interface



SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations



## 4 PARTS INFORMATION LIST AND PIN CONFIGURATION

### 4.1 NuMicro™ NUC230/240xxxAE Selection Guide

#### 4.1.1 NuMicro™ NUC230 Automotive Line Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-bit)	Connectivity						I <sup>2</sup> S	SC	Comp.	PWM	ADC (12-bit)	RTC	EBI	ISP/ICP/IAP	Package
							UART	SPI	I <sup>2</sup> C	USB	LIN	CAN									
NUC230LC2AE	32	8	4	8	35	4	5	1	2	-	3	2	1	2	1	4	7	v	-	v	LQFP48
NUC230LD2AE	64	8	4	8	35	4	5	1	2	-	3	2	1	2	1	4	7	v	-	v	LQFP48
NUC230LE3AE	128	16	Config.	8	35	4	5	1	2	-	3	2	1	2	1	4	7	v	-	v	LQFP48
NUC230SC2AE	32	8	4	8	49	4	5	2	2	-	3	2	1	2	2	6	7	v	v	v	LQFP64
NUC230SD2AE	64	8	4	8	49	4	5	2	2	-	3	2	1	2	2	6	7	v	v	v	LQFP64
NUC230SE3AE	128	16	Config.	8	49	4	5	2	2	-	3	2	1	2	2	6	7	v	v	v	LQFP64
NUC230VE3AE	128	16	Config.	8	83	4	6	4	2	-	3	2	1	3	2	8	8	v	v	v	LQFP100

#### 4.1.2 NuMicro™ NUC240 Connectivity Line Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-bit)	Connectivity						I <sup>2</sup> S	SC	Comp.	PWM	ADC (12-bit)	RTC	EBI	ISP/ICP/IAP	Package
							UART	SPI	I <sup>2</sup> C	USB	LIN	CAN									
NUC240LC2AE	32	8	4	8	31	4	4	1	2	1	2	2	1	1	1	4	7	v	-	v	LQFP48
NUC240LD2AE	64	8	4	8	31	4	4	1	2	1	2	2	1	1	1	4	7	v	-	v	LQFP48
NUC240LE3AE	128	16	Config.	8	31	4	4	1	2	1	2	2	1	1	1	4	7	v	-	v	LQFP48
NUC240SC2AE	32	8	4	8	45	4	5	2	2	1	3	2	1	2	2	4	7	v	v	v	LQFP64
NUC240SD2AE	64	8	4	8	45	4	5	2	2	1	3	2	1	2	2	4	7	v	v	v	LQFP64
NUC240SE3AE	128	16	Config.	8	45	4	5	2	2	1	3	2	1	2	2	4	7	v	v	v	LQFP64
NUC240VE3AE	128	16	Config.	8	79	4	6	4	2	1	3	2	1	3	2	8	8	v	v	v	LQFP100



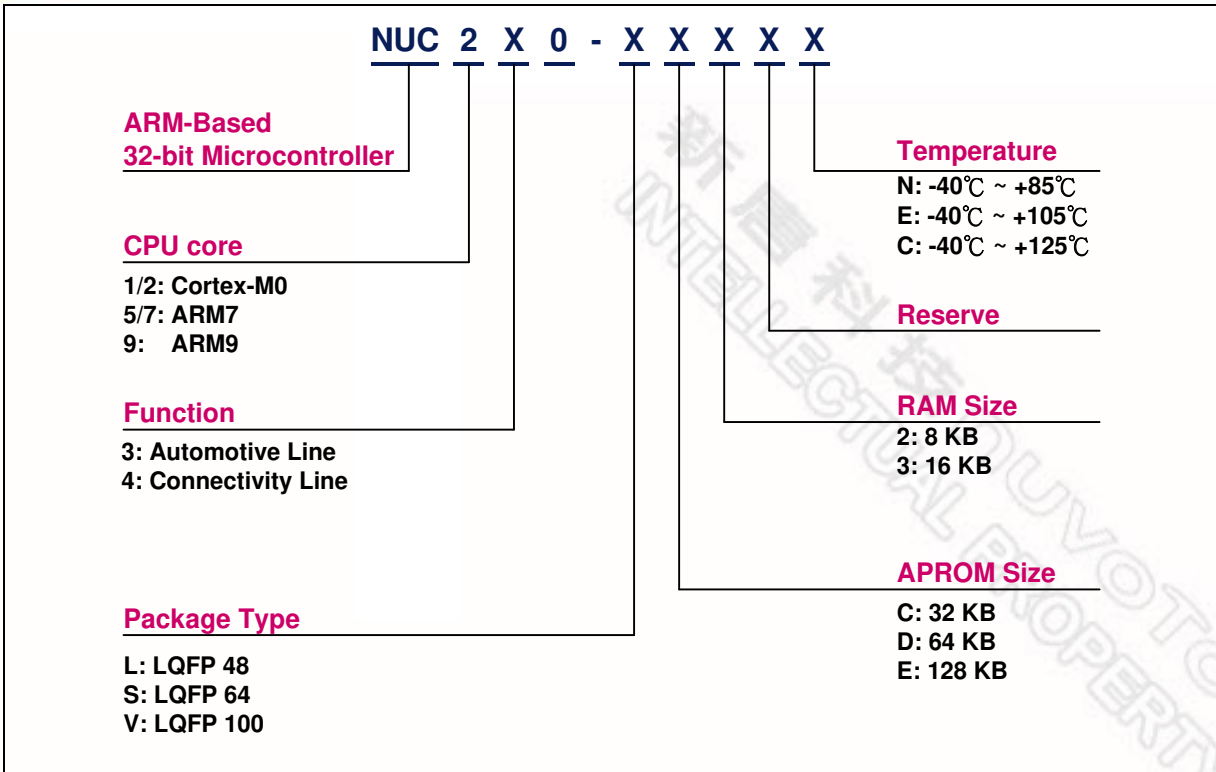


Figure 4-1 NuMicro™ NUC230/240 Series Selection Code



## 4.2 Pin Configuration

### 4.2.1 NuMicro™ NUC230 Pin Diagram

#### 4.2.1.1 NuMicro™ NUC230VxxAE LQFP 100 pin

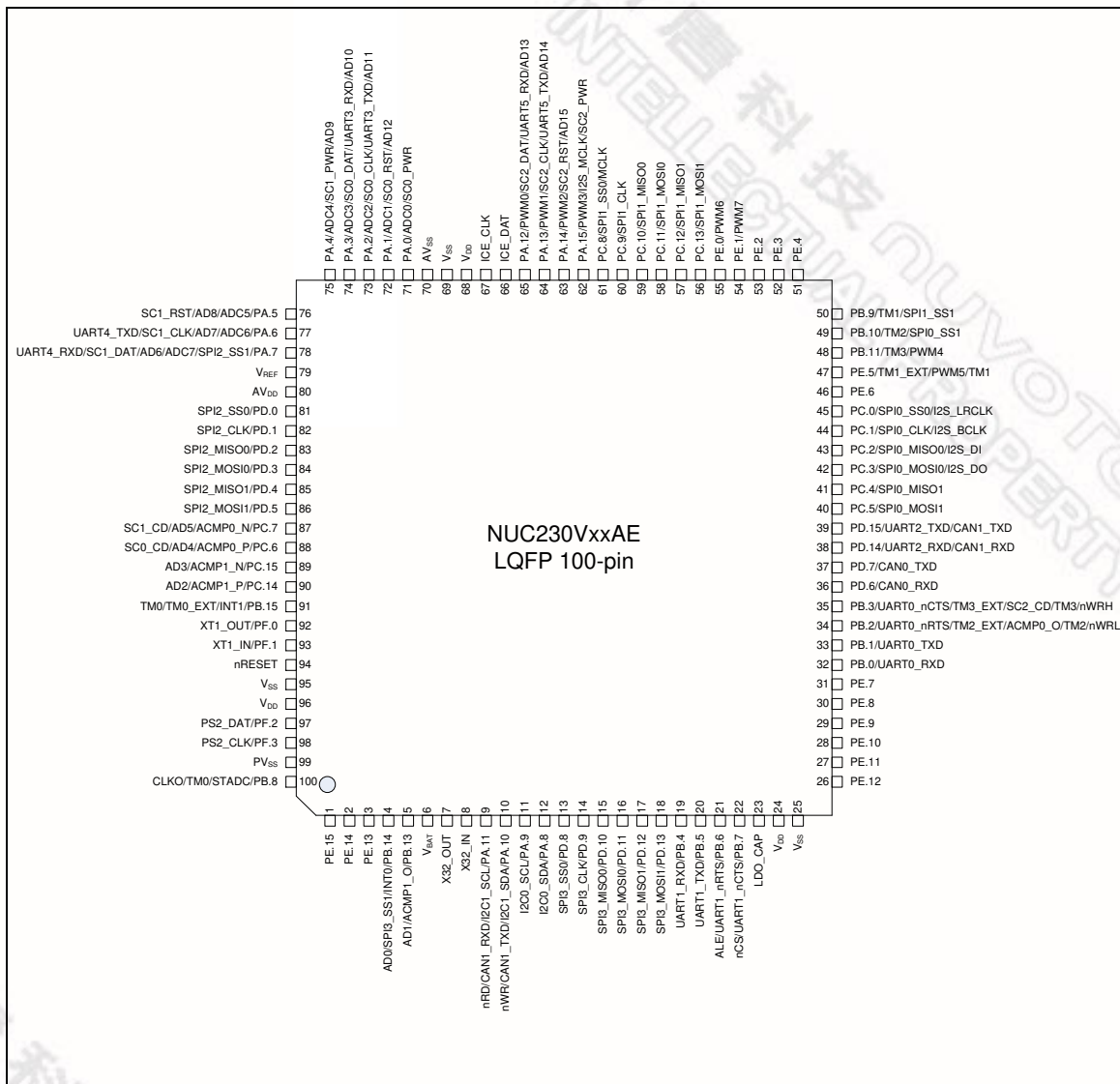


Figure 4-2 NuMicro™ NUC230VxxAE LQFP 100-pin Diagram

NUMICRO™ NUC230/240 DATASHEET



4.2.1.2 NuMicro™ NUC230SxxAE LQFP 64 pin

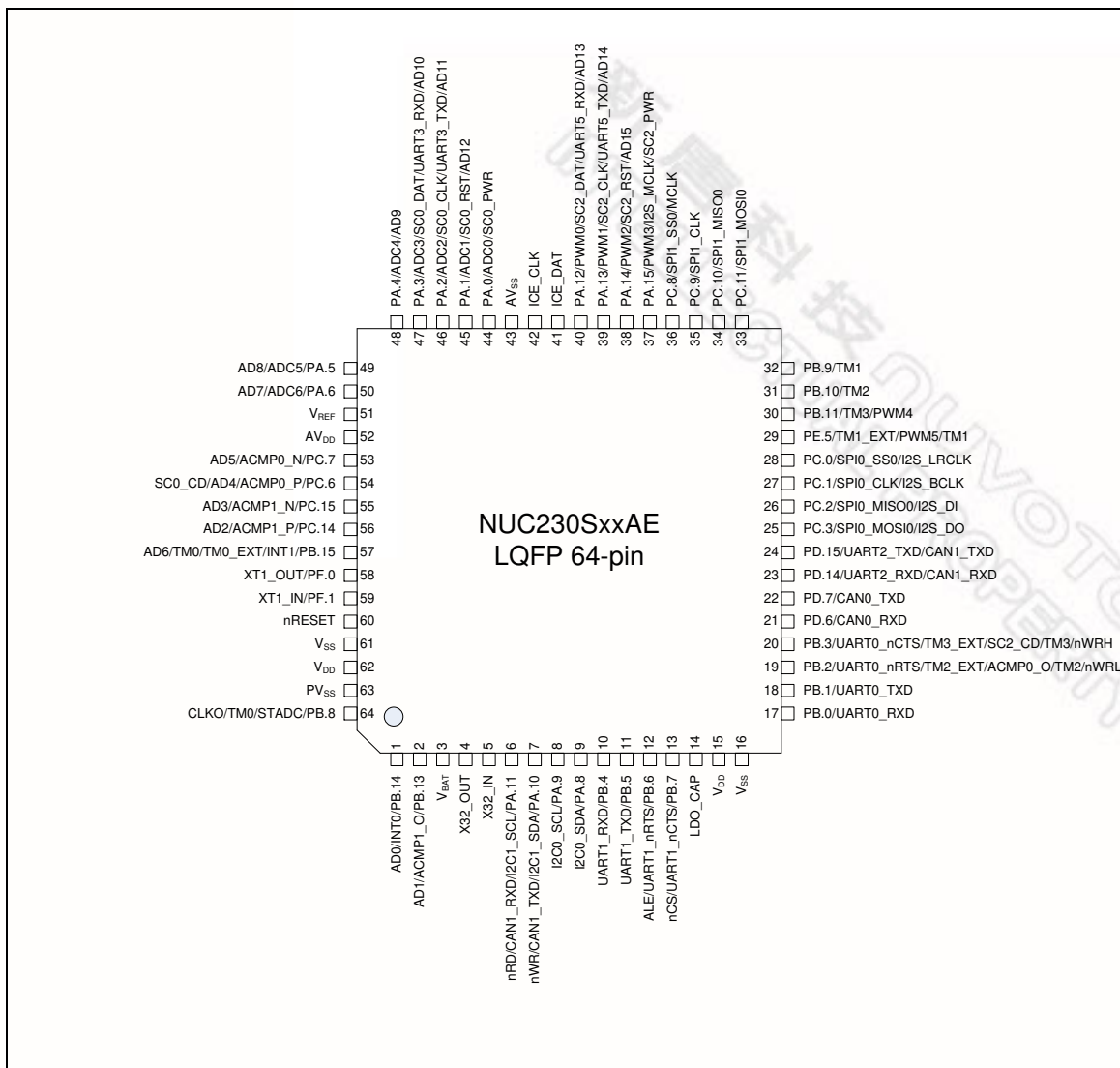


Figure 4-3 NuMicro™ NUC230SxxAE LQFP 64-pin Diagram



4.2.1.3 NuMicro™ NUC230LxxAE LQFP 48 pin

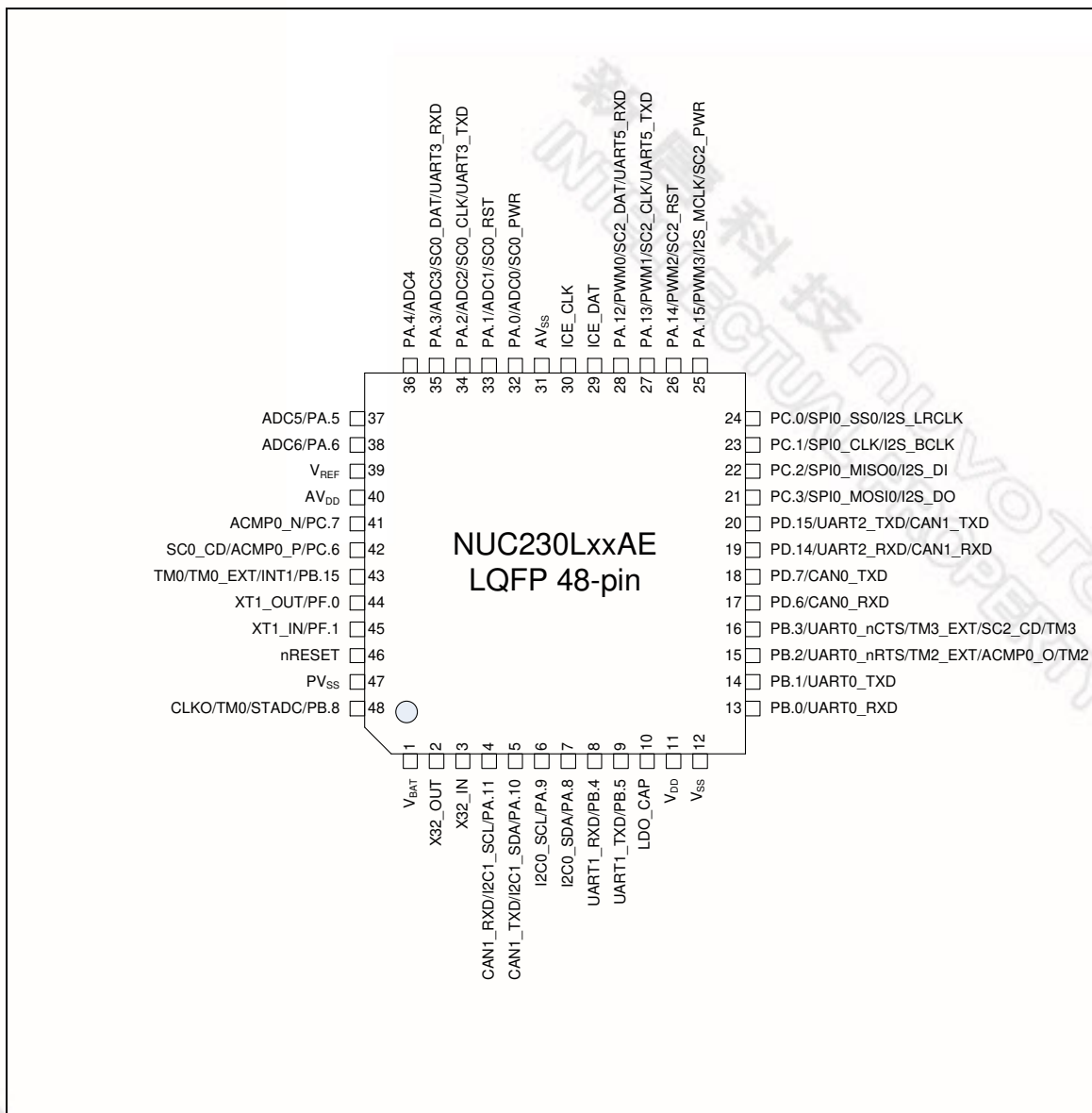


Figure 4-4 NuMicro™ NUC230LxxAE LQFP 48-pin Diagram



### 4.2.2 NuMicro™ NUC240 Pin Diagram

#### 4.2.2.1 NuMicro™ NUC240VxxAE LQFP 100 pin

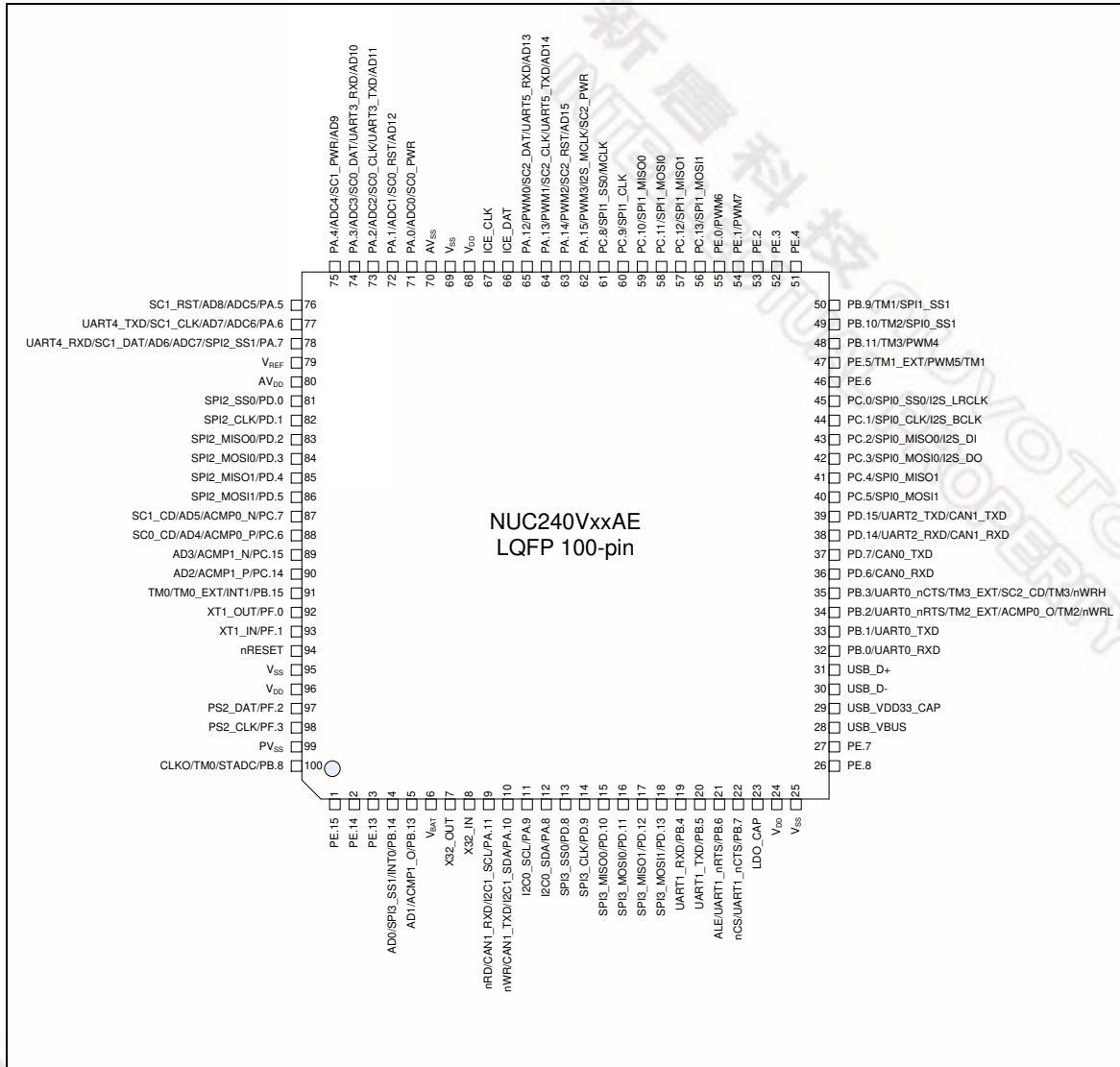


Figure 4-5 NuMicro™ NUC240VxxAE LQFP 100-pin Diagram





4.2.2.2 NuMicro™ NUC240SxxAE LQFP 64 pin

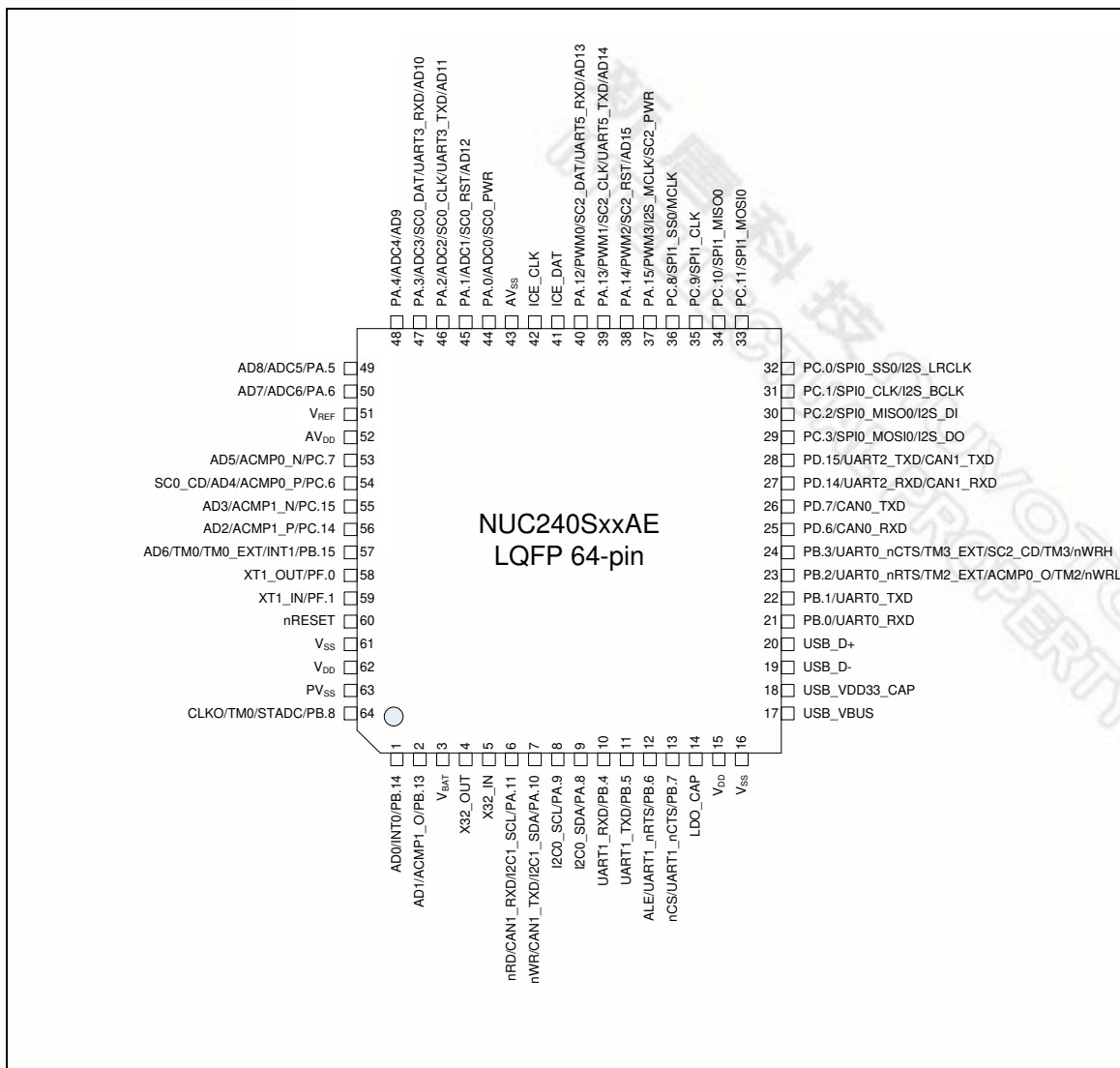


Figure 4-6 NuMicro™ NUC240SxxAE LQFP 64-pin Diagram