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# NUS2401SNT1

## Integrated PNP/NPN Digital Transistors Array

This new option of integrated digital transistors is designed to replace a discrete solution array of three transistors and their external resistor bias network. BRTs (Bias Resistor Transistors) contain a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT technology eliminates these individual components by integrating them into a single device, therefore the integration of three BRTs results in a significant reduction of both system cost and board space. This new device is packaged in the SC-74/Case 318F package which is designed for low power surface mount applications.

### Features

- Integrated Design
- Reduces Board Space and Components Count
- Simplifies Circuitry Design
- Offered in Surface Mount Package Technology (SC-74)
- Available in 3000 Unit Tape and Reel
- Pb-Free Package is Available

### Applications

- Audio Muting Applications
- Drive Circuits Applications
- Industrial: Small Appliances, Security Systems, Automated Test
- Consumer: TVs and VCRs, Stereo Receivers, CD Players, Cassette Recorders

**MAXIMUM RATINGS** (Maximum ratings are those values beyond which device damage can occur. Electrical Characteristics are not guaranteed over this range.)

Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{(BR)CBO}$	60	Vdc
Collector-Emitter Voltage	$V_{(BR)CEO}$	50	Vdc
Emitter-Base Voltage	$V_{(BR)EBO}$	7.0	Vdc
Collector Current - Continuous	$I_C$	200	mAdc

### THERMAL CHARACTERISTICS

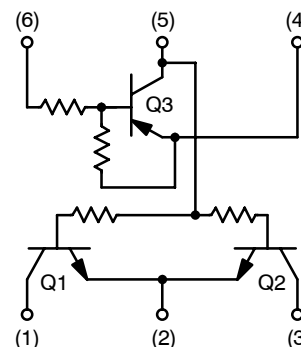
Characteristic	Symbol	Max	Unit
Power Dissipation	$P_D$	350	mW
Junction Temperature	$T_J$	150	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



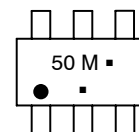
**ON Semiconductor®**

<http://onsemi.com>



SC-74  
CASE 318F  
STYLE 4

### MARKING DIAGRAM



- 50 = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping†
NUS2401SNT1	SC-74	3000/Tape & Reel
NUS2401SNT1G	SC-74 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## ELECTRICAL CHARACTERISTICS

(Unless otherwise noted:  $T_J = 25^\circ\text{C}$  for typical values, common for Q1, Q2, and Q3, – minus signed for Q3 (PNP) omitted.)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Base Cutoff Current ( $V_{CB} = 50\text{ V}$ , $I_E = 0$ )	$I_{CBO}$	–	–	100	nAdc
Collector–Emitter Cutoff Current ( $V_{CE} = 50\text{ V}$ , $I_B = 0$ )	$I_{CEO}$	–	–	500	nAdc
Emitter–Base Cutoff Current ( $V_{CE} = 6.0\text{ V}$ , $I_C = 0$ )	$I_{EBO}$	–	–	500	$\mu\text{A}$
	Q3	–	–	0.1	
	Q1, Q2	–	–		
Collector–Base Breakdown Voltage ( $I_C = 10\ \mu\text{A}$ , $I_E = 0$ )	$V_{(BR)CBO}$	50	–	–	V
Collector–Emitter Breakdown Voltage (Note 1) ( $I_C = 2.0\text{ mA}$ , $I_B = 0$ )	$V_{(BR)CEO}$	50	–	–	V

## ON CHARACTERISTICS (Note 1)

DC Current Gain	Q3	$h_{FE}$	35	60	–	
	Q1, Q2		150	350	–	
Collector–Emitter Saturation Voltage ( $I_C = 10\text{ mA}$ , $I_B = 0.3\text{ mA}$ )	Q3	$V_{CE(sat)}$	–	–	0.25	Vdc
( $I_C = 10\text{ mA}$ , $I_B = 1.0\text{ mA}$ )	Q1, Q2		–	–	0.25	
Output Voltage (on) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 2.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )		$V_{OL}$	–	–	0.2	V
Output Voltage (off) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 0.25\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )		$V_{OH}$	4.9	–	–	V
Input Resistor	Q3	R1	7.0	10	13	$\text{k}\Omega$
	Q1, Q2		0.13	0.175	0.22	
Resistor Ratio	Q3	R1/R2	–	1.0	–	
	Q1, Q2		–	$\infty$	–	

1. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty Cycle < 2%.

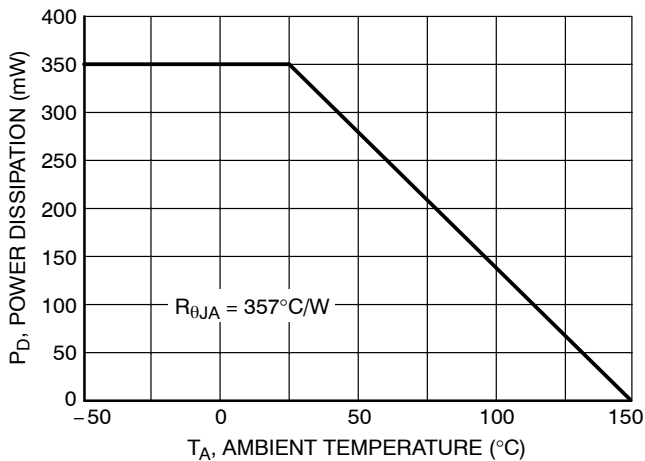


Figure 1. Derating Curve

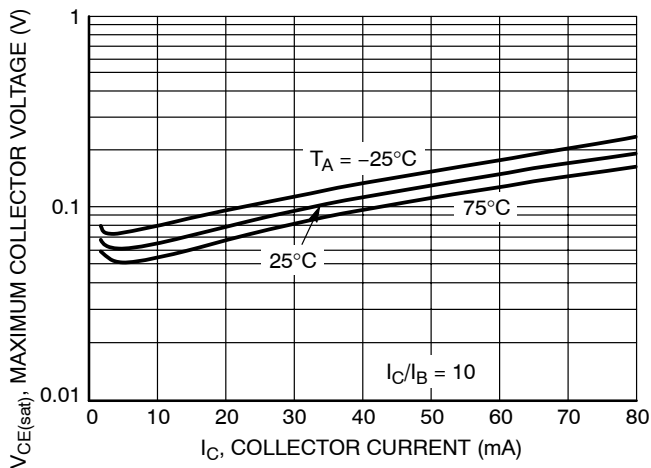


Figure 2. Maximum Collector Voltage versus Collector Current

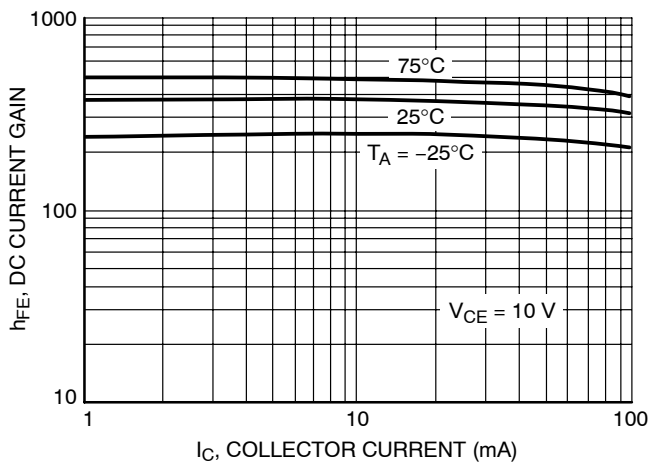


Figure 3. DC Current Gain

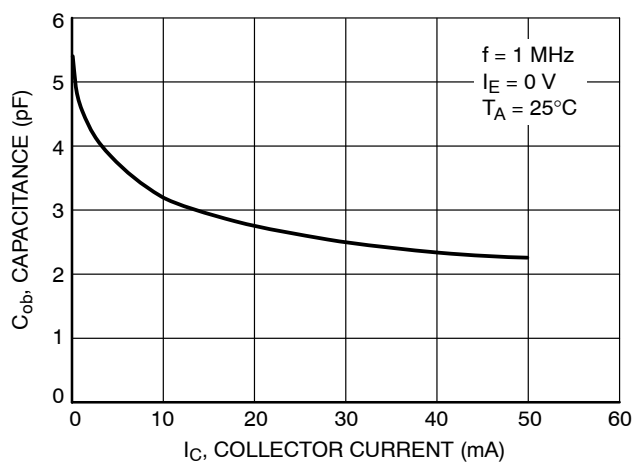


Figure 4. Output Capacitance

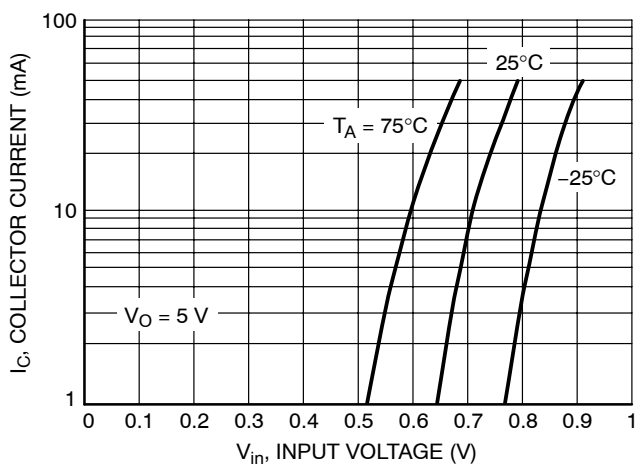


Figure 5. Output Current versus Input Voltage

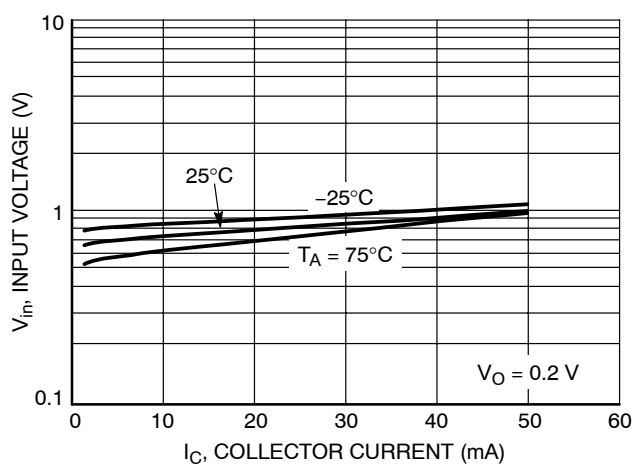


Figure 6. Input Voltage versus Output Current

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## TYPICAL ELECTRICAL CHARACTERISTICS – Q3 (PNP)

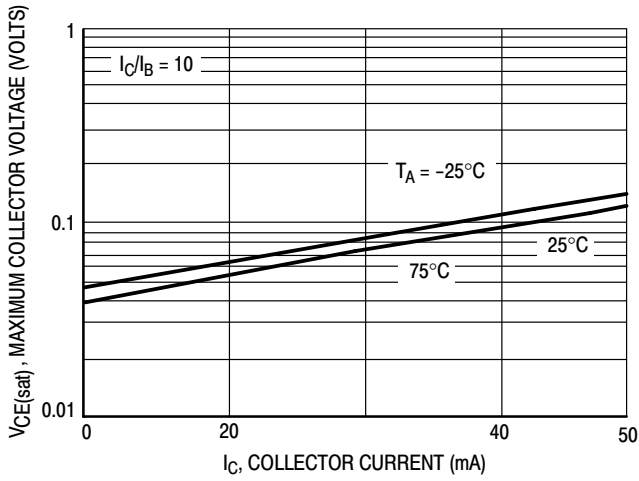


Figure 7.  $V_{CE(sat)}$  versus  $I_C$

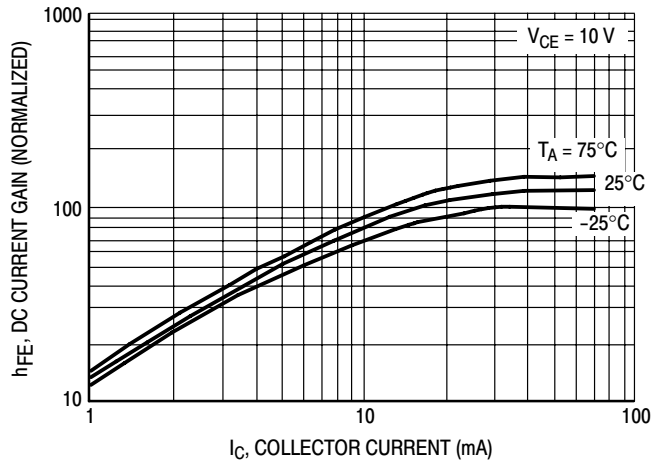


Figure 8. DC Current Gain

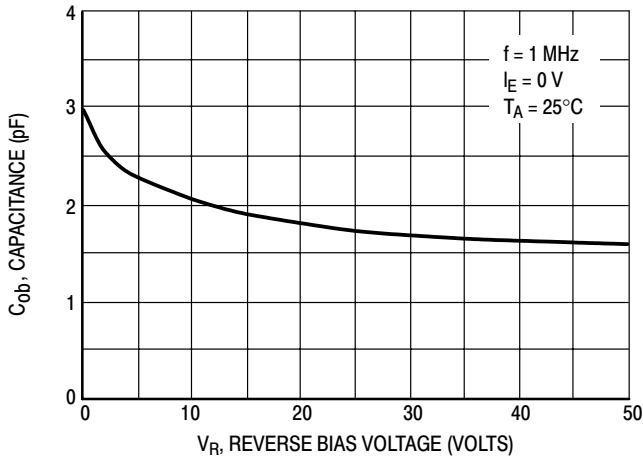


Figure 9. Output Capacitance

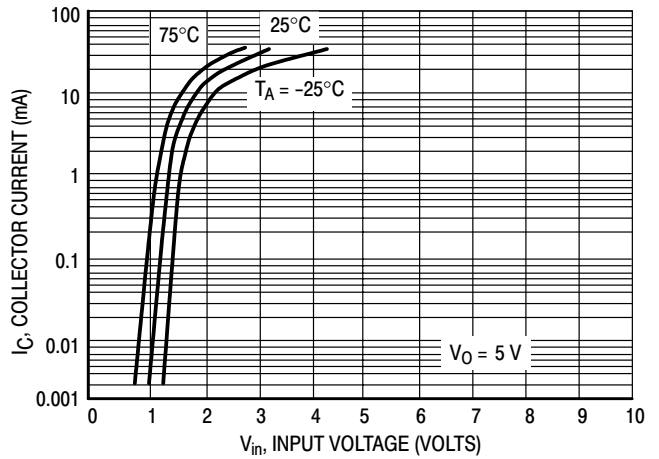


Figure 10. Output Current versus Input Voltage

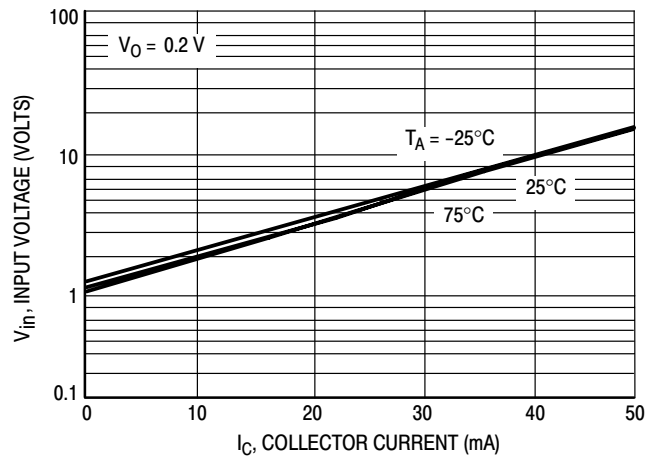
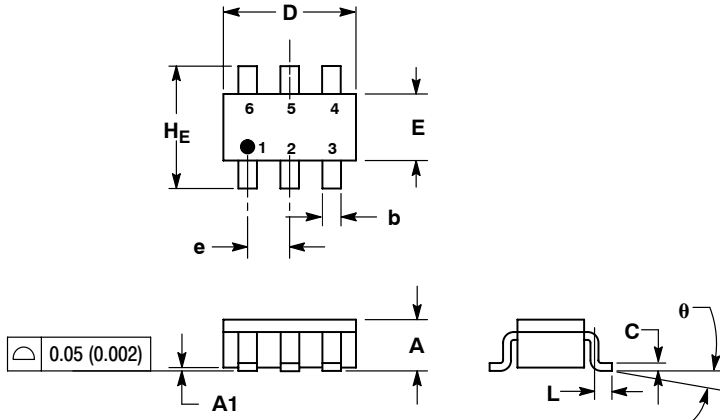


Figure 11. Input Voltage versus Output Current

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## PACKAGE DIMENSIONS

### SC-74 CASE 318F-05 ISSUE L



#### NOTES:

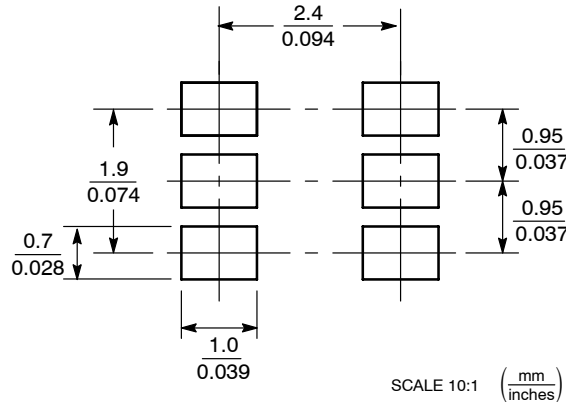
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F-01, -02, -03 OBSOLETE. NEW STANDARD 318F-04.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	-	10°	0°	-	10°

#### STYLE 4:

- PIN 1. COLLECTOR 2  
 2. EMITTER 1/EMITTER 2  
 3. COLLECTOR 1  
 4. EMITTER 3  
 5. BASE 1/BASE 2/COLLECTOR 3  
 6. BASE 3

#### SOLDERING FOOTPRINT\*



SCALE 10:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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