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Integrated Power MOSFET with PNP Low V_{CE(sat)} Switching Transistor

This integrated device represents a new level of safety and board–space reduction by combining the 20 V P–Channel FET with a PNP Silicon Low $V_{\text{CE(sat)}}$ switching transistor. This newly integrated product provides higher efficiency and accuracy for battery powered portable electronics.

Features

- Low R_{DS(on)} (MOSFET) and Low V_{CE(sat)} (Transistor)
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive (MOSFET)
- Performance DFN Package
- This is a Pb-Free Device

Applications

Power Management in Portable and Battery-Powered Products; i.e.,
 Cellular and Cordless Telephones and PCMCIA Cards

MAXIMUM RATINGS FOR P-CHANNEL FET

(T_A = 25°C unless otherwise noted)

Rating	Symbol	5 sec	Steady State	Unit		
Drain-Source Voltage	V _{DS}	-20		V		
Gate-Source Voltage	V _{GS}	±12		±12		V
Continuous Drain Current $(T_J = 150^{\circ}C)$ (Note 1) $T_A = 25^{\circ}C$ $T_A = 85^{\circ}C$	I _D	-5.3 -3.8	-3.9 -2.8	Α		
Pulsed Drain Current	I _{DM}	±20		Α		
Continuous Source Current (Note 1)	I _S	-5.3 -3.9		Α		
Maximum Power Dissipation (Note 1) T _A = 25°C T _A = 85°C	P _D	2.5 1.3	1.3 0.7	W		
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150		°C		

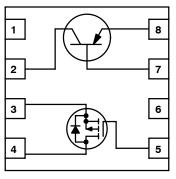
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).



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(Top View)

8

DFN8 CASE 506AL

MARKING DIAGRAM

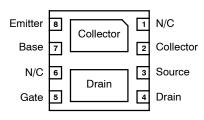


A = Assembly Location Y = Year

WW = Work Week
■ Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



(Bottom View)

ORDERING INFORMATION

Device	Package	Shipping [†]
NUS5530MNR2G	DFN8 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS FOR PNP TRANSISTORS $(T_A = 25^{\circ}C)$

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V _{CEO}	-35	Vdc
Collector-Base Voltage	V _{CBO}	-55	Vdc
Emitter-Base Voltage	V _{EBO}	-5.0	Vdc
Collector Current - Continuous	Ic	-2.0	Adc
Collector Current - Peak	I _{CM}	-7.0	А
Electrostatic Discharge	ESD	HBM Class 3 MM Class C	

THERMAL CHARACTERISTICS FOR P-CHANNEL FET

Characteristic	Symbol	Тур	Max	Unit
Maximum Junction-to-Ambient (Note 4) t ≤ 5 sec Steady State	$R_{ hetaJA}$	40 80	50 95	°C/W
Maximum Junction-to-Foot (Drain) Steady State	$R_{ hetaJF}$	15	20	°C/W

THERMAL CHARACTERISTICS FOR PNP TRANSISTORS

Characteristic	Symbol	Max	Unit
Total Device Dissipation $T_{\Delta} = 25^{\circ}C$	P _D (Note 1)	635	mW
Derate above 25°C		5.1	mW/°C
Thermal Resistance, Junction-to-Ambient	R _{θJA} (Note 1)	200	°C/W
Total Device Dissipation $T_{\Delta} = 25^{\circ}C$	P _D (Note 2)	1.35	W
Derate above 25°C		11	mW/°C
Thermal Resistance, Junction-to-Ambient	R _{θJA} (Note 2)	90	°C/W
Thermal Resistance, Junction-to-Lead #1	$R_{ heta JL}$	15	°C/W
Total Device Dissipation (Single Pulse < 10 sec)	P _{Dsingle} (Notes 2 & 3)	2.75	W
Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C

FR-4 @ 100 mm², 1 oz copper traces.
 FR-4 @ 500 mm², 1 oz copper traces.
 Thermal response.

ELECTRICAL CHARACTERISTICS FOR P-CHANNEL FET ($T_J = 25^{\circ}C$ unless otherwise noted)

		-	-			
Characteristic	Symbol	Test Condition	Min	Тур	Max	Unit
Static				•		
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-0.6		-1.2	V
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1.0	μΑ
		$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V},$ $T_{J} = 85^{\circ}\text{C}$			-5.0	
On-State Drain Current (Note 5)	I _{D(on)}	$V_{DS} \leq -5.0 \text{ V}, V_{GS} = -4.5 \text{ V}$	-20			Α
Drain-Source On-State Resistance (Note 5)	r _{DS(on)}	$V_{GS} = -3.6 \text{ V}, I_D = -1.0 \text{ A}$	-	0.050	0.06	Ω
		$V_{GS} = -2.5 \text{ V}, I_D = -1.0 \text{ A}$		0.070	0.083	
Forward Transconductance (Note 5)	9 _{fs}	$V_{DS} = -10 \text{ V}, I_{D} = -3.9 \text{ A}$		12		Mhos
Diode Forward Voltage (Note 5)	V_{SD}	I _S = -2.1 A, V _{GS} = 0 V		-0.8	-1.2	V
Dynamic (Note 6)	•		•	•	•	
Total Gate Charge	Q_{G}			9.7	22	nC
Gate-Source Charge	Q _{GS}	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V},$ $I_{D} = -3.9 \text{ A}$		1.2		
Gate-Drain Charge	Q_{GD}			3.6		
Input Capacitance	C _{iss}			710		pF
Output Capacitance	C _{oss}	$V_{DS} = -5.0 \text{ Vdc}, V_{GS} = 0 \text{ Vdc},$ f = 1.0 MHz		400		
Reverse Transfer Capacitance	C _{rss}			140		
Turn-On Delay Time	t _{d(on)}			14	30	ns
Rise Time	t _r	$V_{DD} = -10 \text{ V}, R_L = 10 \Omega$		22	55	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong -1.0 \text{ A}, V_{GEN} = -4.5 \text{ V},$ $R_G = 6 \Omega$		42	100	
Fall Time	t _f			35	70	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -1.1 A, di/dt = 100 A/μs		30	60	

Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).
 Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Guaranteed by design, not subject to production testing.

ELECTRICAL CHARACTERISTICS FOR PNP TRANSISTORS ($T_A = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit	
OFF CHARACTERISTICS						
Collector - Emitter Breakdown Voltage (I _C = -10 mAdc, I _B = 0)	V _{(BR)CEO}	-35	-45	-	Vdc	
Collector – Base Breakdown Voltage (I _C = -0.1 mAdc, I _E = 0)	V _{(BR)CBO}	-55	-65	-	Vdc	
Emitter – Base Breakdown Voltage (I _E = -0.1 mAdc, I _C = 0)	V _{(BR)EBO}	-5.0	-7.0	-	Vdc	
Collector Cutoff Current (V _{CB} = -35 Vdc, I _E = 0)	I _{CBO}	-	-0.03	-0.1	μAdc	
Collector-Emitter Cutoff Current (V _{CES} = -35 Vdc)	I _{CES}	-	-0.03	-0.1	μAdc	
Emitter Cutoff Current (V _{EB} = -6.0 Vdc)	I _{EBO}	-	-0.01	-0.1	μAdc	
ON CHARACTERISTICS						
DC Current Gain (Note 7) $(I_C = -1.0 \text{ A}, V_{CE} = -2.0 \text{ V})$ $(I_C = -1.5 \text{ A}, V_{CE} = -2.0 \text{ V})$ $(I_C = -2.0 \text{ A}, V_{CE} = -2.0 \text{ V})$	h _{FE}	100 100 100	200 200 200	- 400 -		
Collector – Emitter Saturation Voltage (Note 7) ($I_C = -0.1 \text{ A}$, $I_B = -0.010 \text{ A}$) ($I_C = -1.0 \text{ A}$, $I_B = -0.010 \text{ A}$) ($I_C = -2.0 \text{ A}$, $I_B = -0.02 \text{ A}$)	V _{CE(sat)}	- - -	- - -	-0.10 -0.15 -0.30	V	
Base – Emitter Saturation Voltage (Note 7) (I _C = -1.0 A, I _B = -0.01 A)	V _{BE(sat)}	_	-0.68	-0.85	V	
Base – Emitter Turn–on Voltage (Note 7) (I _C = -2.0 A, V _{CE} = -3.0 V)	V _{BE(on)}	_	-0.81	-0.875	V	
Cutoff Frequency (I _C = -100 mA, V _{CE} = -5.0 V, f = 100 MHz)	f _T	100	-	-	MHz	
Input Capacitance (V _{EB} = -0.5 V, f = 1.0 MHz)	Cibo	-	600	650	pF	
Output Capacitance (V _{CB} = -3.0 V, f = 1.0 MHz)	Cobo	-	85	100	pF	
Turn-on Time (V _{CC} = -10 V, I _{B1} = -100 mA, I _C = -1 A, R _L = 3 Ω)	t _{on}	-	35	-	nS	
Turn-off Time (V _{CC} = -10 V, I _{B1} = I _{B2} = -100 mA, I _C = 1 A, R _L = 3 Ω)	t _{off}	-	225	_	nS	

^{7.} Pulsed Condition: Pulse Width = 300 μ sec, Duty Cycle \leq 2%

TYPICAL ELECTRICAL CHARACTERISTICS FOR P-CHANNEL FET

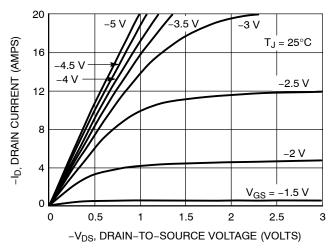


Figure 1. On-Region Characteristics

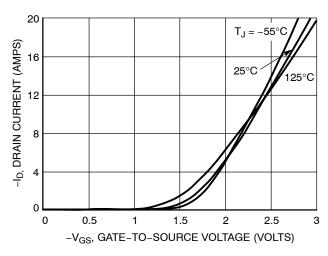


Figure 2. Transfer Characteristics

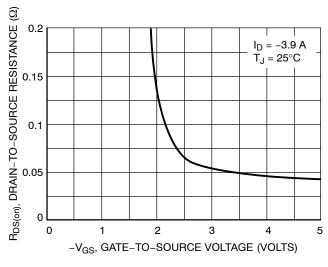


Figure 3. On-Resistance versus Gate-to-Source Voltage

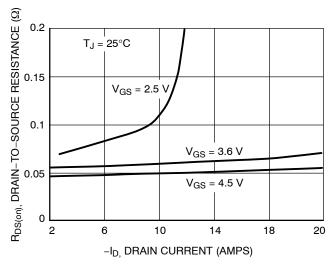


Figure 4. On-Resistance versus Drain Current and Gate Voltage

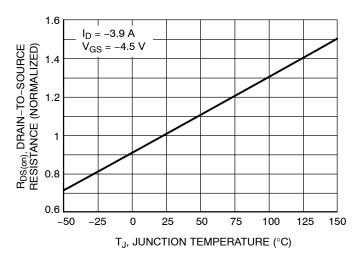


Figure 5. On–Resistance Variation with Temperature

TYPICAL ELECTRICAL CHARACTERISTICS FOR P-CHANNEL FET

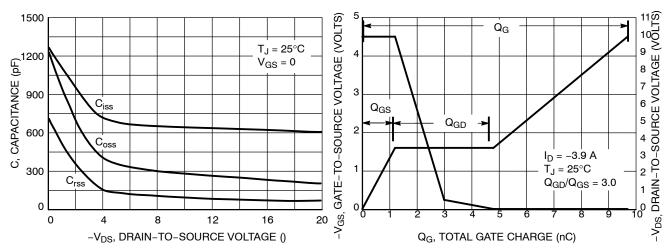


Figure 6. Capacitance Variation

Figure 7. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

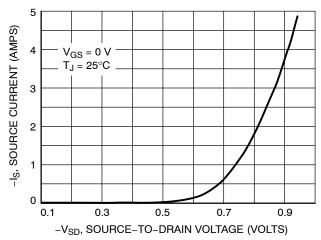


Figure 8. Diode Forward Voltage versus Current

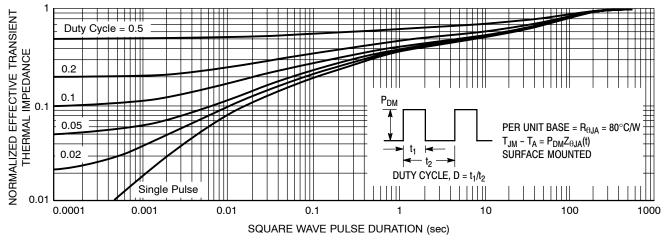


Figure 9. Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL ELECTRICAL CHARACTERISTICS FOR PNP TRANSISTOR

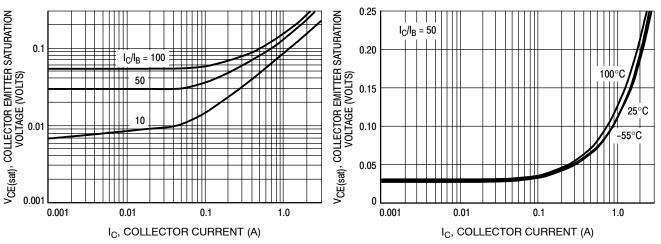


Figure 10. Collector Emitter Saturation Voltage versus Collector Current

Figure 11. Collector Emitter Saturation Voltage versus Collector Current

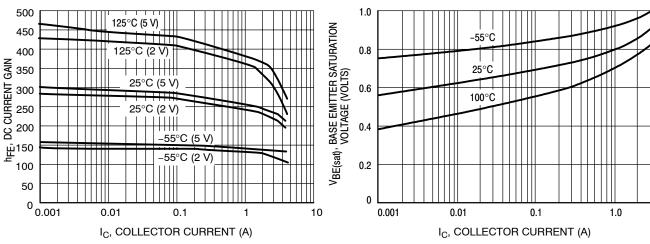


Figure 12. DC Current Gain versus Collector Current

100°C

25°C

-55°C

1.0

VBE(on), BASE EMITTER TURN-ON VOLTAGE (VOLTS)

1.0

0.9

0.8

0.7

0.6

0.5

0.001

0.01

Figure 13. Base Emitter Saturation Voltage

versus Collector Current

I_C, COLLECTOR CURRENT (A)

Figure 14. Base Emitter Turn-On Voltage versus Collector Current

0.1

Figure 15. Input Capacitance

TYPICAL ELECTRICAL CHARACTERISTICS FOR PNP TRANSISTOR

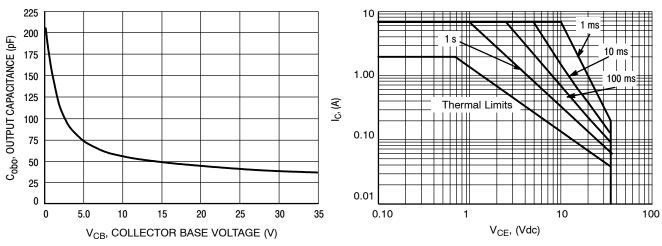


Figure 16. Output Capacitance

Figure 17. Safe Operating Area

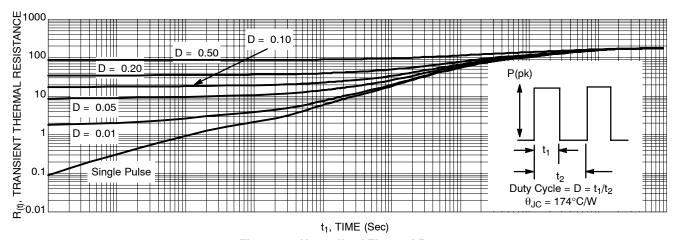
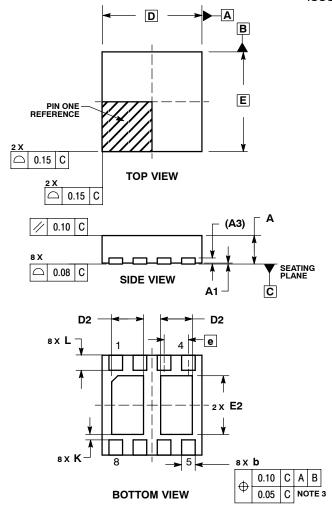


Figure 18. Normalized Thermal Response

PACKAGE DIMENSIONS

DFN8CASE 506AL-01 ISSUE A

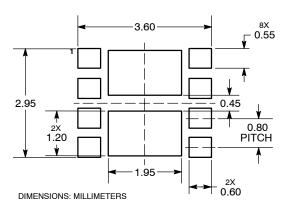


NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS. 3. DIMENSION 6 APPLIES TO PLATED TERMINAL
- DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm.
- COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS					
DIM	MIN	NOM	MAX			
Α	0.80	0.90	1.00			
A1	0.00	0.03	0.05			
А3		0.20 RE	F			
b	0.35	0.40	0.45			
D		3.30 BS	C			
D2	0.95	1.05	1.15			
Е		3.30 BS	Ö			
E2	1.80	1.90	2.00			
е	0.80 BSC					
K	0.21					
L	0.30	0.40	0.50			

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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