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NUS6189MN

Low Profile Overvoltage Protection IC with Integrated MOSFET

This device represents a new level of safety and integration by combining an overvoltage protection circuit (OVP) with a 30 V P−channel power MOSFET, a low $V_{CE(SAT)}$ transistor, and low $R_{DS(on)}$ power MOSFET or charging. The OVP is specifically designed to protect sensitive electronic circuitry from overvoltage transients and power supply faults. During such events, the IC quickly disconnects the input supply from the load, thus protecting it. The integration of the additional transistor and power MOSFET reduces layout space and promotes better charging performance.

The IC is optimized for applications that use an external AC−DC adapter or a car accessory charger to power a portable product or recharge its internal batteries.

Features

- Overvoltage Turn−Off Time of Less Than 1.0 μs
- Accurate Voltage Threshold of 6.85 V, Nominal
- Undervoltage Lockout Protection; 2.8 V, Nominal
- High Accuracy Undervoltage Threshold of 2.0%
- −30 V Integrated P−Channel Power MOSFET
- Low $R_{DS(on)}$ = 50 mΩ @ −4.5 V
- High Performance −12 V P−Channel Power MOSFET
- Single−Low $V_{ce(sat)}$ Transistors as Charging Power Mux
- Compact 3.0 x 4.0 mm QFN Package
- Maximum Solder Reflow Temperature @ 260°C
- This is a Pb−Free Device

Benefits

- Provide Battery Protection
- Integrated Solution Offers Cost and Space Savings
- Integrated Solution Improves System Reliability
- Optimized for Commercial PMUs from Top Suppliers

Applications

- Portable Computers and PDAs
- Cell Phones and Handheld Products
- Digital Cameras

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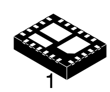
MARKING DIAGRAM



QFN22
CASE 485AT

NUS
6189
ALYW▪
▪

NUS6189	=	Specific Device Code
A	=	Assembly Location
L	=	Wafer Lot
Y	=	Year
W	=	Work Week
▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NUS6189MNTWG	QFN22 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

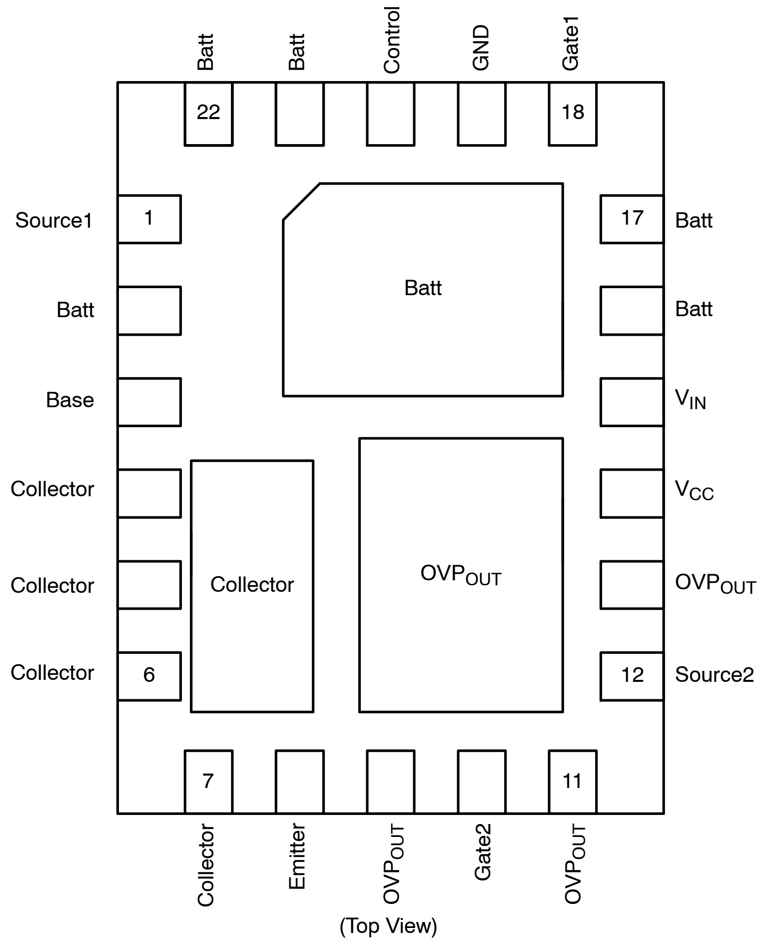


Figure 1. Pinout

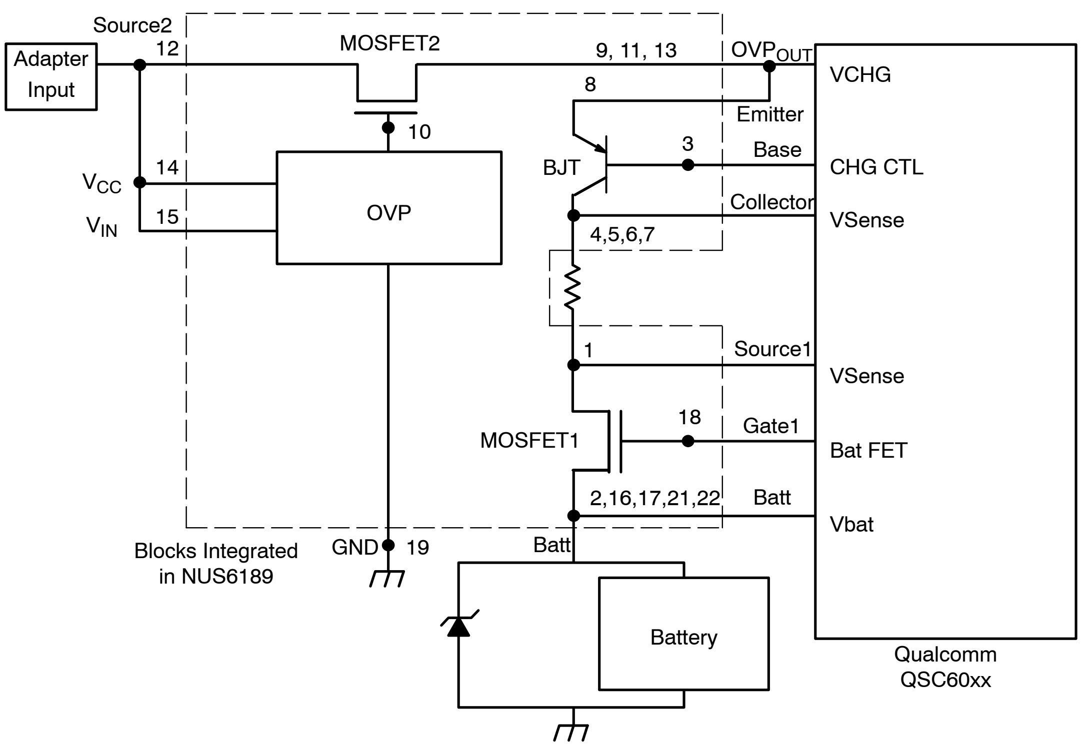


Figure 2. Typical Charging Solution for Qualcomm QSC60xx

FUNCTIONAL PIN DESCRIPTIONS

Pin	Function	Description
1	Source 1	This pin is the source of MOSFET1 and connects to the more negative Vsense pin of the PMIC and to the more negative side of the current sense resistor.
2, 16, 17, 21, 22	Batt	These pins are the drain of MOSFET2 and connect to the battery and the Vbat pin of the PMIC.
3	Base	The base of the internal bipolar transistor is connected to this pin. It connects to the Charge Control pin of the PMIC.
4, 5, 6, 7	Collector	The collector of the internal bipolar transistor connects to these pins and should be connected to the more positive side of the current sense resistor as well as the more positive Vsense pin of the PMIC.
8	Emitter	This pin is connected to the emitter of the bipolar transistor. It should be connected externally to the OVP_{OUT} pins.
9, 11, 13	OVP_{OUT}	These pins are the output of the OVP circuit. Internally they connect to the drain of MOSFET2. These pins connect externally to the Vcharge pin of the PMIC.
10	Gate2	This pin is the gate of MOSFET2. It is not normally connected to external circuitry.
12	Source 2	The source of the OVP FET is connected to this pin. This pin needs to be connected to pins 14 & 15.
14	V_{CC}	This pin is the V_{CC} pin of the OVP chip. It needs to be connected to pins 12 and 15.
15	V_{IN}	This pin senses the output voltage of the charger. If the voltage on this input rises above the over-voltage threshold (V_{TH}), the OVP_{OUT} pin will be driven to within 1.0 V of V_{IN}, thus disconnecting the FET. The nominal threshold level is 6.85 V. This pin needs to be connected to pins 12 and 14.
18	Gate1	This pin is the gate of MOSFET1. It connects to the Bat FET pin of the PMIC.
19	Gnd	This is the ground reference pin for the OVP chip.
20	Control	This logic signal is used to control the state of OVP_{OUT} and turn−on/off the P−channel MOSFET. A logic level high results in the OVP_{OUT} signal being driven to within 1.0 V of VCC which turns off MOSFET2. If this pin is not used, it should be connected to ground.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{IN} to Ground	V_{IN}	-0.3 to 30	V
Gate2 Voltage to Ground	V_{G2}	-0.3 to 30	V
Control Pin to Ground	V_{CNTRL}	-0.3 to 13	V
Shunt Voltage (OVP_{OUT} to Batt)	V_{shunt}	12	V
Maximum Power Dissipation (T_A = 50°C, Notes 1 & 3)	P_D	1.2	W
Thermal Resistance, Junction-to-Air (Note 1) Average θ for chip, minimum copper Maximum θ for power device, minimum copper Average θ, for chip (Note 2) Maximum θ for power device (Note 1) Average θ for chip (Note 1) Maximum θ for power device (Note 1)	$\theta_{J\text{-}A}$	 137 145 98 103 77 82	°C/W
Operating Case Temperature (Note 4)	T_{Cmax}	125	°C
Operating Ambient Temperature (P_D = 0.5 W, Note 1)	T_{Amb}	109	°C
Operating Junction Temperature (All Dice)	T_{Jmax}	150	°C
Thermal Resistance Junction−to−Case (Note 4)	Ψ_{JC}	30	°C/W
Storage Temperature Range	T_{stg}	-65 to 150	°C
Continuous Input Current (T_A = 50°C, Notes 1 & 3)	I_{max}	2.6	A
Gate-to-Source Voltage MOSFET1	V_{GS1}	±8.0	V
Drain-to-Source Voltage MOSFET1	V_{DS1}	−12	V
Drain-to-Source Voltage MOSFET2	V_{DS2}	−30	V
Collector-Emitter Voltage BJT	V_{CEO}	−20	V
Collector-Base Voltage BJT	V_{CBO}	−20	V
Emitter-Base Voltage BJT	V_{EBO}	−7.0	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface−mounted on FR4 board using 1 inch sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface−mounted on FR4 board using 0.25 inch sq pad size (Cu area = 0.37 in sq [1 oz] including traces).
3. V_{IN} = 6.0 V, all power devices fully enhanced.
4. Surface−mounted on FR4 board using 400 mm sq pad size, 4 oz Cu, P_D < 800 mW.

ELECTRICAL CHARACTERISTICS (T_J = 25°C, CNTRL ≤ 1.5 V, V_{CC} = 6.0 V, unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
OVP THRESHOLD					
Input Threshold (V_{IN} Increasing)	V_{th}	6.65	6.85	7.08	V
Input Hysteresis (V_{IN} Decreasing)	V_{hyst}	50	150	200	mV
Input Impedance (V_{IN} = V_{th})	R_{IN}	70	150	–	kΩ
CONTROL INPUT					
Control Voltage High (Output On)	$V_{cntrlHI}$	1.50	–	–	V
Control Voltage Low (Output Off)	$V_{cntrlLO}$	–	–	0.50	V
Control Current High (V_{ih} = 5.0 V)	I_{ih}	–	95	200	μA
Control Current Low (V_{il} = 0.5 V)	I_{il}	–	10	–	μA
OVP GATE DRIVE VOLTAGE					
Gate2 Voltage High (V_{IN} = 8.0 V; I_{Source} = 10 mA) Gate2 Voltage High (V_{IN} = 8.0 V; I_{Source} = 0.25 mA) Gate2 Voltage High (V_{IN} = 8.0 V; I_{Source} = 0 mA)	V_{oh}	V_{IN} – 1.0 V_{IN} – 0.25 V_{IN} – 0.1	– – –	– – –	V
Gate2 Voltage Low (V_{IN} = 6.0 V; I_{Sink} = 0 mA, Control = 0 V)	V_{ol}	–	–	0.10	V
Gate2 Sink Current (V_{IN} < V_{Th}, OVP_{OUT} = 1.0 V, Note 5)	I_{Sink}	10	33	50	μA
TIMING					
Turn on Delay – Input (V_{IN} stepped down from 8 to 6 V; measured at 50% point of OVP_{OUT}, Note 5)	t_{on_IN}	–	–	10	μs
Turn off Delay – Input (V_{IN} stepped up from 6.0 to 8.0 V; C_L = 12 nF Output > V_{IN} – 1.0 V)	t_{off_IN}	–	0.5	1.0	μs
Turn on Delay – Control (Control signal stepped down from 2.0 to 0.5 V; measured to 50% point of OVP_{OUT}, Note 5)	t_{on_CT}	–	–	10	μs
Turn off Delay – Control (Control signal stepped up from 0.5 to 2.0 V; C_L = 12 nF Output > V_{IN} –1.0 V)	t_{off_CT}	–	1.0	2.0	μs
TOTAL DEVICE					
V_{IN} Operating Voltage Range (Note 5)	V_{IN}	3.0	4.8	25	V
Input Bias Current	I_{Bias}	–	0.75	1.0	mA
Undervoltage Lockout (V_{IN} Decreasing)	V_{Lock}	2.5	2.8	3.0	V
OVP FET (MOSFET2) (T_J = 25°C, V_{CC} = 6.0 V, unless otherwise specified)					
Voltage Drop (V_{IN} to OVP_{OUT}, V_{GS} = -4.5 V) I_{Load} = 0.6 A I_{Load} = 1.0 A I_{Load} = 1.0 A, T_J = 150°C (Note 5)	V_{OVP}	 – – –	 33 66 90	 54 100 135	mV
On Resistance I_{Load} = 0.6 A I_{Load} = 1.0 A I_{Load} = 1.0 A, T_J = 150°C (Note 5)	$R_{DS(on)}$	 – – –	 50 52 90	 90 100 135	mΩ
Off State Leakage Current T_J = 125°C	I_{Leak}	– –	-0.1 –	-1.0 -100	μA
CHARGING BJT (T_J = 25°C, unless otherwise specified)					
Collector-Emitter Cutoff Current (V_{CES} = -20 V, Note 5)	I_{CES}	–	–	-0.1	μA
DC Current Gain (I_B = -2.0 mA, V_{CE} = -2.0 V, Note 6)	h_{fe}	180	–	–	–
Collector-Emitter Saturation Voltage I_C = -1.0 A, I_B = -0.01 A I_C = -1.0 A, I_B = -0.1 A	$V_{CE(sat)}$	 – –	 -0.10 -0.069	 -0.12 -0.09	V

ELECTRICAL CHARACTERISTICS (T_J = 25°C, CNTRL ≤ 1.5 V, V_{CC} = 6.0 V, unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{EB} = -0.5 V, f = 1.0 MHz, Note 5)	C_{ibo}	–	240	400	pF
Output Capacitance (V_{CB} = -3.0 V, f = 1.0 MHz, Note 5)	C_{obo}	–	50	100	pF

CHARGING FET (MOSFET1) (T_J = 25°C, unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Voltage Drop Across FET V_{GS} = -4.5 V, I_{Load} = 1.0 A V_{GS} = -2.5 V, I_{Load} = 1.0 A V_{GS} = -4.5 V, I_{Load} = 1.0 A, T_J = 150°C (Note 5)	V_{DS}	 – – –	 32 44 62	 40 50 70	mV
On Resistance V_{GS} = -4.5 V, I_{Load} = 1.0 A V_{GS} = -2.5 V, I_{Load} = 1.0 A V_{GS} = -4.5 V, I_{Load} = 1.0 A, T_J = 150°C, (Note 5)	$R_{DS(on)}$	 – – –	 32 44 62	 40 50 70	mV
Off State Leakage Current (Note 5) T_J = 125°C	I_{Leak}	– –	−0.1 –	−1.0 −10	μA
Input Capacitance	C_{ISS}	–	1330	–	pF
Output Capacitance	C_{OSS}	–	200	–	pF
Reverse Transfer Capacitance	C_{RSS}	–	115	–	pF
Total Gate Charge (Note 5)	$Q_{G(TOT)}$	–	13	15.7	nC
Threshold Gate Charge	$Q_{G(TH)}$	–	1.5	–	nC
Gate-to-Source Charge	Q_{GS}	–	2.2	–	nC
Gate-to-Drain Charge	Q_{GD}	–	2.9	–	nC
Gate Resistance	R_G	–	14.4	–	Ω
Forward Transconductance (V_{DS} = -6 V, I_D = 1.0 A)	g_{fs}	–	0.9	–	S
Gate Threshold Voltage (V_{GS} = V_{DS}, I_D = -250 μA)	$V_{GS(th)}$	−0.45	−0.67	−1.1	V
Negative Threshold Temperature Coefficient	$V_{GS(th)}/T_J$	–	2.7	–	mV/°C

5. Guaranteed by design.
6. Pulsed Condition: Pulse Width = 300 us, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS − 12V, P−CHANNEL MOSFETS (MOSFET1 − CHARGING)

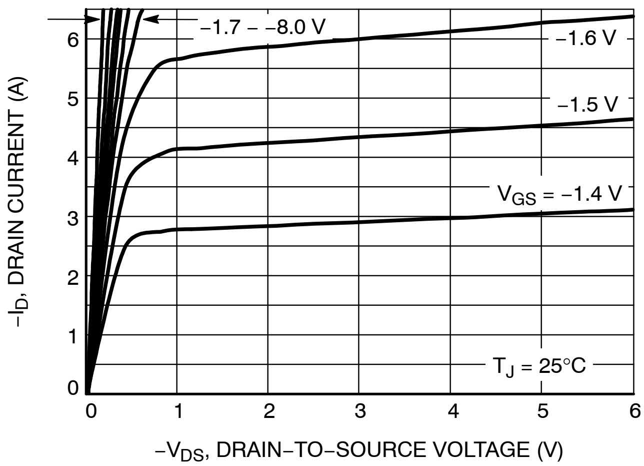


Figure 3. On−Region Characteristics

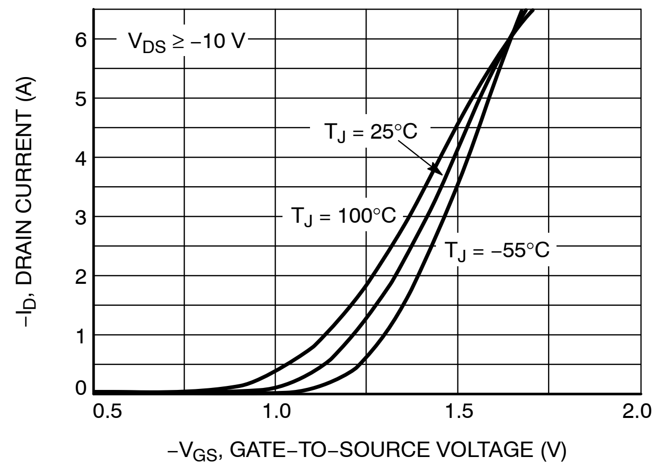


Figure 4. Transfer Characteristics

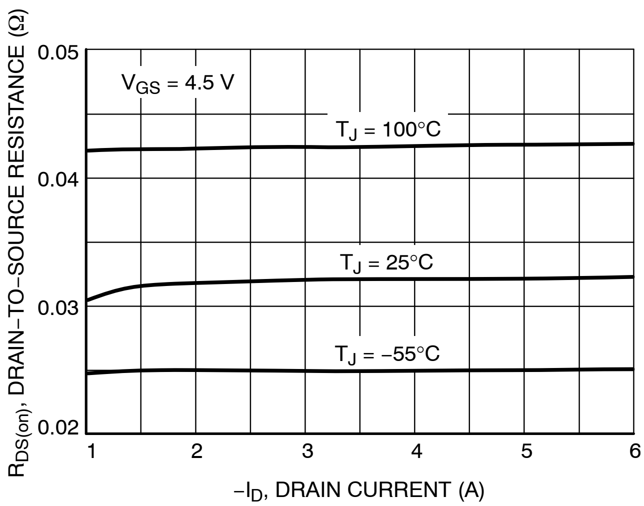


Figure 5. On−Resistance vs. Drain Current

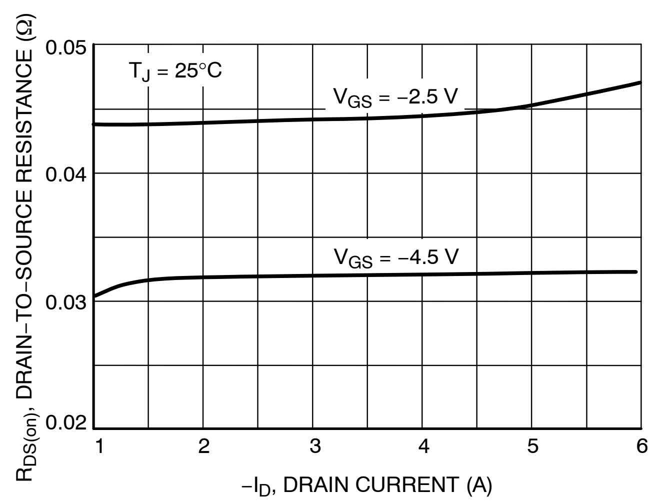


Figure 6. On−Resistance vs. Drain Current and Gate Voltage

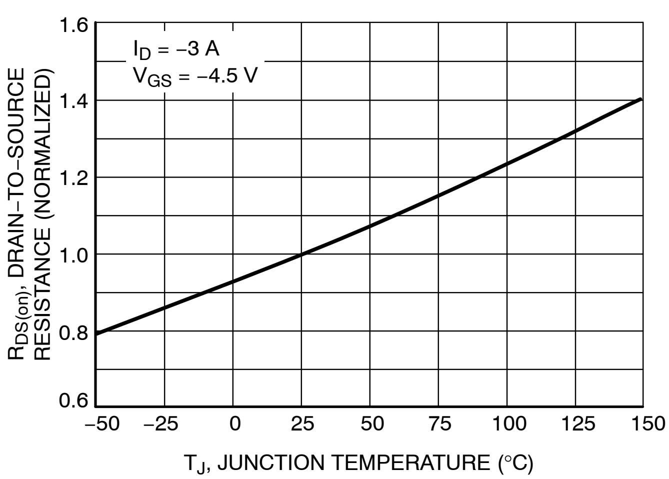


Figure 7. On−Resistance Variation with Temperature

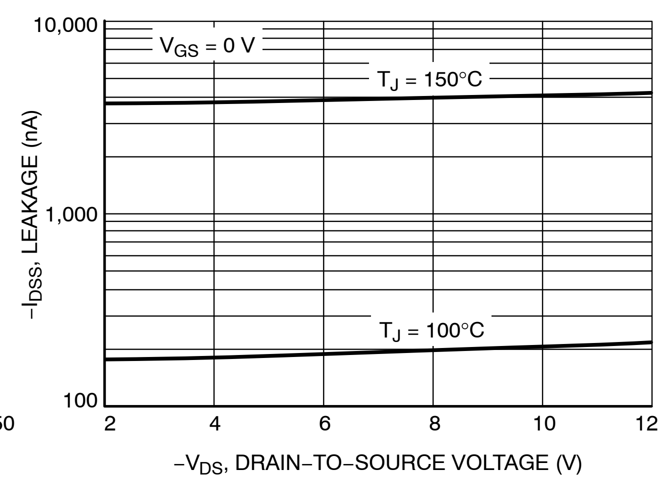


Figure 8. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS – 12V, P–CHANNEL MOSFETS (MOSFET1 – CHARGING)

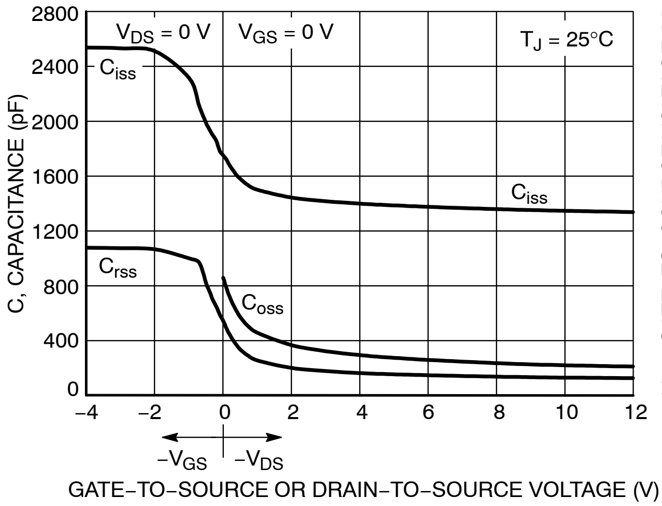


Figure 9. Capacitance Variation

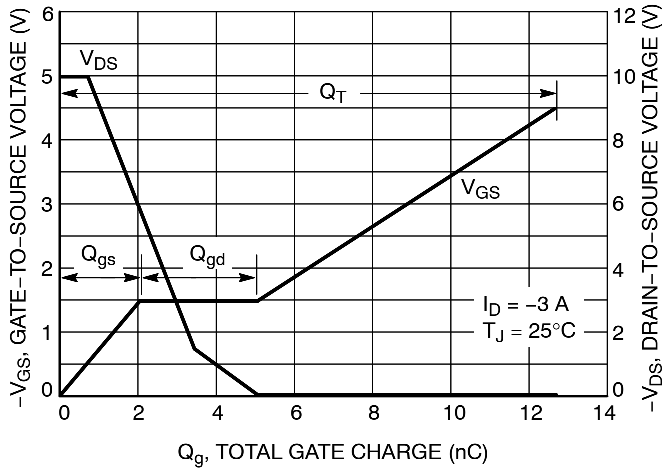


Figure 10. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge

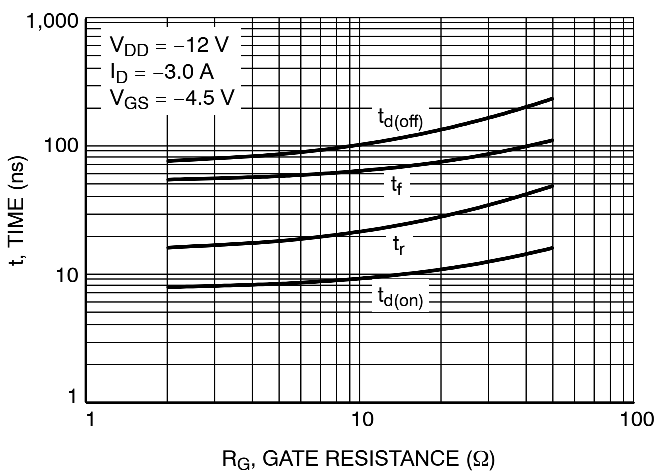


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

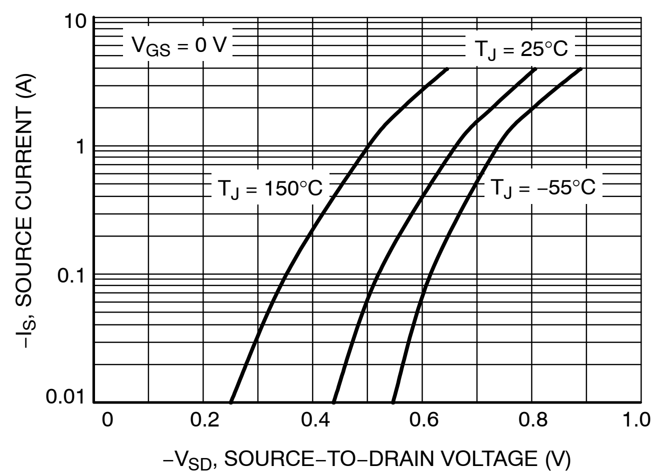
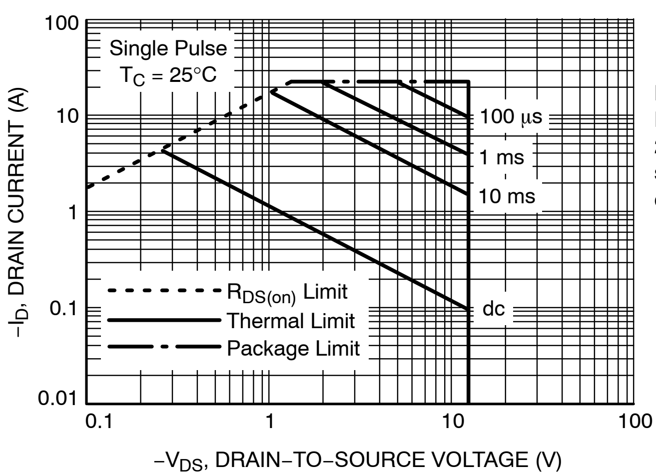


Figure 12. Diode Forward Voltage vs. Current



Mounted on 2″ sq. FR4 board (0.5″ sq. 2 oz. Cu single sided) with MOSFET die operating.

Figure 13. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS – 12V, P−CHANNEL MOSFETS (MOSFET1 – CHARGING)

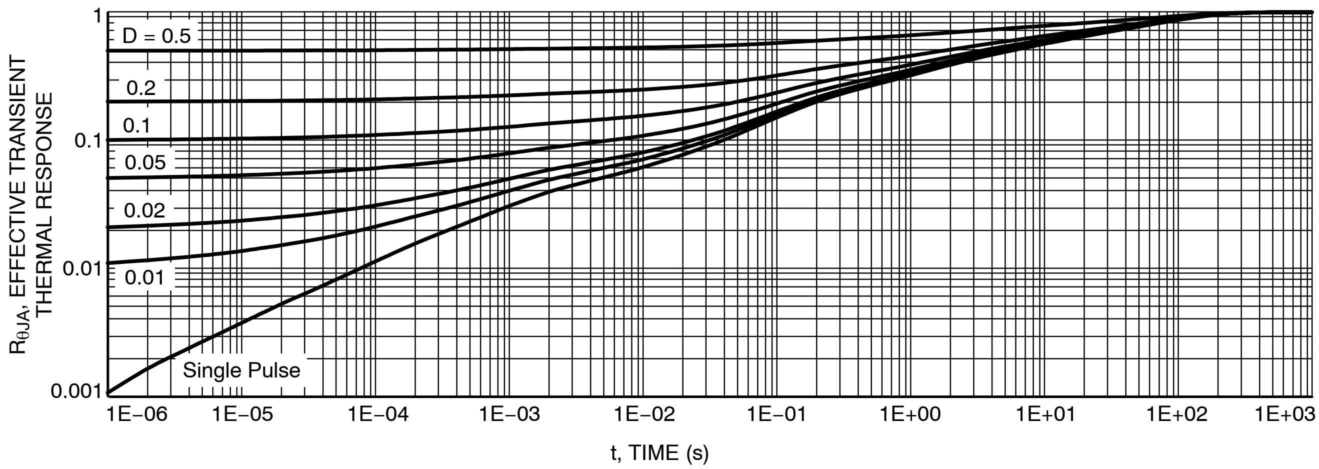


Figure 14. FET Thermal Response

TYPICAL CHARACTERISTICS − SINGLE PNP TRANSISTOR (BJT − CHARGING)

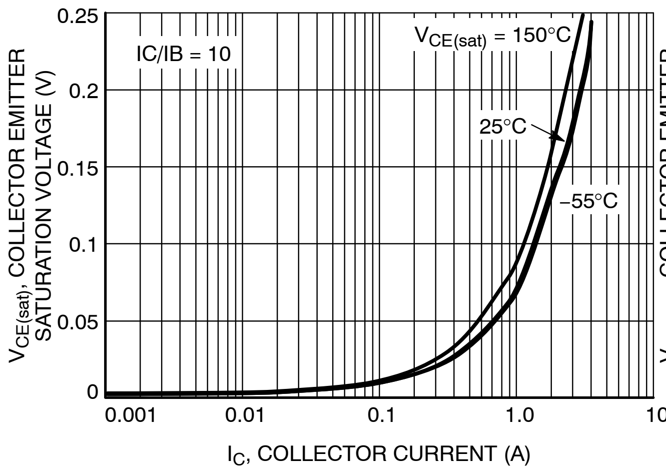


Figure 15. Collector Emitter Saturation Voltage vs. Collector Current

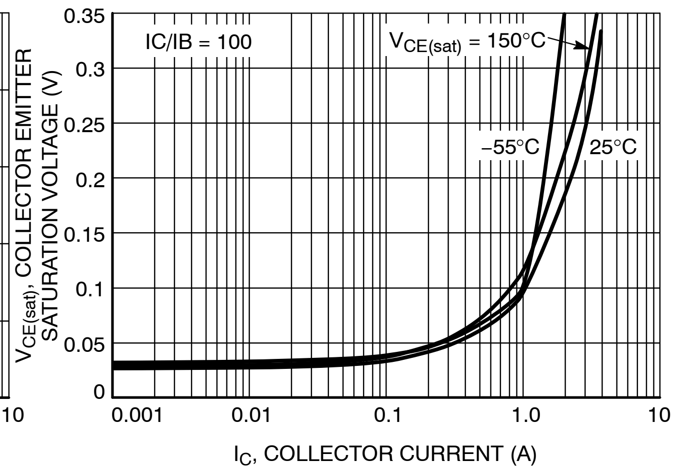


Figure 16. Collector Emitter Saturation Voltage vs. Collector Current

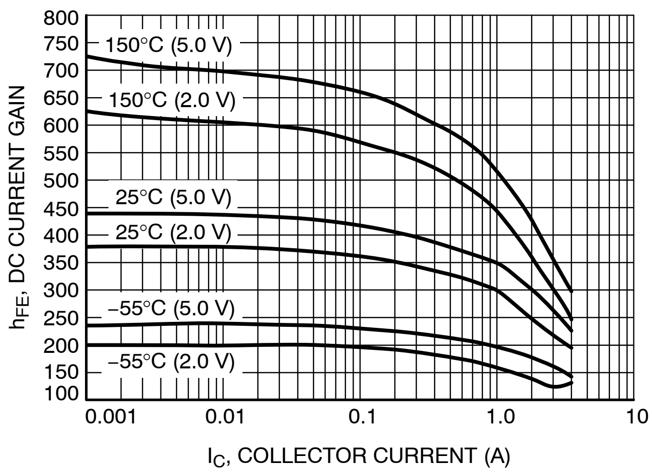


Figure 17. DC Current Gain vs. Collector Current

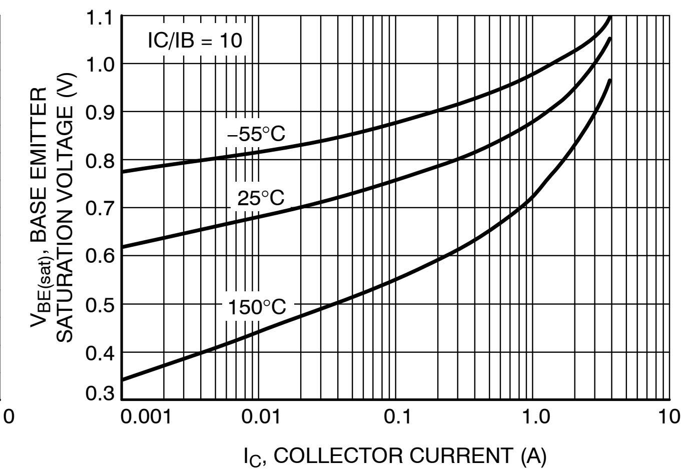


Figure 18. Base Emitter Saturation Voltage vs. Collector Current

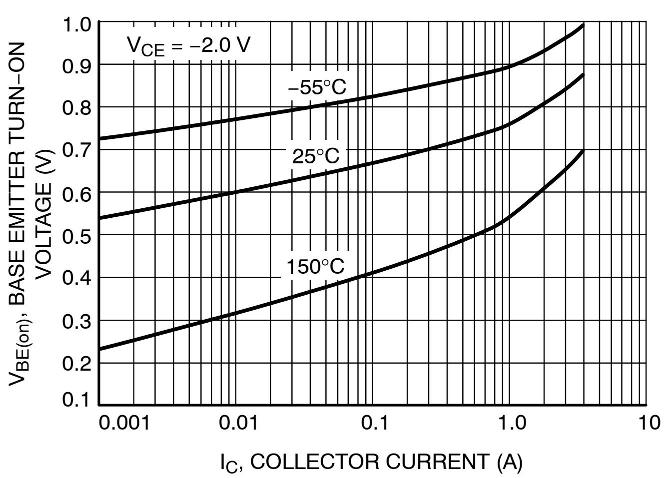


Figure 19. Base Emitter Turn−On Voltage vs. Collector Current

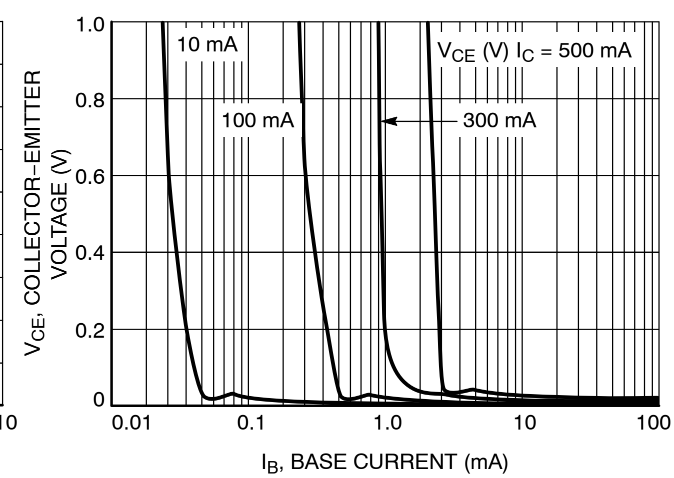


Figure 20. Saturation Region

TYPICAL CHARACTERISTICS – SINGLE PNP TRANSISTOR (BJT – CHARGING)

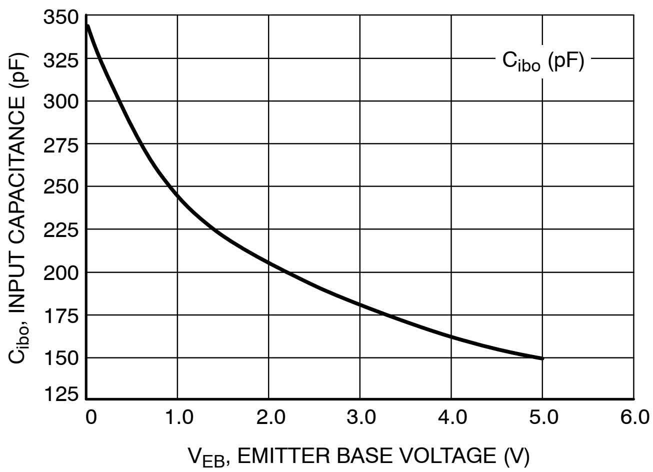


Figure 21. Input Capacitance

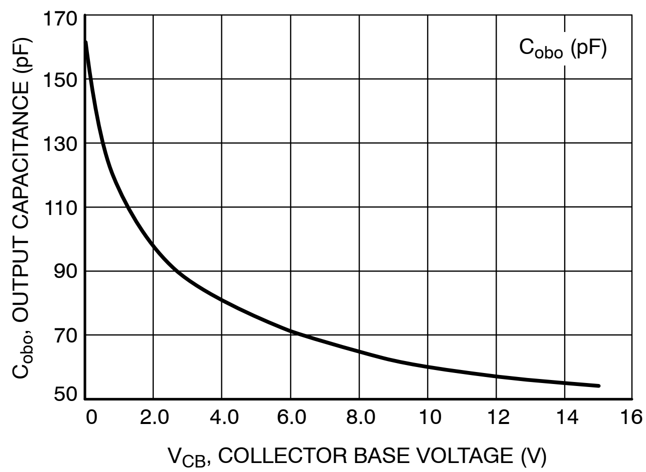


Figure 22. Output Capacitance

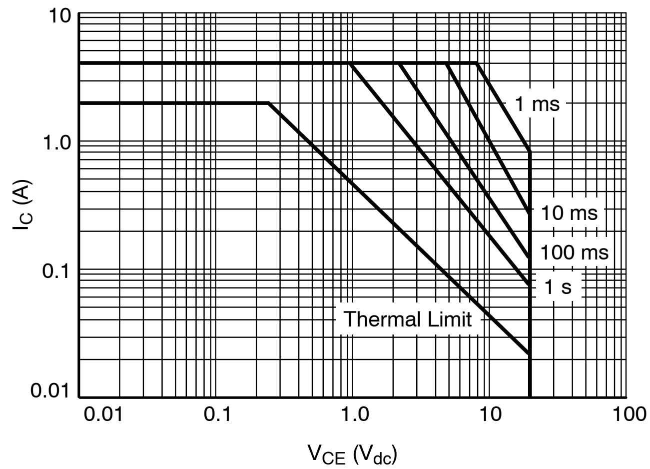


Figure 23. Safe Operating Area

TYPICAL PERFORMANCE CURVES – OVERVOLTAGE PROTECTION IC

(T_A= 25°C, unless otherwise specified)

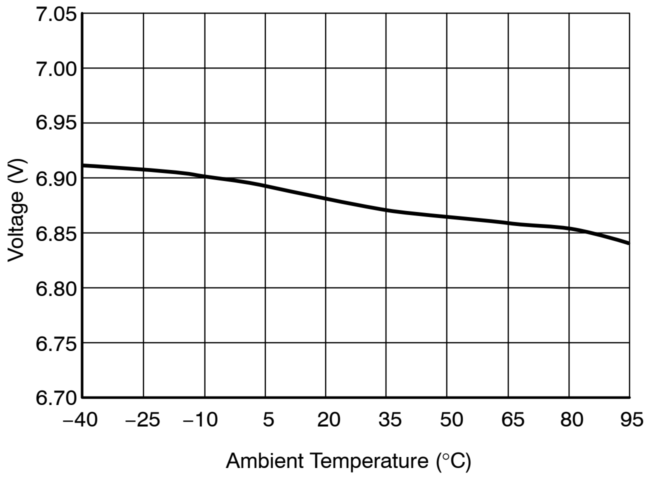


Figure 24. Typical V_{th} Threshold Variation vs. Temperature

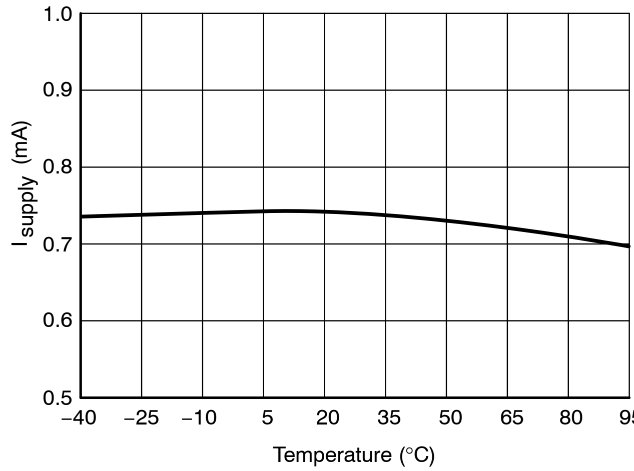


Figure 25. Typical Supply Current vs. Temperature $I_{cc} + I_{in}$, $V_{CC} = 6$ V

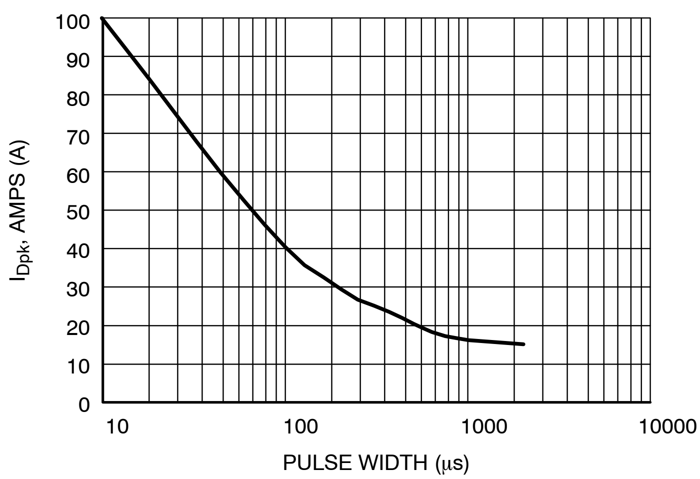


Figure 26. Typical Maximum Drain Peak Current vs Pulse Width (Non−repetitive Single Pulse, V_{GS} = 10 V, T_A = 25°C)

TYPICAL PERFORMANCE CURVES − 30V, P−CHANNEL MOSFET (MOSFET2 − OVP)

(T_A= 25°C, unless otherwise specified)

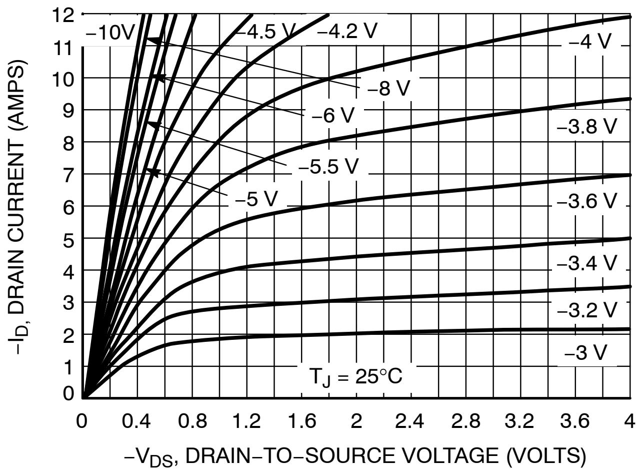


Figure 27. On−Region Characteristics

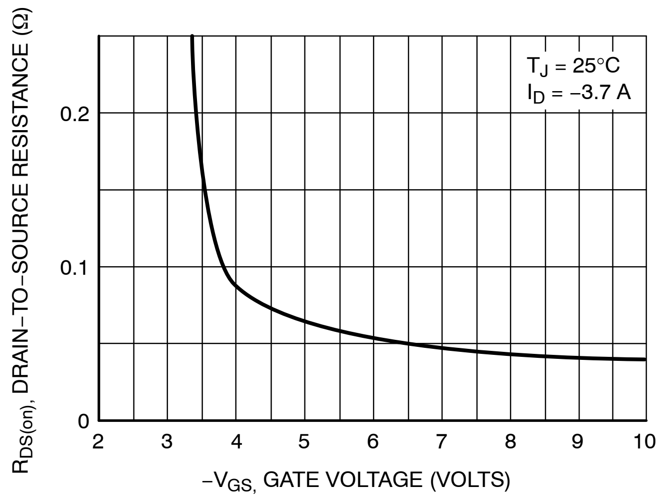


Figure 28. On−Resistance vs. Gate−to−Source Voltage

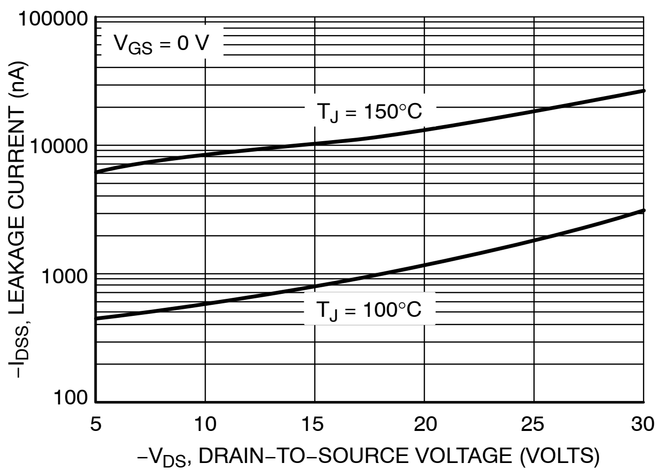


Figure 29. Drain−to−Source Leakage Current vs. Voltage

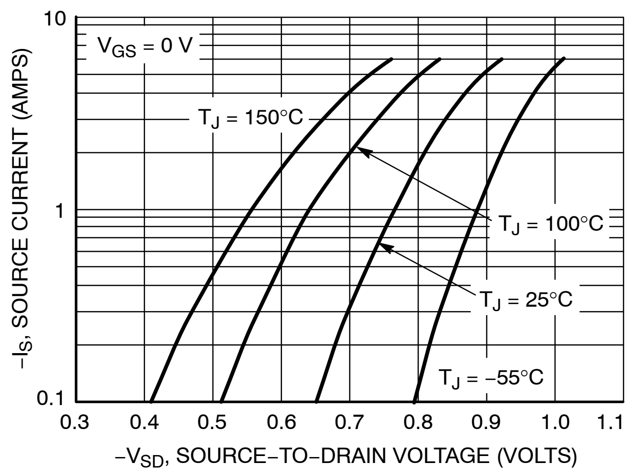
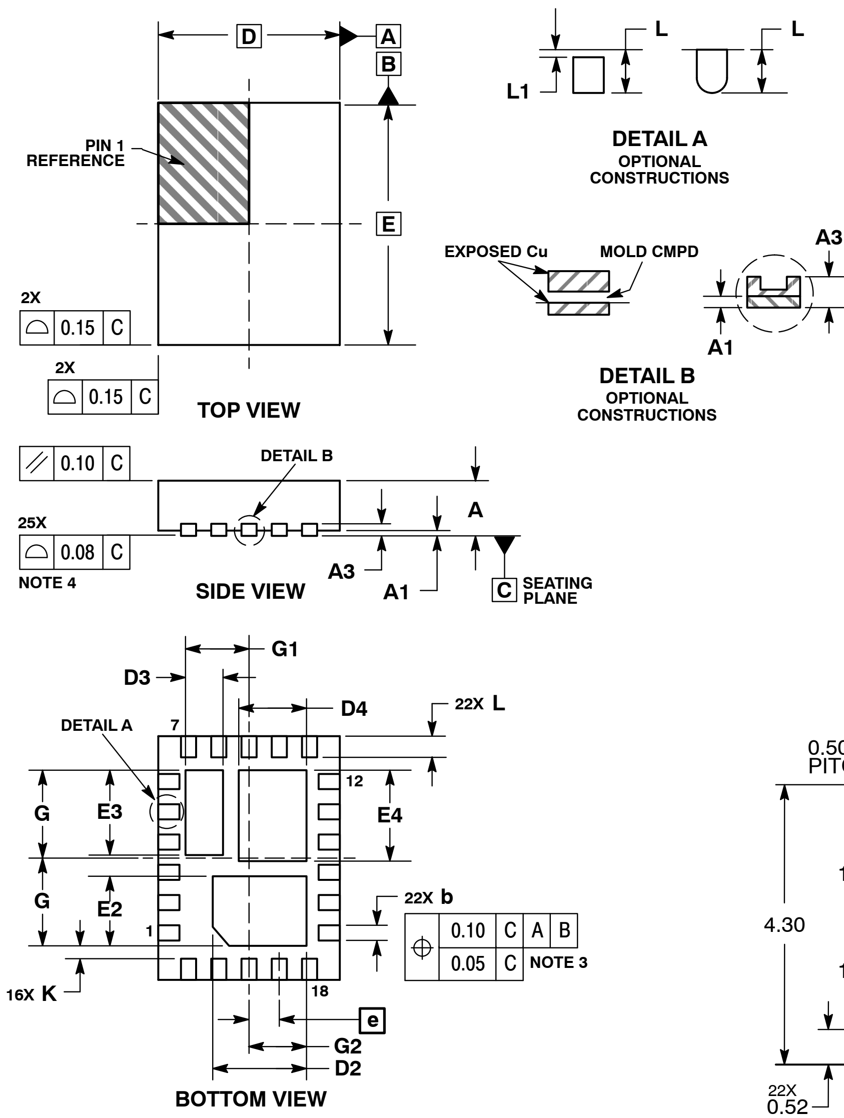


Figure 30. Diode Forward Voltage vs. Current

PACKAGE DIMENSIONS

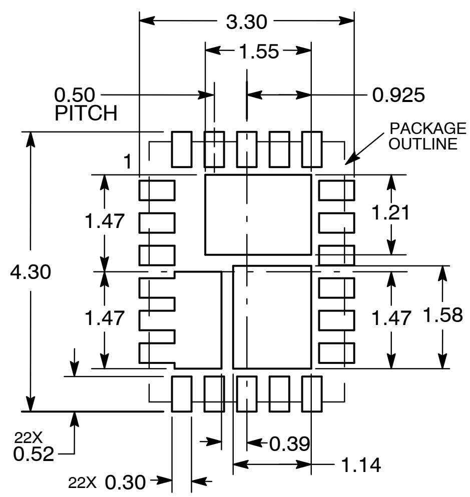
QFN22, 3x4, 0.5P
CASE 485AT−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.025	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
D	3.00 BSC		
D2	1.45	1.50	1.55
D3	0.52	0.57	0.62
D4	1.02	1.07	1.12
E	4.00 BSC		
E2	1.05	1.10	1.15
E3	1.30	1.35	1.40
E4	1.40	1.45	1.50
e	0.50 BSC		
K	0.25	---	---
L	0.30	0.325	0.35
L1	---	---	0.15
G	1.35	1.40	1.50
G1	0.95	1.05	1.15
G2	0.855	0.885	0.915

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

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