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ARM[®] Cortex[®]-M0
32-bit Microcontroller

NuMicro[®] Family
Mini58DE Series
Datasheet

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1 GENERAL DESCRIPTION

The NuMicro® Mini58 series is pin-to-pin and function compatible with the NuMicro® Mini51 series, the 32-bit microcontroller (MCU) embedded with the ARM® Cortex®-M0 core. The Mini58 series can bridge the gap and replace the cost equivalent to traditional 8- and 16-bit microcontroller by 32-bit performance and rich functions. The Mini58 series supports a wide range of applications from low-end, price sensitive designs to computing-intensive ones and provides advanced high-end features in economical products.

The Mini58 series can run up to 50 MHz which is faster than 24 MHz in Mini51 series, and operate at a wide voltage range of 2.5V ~ 5.5V and temperature range of -40°C ~ +105°C. For the Mini58 series, the embedded program flash size upgrades from 16 Kbytes to 32 Kbytes and SRAM upgrades from 2 Kbytes to 4 Kbytes. The Mini58 series also offers size configurable Data Flash (shared with program flash), and 2.5 Kbytes flash for the ISP.

The Mini58 series has many high-performance peripheral functions, such as 22.1184 MHz internal RC oscillator ($\pm 1\%$ accuracy), I/O port with up to 30 pins, four 32-bit timers, two UARTs with the RS485 function and IrDA function interface, one SPI interface, two I²C interfaces, up to three 16-bit PWM generators providing six channels, an 8-channel 10-bit ADC, Watchdog Timer, Window Watchdog Timer, two Analog Comparators and a Brown-out Detector. All these peripherals have been incorporated into the Mini58 series to reduce component count, board space and system cost. Compared to the Mini51 series, the Mini58 series supports additional one UART and one I²C interface for better and more flexible connectivity applications.

Additionally, the Mini58 series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product. The Mini58 series also supports In-Application-Programming (IAP) function, user switches the code executing without the chip reset after the embedded flash updated.

2 FEATURES

- Core
 - ARM® Cortex®-M0 core running up to 50 MHz
 - One 24-bit system timer
 - Supports low power Idle mode
 - A single-cycle 32-bit hardware multiplier
 - NVIC for the 32 interrupt inputs, each with 4-level of priority
 - Supports Serial Wire Debug (SWD) interface and two watchpoints/four breakpoints
- Built-in LDO for wide operating voltage: 2.5V to 5.5V
- Memory
 - 32 KB Flash memory for program memory (APROM)
 - Configurable Flash memory for data memory (Data Flash)
 - 2.5 KB Flash for loader (LDROM)
 - 4 KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
 - Programmable system clock source
 - ◆ Switch clock sources on-the-fly
 - Support 4 ~ 24 MHz external high speed crystal oscillator (HXT) for precise timing operation
 - Support 32.768 kHz external low speed crystal oscillator (LXT) for idle wake-up and system operation clock
 - Built-in 22.1184 MHz internal high speed RC oscillator (HIRC) for system operation (1% accuracy at 25°C, 5V)
 - ◆ Dynamically calibrating the HIRC OSC to 22.1184 MHz ±1% from -40°C to 105°C by external 32.768K crystal oscillator (LXT)
 - Built-in 10 kHz internal low speed RC oscillator (LIRC) for Watchdog Timer and wake-up operation
 - PLL allowing CPU operation up to the maximum 50 MHz
- I/O Port
 - Up to 30 general-purpose I/O (GPIO) pins for LQFP-48 package
 - Four I/O modes:
 - ◆ Quasi-bidirectional input/output
 - ◆ Push-Pull output
 - ◆ Open-Drain output
 - ◆ Input only with high impedance
 - Optional Schmitt trigger input
- Timer
 - Provides two channel 32-bit Timers; one 8-bit pre-scaler counter with 24-bit up-timer for each timer

- ◆ Supports Event Counter mode
- ◆ Supports Toggle Output mode
- ◆ Supports external trigger in Pulse Width Measurement mode
- ◆ Supports external trigger in Pulse Width Capture mode
- WDT (Watchdog Timer)
 - Programmable clock source and time-out period
 - Supports wake-up function in Power-down mode and Idle mode
 - Interrupt or reset selectable on watchdog time-out
- WWDT (Window Watchdog Timer)
 - 6-bit down counter value (CNTDAT) and 6-bit compare value (CMPDAT) to make the WWDT time-out window period flexible
 - Supports 4-bit value (PSCSEL) to programmable maximum 11-bit prescale counter period of WWDT counter
- PWM
 - Up to three built-in 16-bit PWM generators, providing six PWM outputs or three complementary paired PWM outputs
 - Individual clock source, clock divider, 8-bit pre-scalar and dead-time generator for each PWM generator
 - PWM interrupt synchronized to PWM period
 - Supports edge-alignment or center-alignment
 - Supports fault detection
- UART (Universal Asynchronous Receiver/Transmitters)
 - Two UART devices
 - Buffered receiver and transmitter, each with 16-byte FIFO
 - Optional flow control function (CTS_n and RTS_n)
 - Supports IrDA (SIR) function
 - Programmable baud-rate generator up to 1/16 system clock
 - Supports RS-485 function
- SPI (Serial Peripheral Interface)
 - One SPI device
 - Master up to 25 MHz, and Slave up to 10 MHz
 - Supports Master/Slave mode
 - Full-duplex synchronous serial data transfer
 - Variable length of transfer data from 1 to 32 bits
 - MSB or LSB first data transfer
 - RX latching data can be either at rising edge or at falling edge of serial clock
 - TX sending data can be either at rising edge or at falling edge of serial clock
 - Supports Byte Suspend mode in 32-bit transmission
- I²C

- Two I²C devices
- Supports Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Programmable clocks allow for versatile rate control
- Supports multiple address recognition (four slave addresses with mask option)
- ADC (Analog-to-Digital Converter)
 - 10-bit SAR ADC with 250 kSPS
 - Up to 8-ch single-end input and one internal input from band-gap
 - Conversion started either by software trigger or external pin trigger
- Analog Comparator
 - Two analog comparators with programmable 16-level internal voltage reference
 - Built-in CRV (comparator reference voltage)
- ISP (In-System Programming), ICP (In-Circuit Programming), and IAP (In-Application-Programming) update
- BOD (Brown-out Detector)
 - With 4 programmable threshold levels: 4.4V/3.7V/2.7V/2.2V
 - Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
 - Threshold voltage level: 2.0V
- Operating Temperature: -40°C ~105°C
- Reliability: EFT > ± 4KV, ESD HBM pass 4KV
- Packages:
 - Green package (RoHS)
 - 48-pin LQFP (7x7), 33-pin QFN (5x5) , 33-pin QFN (4x4), 20-pin TSSOP

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
BOD	Brown-out Detection
DAP	Debug Access Port
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
ICP	In Circuit Programming
ISP	In System Programming
ISR	Interrupt Service Routine
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LXT	32.768 kHz External Low Speed Crystal Oscillator
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro® Mini58 Series Naming Rule

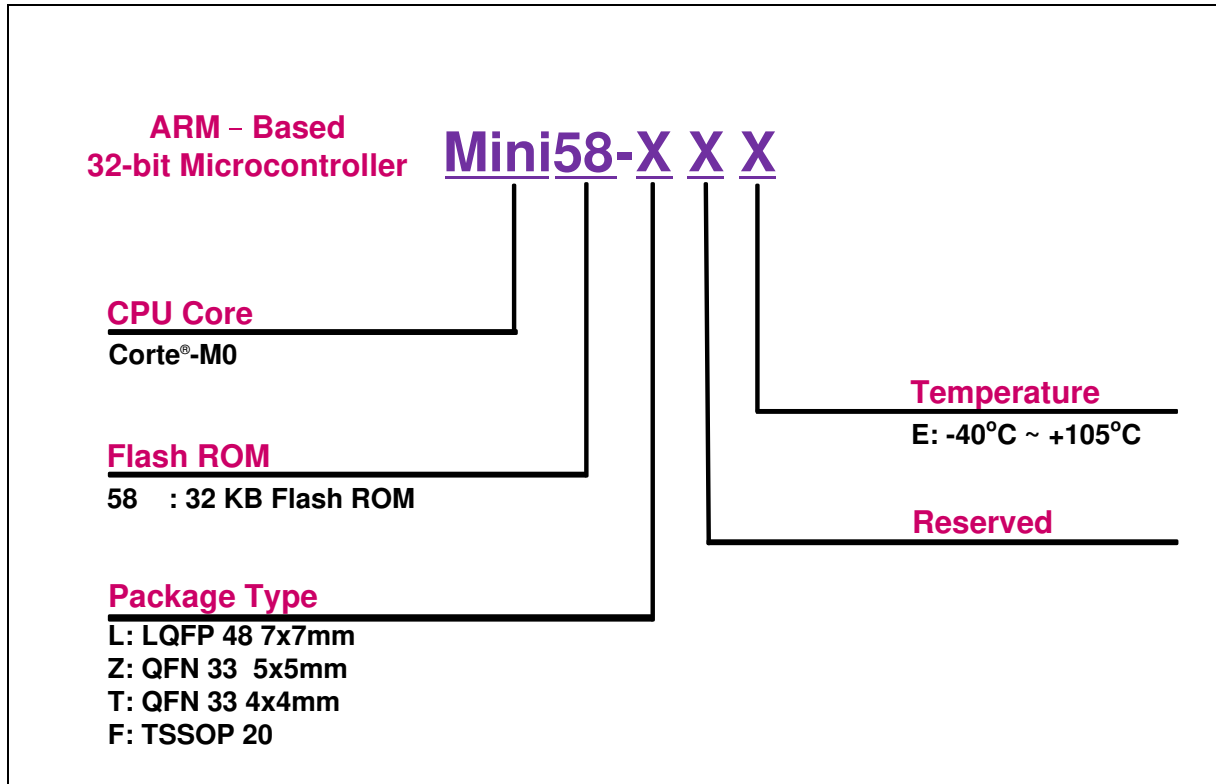


Figure 4.1-1 NuMicro® Mini58 Series Naming Rule

4.2 NuMicro® Mini58 Series Product Selection Guide

Part Number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity			Comp.	PWM	ADC	ISP ICP	IRC 22.1184 MHz	Package
							UART	SPI	I ² C						
MINI58LDE	32 KB	4 KB	Configurable	2.5 KB	up to 30	2x32-bit	2	1	2	2	6	8x10-bit	v	v	LQFP48
MINI58ZDE	32 KB	4 KB	Configurable	2.5 KB	up to 29	2x32-bit	2	1	2	2	6	8x10-bit	v	v	QFN33(5x5)
MINI58TDE	32 KB	4 KB	Configurable	2.5 KB	up to 29	2x32-bit	2	1	2	2	6	8x10-bit	v	v	QFN33(4x4)
MINI58FDE	32 KB	4 KB	Configurable	2.5 KB	up to 17	2x32-bit	2	1	2	-	6	4x10-bit	v	v	TSSOP20

Table 4.2-1 NuMicro® Mini58 Series Product Selection Guide

4.3 PIN CONFIGURATION

4.3.1 LQFP 48-pin

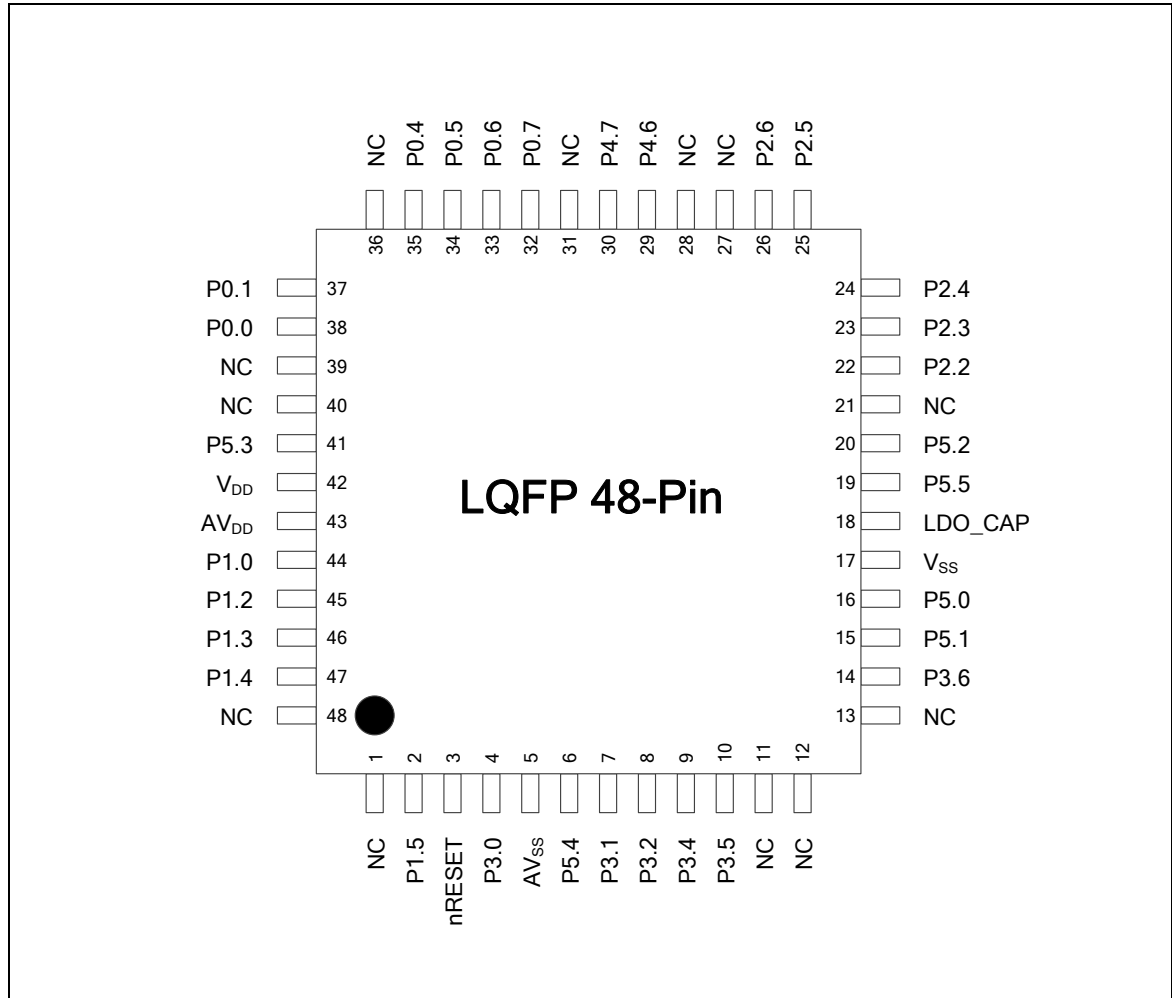


Figure 4.3-1 NuMicro® Mini58 Series LQFP 48-pin Diagram

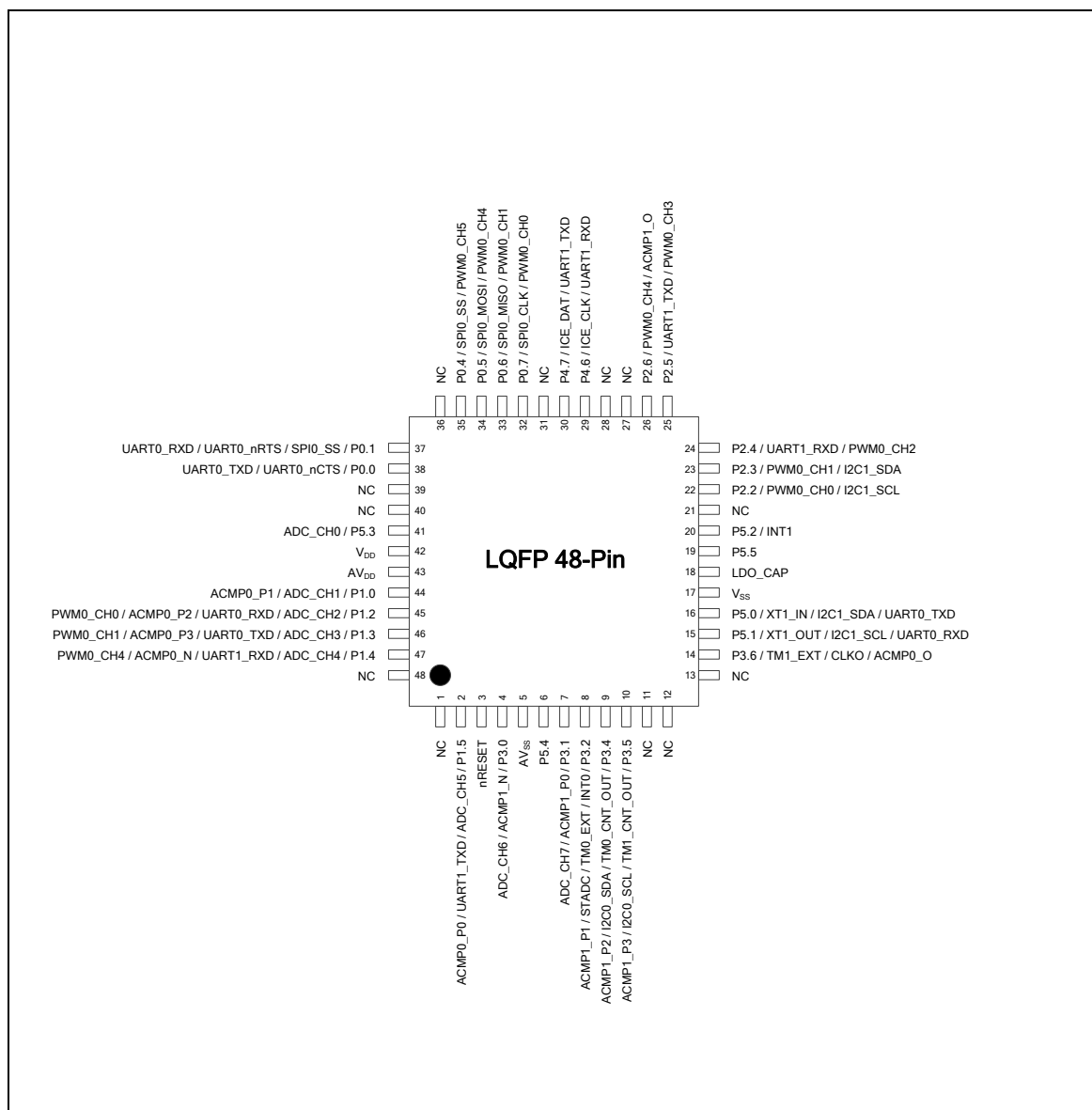


Figure 4.3-2 NuMicro® Mini58 Series LQFP 48-pin Multi-Function Diagram

4.3.2 QFN 33-pin

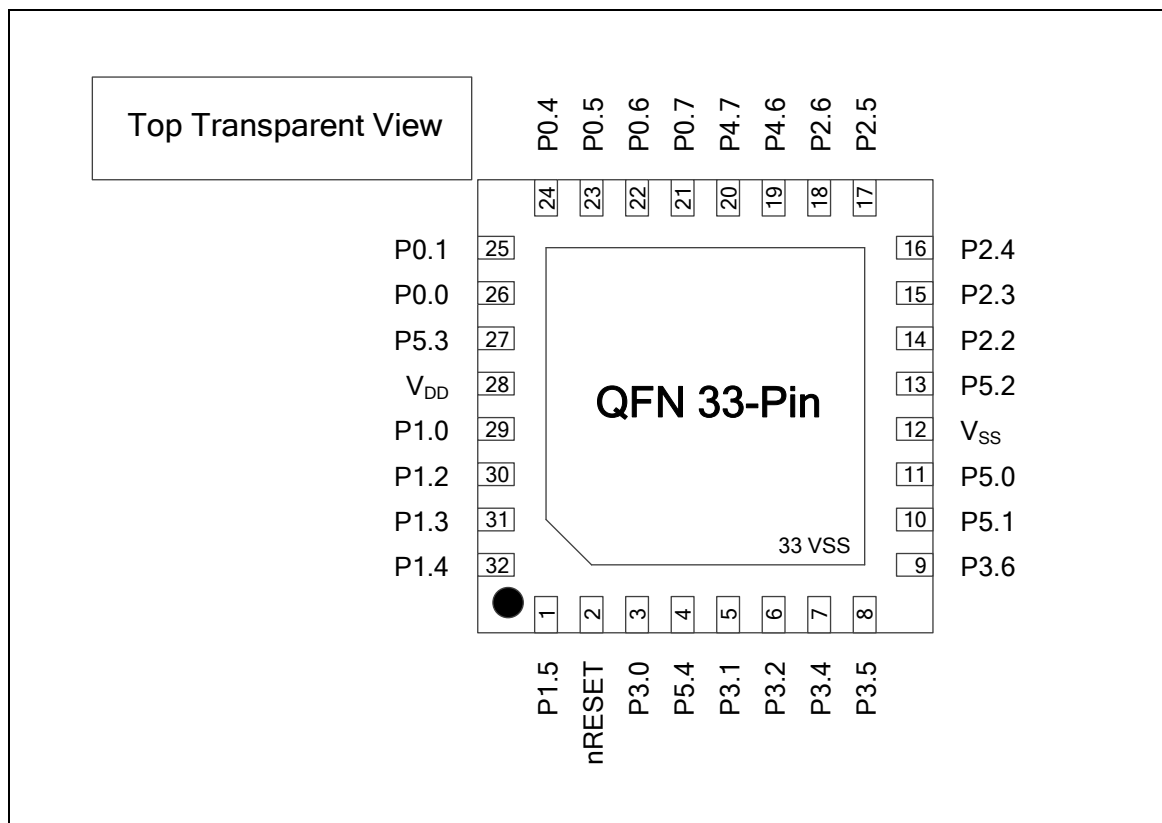


Figure 4.3-3 NuMicro® Mini58 Series QFN 33-pin Diagram

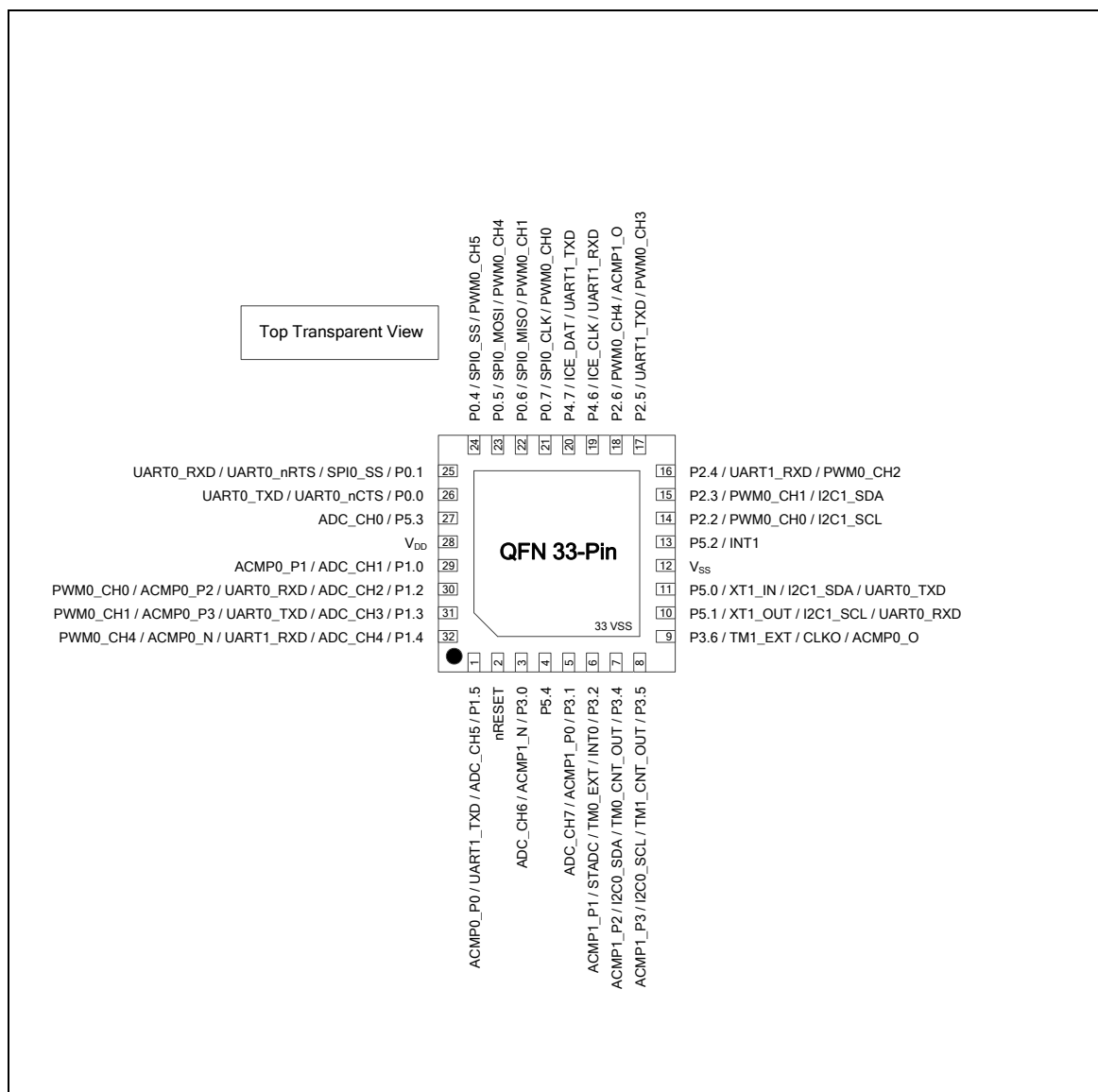


Figure 4.3-4 NuMicro® Mini58 Series QFN 33-pin Multi-function Diagram

4.3.3 TSSOP 20-pin

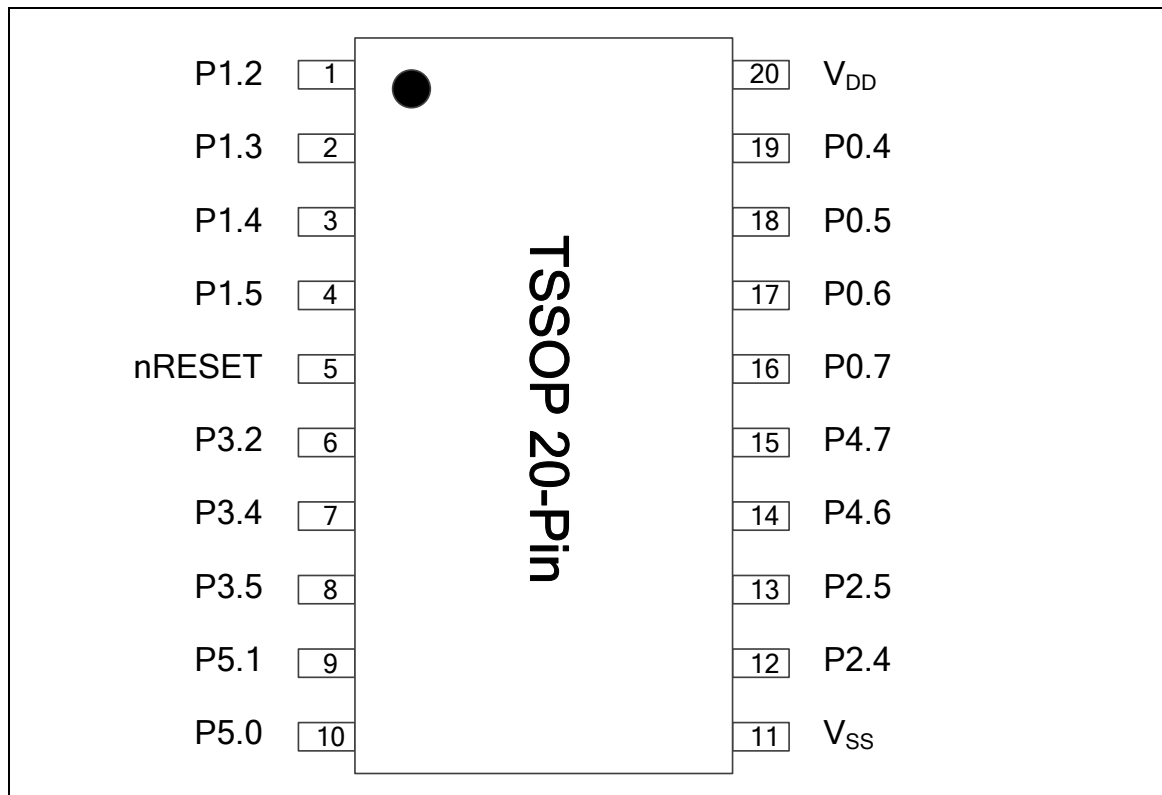


Figure 4.3-5 NuMicro® Mini58 Series TSSOP 20-pin Diagram

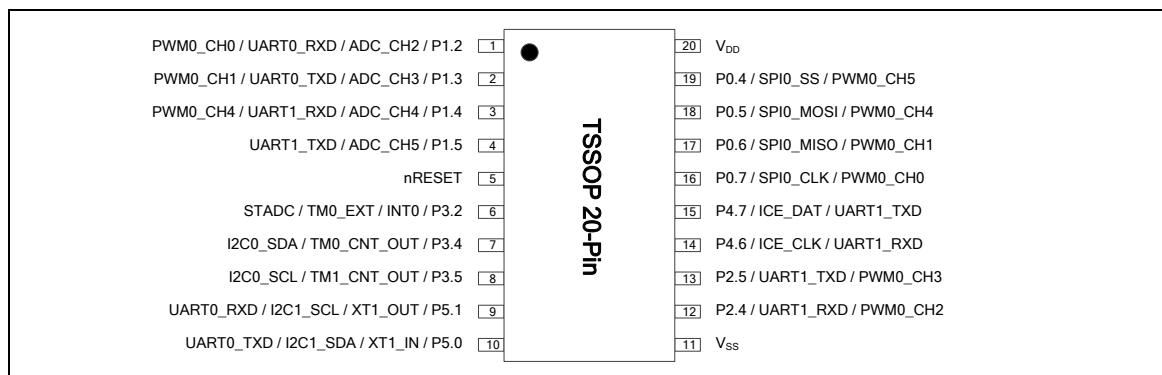


Figure 4.3-6 NuMicro® Mini58 Series TSSOP 20-pin Multi-function Diagram

4.4 Pin Description

Pin Number			Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin			
1	---	---	NC	---	Not connected
2	1	4	P1.5	I/O	General purpose digital I/O pin
			ADC_CH5	AI	ADC analog input pin
			UART1_TXD	O	UART1 transmitter output pin
			ACMP0_P0	AI	Analog comparator positive input pin
3	2	5	nRESET	I(ST)	The Schmitt trigger input pin for hardware device reset. A “Low” on this pin for 768 clock counter of Internal RC 22.1184 MHz while the system clock is running will reset the device. nRESET pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
4	3	---	P3.0	I/O	General purpose digital I/O pin
			ADC_CH6	AI	ADC analog input pin
			ACMP1_N	AI	Analog comparator negative input pin
5	---	---	AV _{SS}	AP	Ground pin for analog circuit
6	4	---	P5.4	I/O	General purpose digital I/O pin
7	5	---	P3.1	I/O	General purpose digital I/O pin
			ADC_CH7	AI	ADC analog input pin
			ACMP1_P0	AI	Analog comparator positive input pin
8	6	6	P3.2	I/O	General purpose digital I/O pin
			INT0	I	External interrupt 0 input pin
			STADC	I	ADC external trigger input pin
			TM0_EXT	I/O	Timer 0 external capture / reset trigger input pin / toggle output pin
			ACMP1_P1	AI	Analog comparator positive input pin (not support in TSSOP20 package)
9	7	7	P3.4	I/O	General purpose digital I/O pin
			TM0_CNT_OUT	I/O	Timer 0 external event counter input pin / toggle output pin
			I2C0_SDA	I/O	I ² C0 data I/O pin
			ACMP1_P2	AI	Analog comparator positive input pin
10	8	8	P3.5	I/O	General purpose digital I/O pin
			TM1_CNT_OUT	I/O	Timer 1 external event counter input pin / toggle output pin
			I2C0_SCL	I/O	I ² C0 clock I/O pin
			ACMP1_P3	AI	Analog comparator positive input pin
11	---	---	NC	---	Not connected

Pin Number			Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin			
12	---	---	NC	---	Not connected
13	---	--	NC	---	Not connected
14	9	---	P3.6	I/O	General purpose digital I/O pin
			ACMP0_O	O	Analog comparator output pin
			CLKO	O	Frequency divider output pin
			TM1_EXT	I/O	Timer 1 external capture / reset trigger input pin / toggle output pin
15	10	9	P5.1	I/O	General purpose digital I/O pin
			XT1_OUT	O	The output pin from the internal inverting amplifier. It emits the inverted signal of XT1_IN.
			I2C1_SCL	I/O	I ² C1 clock I/O pin
			UART0_RXD	I	UART0 data receiver input pin
16	11	10	P5.0	I/O	General purpose digital I/O pin
			XT1_IN	I	The input pin to the internal inverting amplifier. The system clock could be from external crystal or resonator.
			I2C1_SDA	I/O	I ² C1 data I/O pin
			UART0_TXD	O	UART0 transmitter output pin
17	12	11	V _{ss}	P	Ground pin for digital circuit
	33				
18	---	---	LDO_CAP	P	LDO output pin
19	---	---	P5.5	I/O	General purpose digital I/O pin User program must enable pull-up resistor in the QFN-33 package.
20	13	---	P5.2	I/O	General purpose digital I/O pin
			INT1	I	External interrupt 1 input pin
21	---	---	NC	---	Not connected
22	14	---	P2.2	I/O	General purpose digital I/O pin
			PWM0_CH0	O	PWM0 output of PWM unit
			I2C1_SCL	I/O	I ² C1 clock I/O pin
23	15	---	P2.3	I/O	General purpose digital I/O pin
			PWM0_CH1	O	PWM1 output of PWM unit
			I2C1_SDA	I/O	I ² C1 data I/O pin
24	16	12	P2.4	I/O	General purpose input/output digital pin
			UART1_RXD	I	UART1 data receiver input pin
			PWM0_CH2	O	PWM2 output of PWM unit

Pin Number			Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin			
25	17	13	P2.5	I/O	General purpose digital I/O pin
			UART1_TXD	O	UART1 transmitter output pin
			PWM0_CH3	O	PWM3 output of PWM unit
26	18	---	P2.6	I/O	General purpose digital I/O pin
			PWM0_CH4	O	PWM4 output of PWM unit
			ACMP1_O	O	Analog comparator output pin
27	---	---	NC	---	Not connected
28	---	---	NC	---	Not connected
29	19	14	P4.6	I/O	General purpose digital I/O pin
			ICE_CLK	I	Serial wired debugger clock pin
			UART1_RXD	I	UART1 data receiver input pin
30	20	15	P4.7	I/O	General purpose digital I/O pin
			ICE_DAT	I/O	Serial wired debugger data pin
			UART1_TXD	O	UART1 transmitter output pin
31	---	---	NC	---	Not connected
32	21	16	P0.7	I/O	General purpose digital I/O pin
			SPI0_CLK	I/O	SPI serial clock pin
			PWM0_CH0	O	PWM0 output of PWM unit
33	22	17	P0.6	I/O	General purpose digital I/O pin
			SPI0_MISO	I/O	SPI MISO (master in/slave out) pin
			PWM0_CH1	O	PWM1 output of PWM unit
34	23	18	P0.5	I/O	General purpose digital I/O pin
			SPI0_MOSI	O	SPI MOSI (master out/slave in) pin
			PWM0_CH4	O	PWM4 output of PWM unit
35	24	19	P0.4	I/O	General purpose digital I/O pin
			SPI0_SS	I/O	SPI slave select pin
			PWM0_CH5	O	PWM5 output of PWM unit
36	---	---	NC	---	Not connected
37	25	---	P0.1	I/O	General purpose digital I/O pin
			UART0_nRTS	O	UART0 RTS pin
			UART0_RXD	I	UART0 data receiver input pin
			SPI0_SS	I/O	SPI slave select pin
38	26	---	P0.0	I/O	General purpose digital I/O pin

Pin Number			Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin			
			UART0_nCTS	I	UART0 CTS pin
			UART0_TXD	O	UART0 transmitter output pin
39	---	---	NC	---	Not connected
40	---	---	NC	---	Not connected
41	27	---	P5.3	I/O	General purpose digital I/O pin
			ADC_CH0	AI	ADC analog input pin
42	28	20	V _{DD}	P	Power supply for digital circuit
43			AV _{DD}	P	Power supply for analog circuit
44	29	---	P1.0	I/O	General purpose digital I/O pin
			ADC_CH1	AI	ADC analog input pin
			ACMP0_P1	AI	Analog comparator positive input pin
45	30	1	P1.2	I/O	General purpose digital I/O pin
			ADC_CH2	AI	ADC analog input pin
			UART0_RXD	I	UART0 data receiver input pin
			ACMP0_P2	AI	Analog comparator positive input pin (not support in TSSOP20 package)
			PWM0_CH0	O	PWM0 output of PWM unit
46	31	2	P1.3	I/O	General purpose digital I/O pin
			ADC_CH3	AI	ADC analog input pin
			UART0_TXD	O	UART0 transmitter output pin
			ACMP0_P3	AI	Analog comparator positive input pin (not support in TSSOP20 package)
			PWM0_CH1	O	PWM1 output of PWM unit
47	32	3	P1.4	I/O	General purpose digital I/O pin
			ADC_CH4	I/O	ADC analog input pin
			UART1_RXD	I	UART1 data receiver input pin
			ACMP0_N	AI	Analog comparator negative input pin (not support in TSSOP20 package)
			PWM0_CH4	O	PWM4 output of PWM unit
48	---	--	NC	---	Not connected

Table 4.4-1 NuMicro® Mini58 Series Pin Description

[1] I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.

5 BLOCK DIAGRAM

5.1 NuMicro® Mini58 Block Diagram

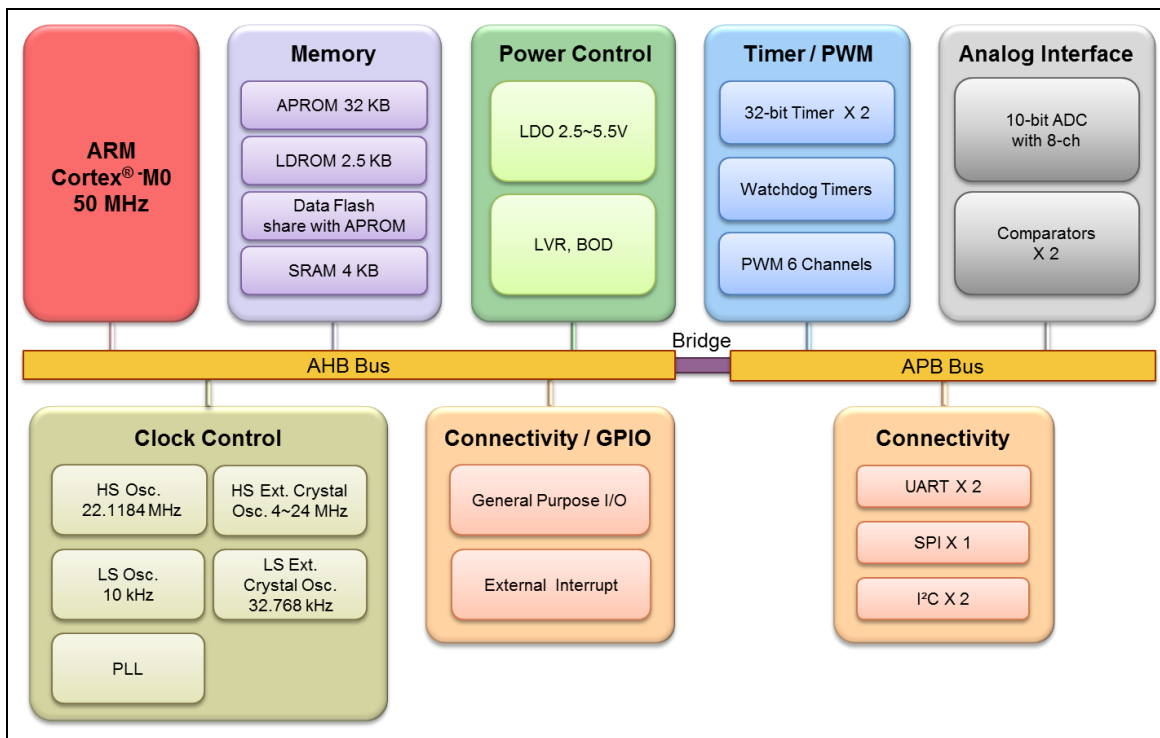


Figure 5.1-1 NuMicro® Mini58 Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M0 Core

6.1.1 Overview

The Cortex®-M0 processor, a configurable, multistage, 32-bit RISC processor, has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processors. The profile supports two modes - Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset and can be entered as a result of an exception return. Figure 6.1-1 shows the functional controller of the processor.

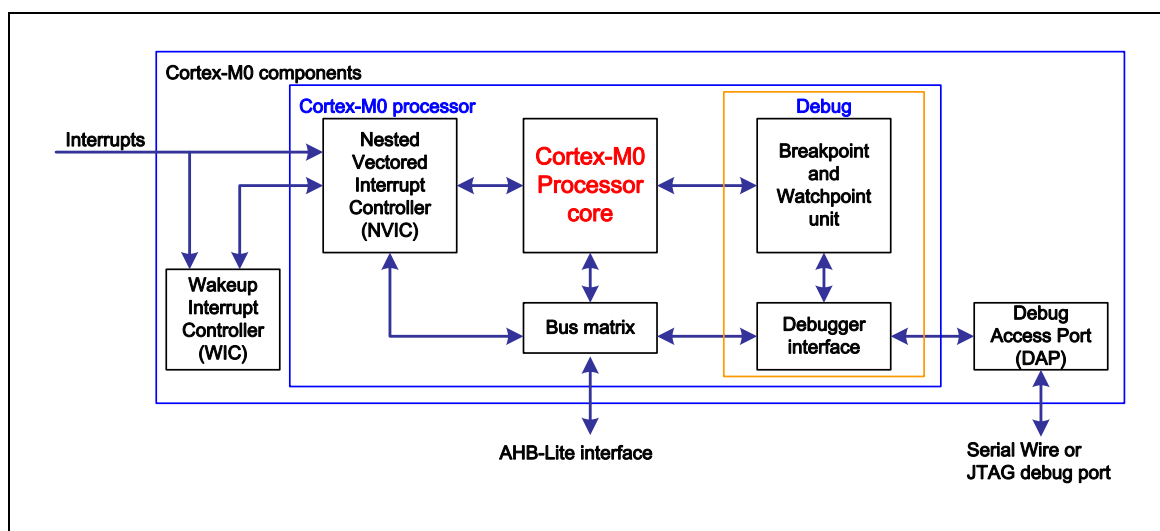


Figure 6.1-1 Functional Block Diagram

6.1.2 Features

- A low gate count processor
 - ARMv6-M Thumb® instruction set
 - Thumb-2 technology
 - ARMv6-M compliant 24-bit SysTick timer
 - A 32-bit hardware multiplier
 - System interface supported with little-endian data accesses
 - Ability to have deterministic, fixed-latency, interrupt handling
 - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
 - C Application Binary Interface compliant exception model:
 - This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
 - Low power Idle mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature