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NuMicro™ Family Nano102/112 Series Datasheet

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NUMICRO™ NANO102/112 SERIES PRELIMINARY DATASHEET



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NUMICRO™ NANO102/112 SERIES PRELIMINARY DATASHEET

1 GENERAL DESCRIPTION

The Nano112 series ultra-low-power 32-bit microcontroller embedded with ARM® Cortex™-M0 core operates at low voltage range from 1.8V to 3.6V and runs up to 32 MHz frequency with 16/32 Kbytes embedded Flash and 4/8 Kbytes embedded SRAM and 4 Kbytes Flash loader memory for In-System Programming (ISP). The Nano112 series integrates 4 COM x 36 SEG or 6 COM x 34 SEG LCD controller, RTC, 12-bit SAR ADC, comparators and provides high performance connectivity peripheral interfaces such as UART, SPI, I²C, GPIOs, and ISO-7816-3 for Smart card. The Nano112 series supports Brown-out Detector, Power-down mode with RTC turn on, RAM retention is less than 1.5 μ A, Deep power down mode with RAM retention is less than 650 nA and fast wake-up via many peripheral interfaces.

The Nano112 series provides low voltage, low operating power consumption, low standby current, high integration peripherals, high-efficiency operation, fast wake-up function and the lowest cost 32-bit microcontrollers. The Nano112 series is suitable for a wide range of battery device applications such as:

- Wearable Device
- Smart Watch
- Wireless Gaming Control
- Hand-Held Medical Device
- RFID Reader
- Mobile Payment Smart Card Reader
- Security Alarm System
- Smart Home Appliance
- Wireless Thermostats
- Wireless Sensors Node Device (WSND)
- Wireless Auto Meter Reading (AMR)
- Portable Wireless Data Collector
- Smart Water, Gas, Heat Meters

The Nano112 series includes two product lines: Nano102 Base line and Nano112 LCD line.

The Nano102 Base line, an ultra-low-power 32-bit microcontroller embedded with ARM® Cortex™-M0 core, operates at low voltage range from 1.8V to 3.6V and runs up to 32 MHz frequency with 16/32 Kbytes embedded flash and 4/8 Kbytes embedded SRAM and 4 Kbytes Flash loader memory for In-System Programming (ISP). It integrates RTC, 8-channels 12-bit SAR ADC, 2xComparators and provides high performance connectivity peripheral interfaces such as 2 x Low Power UARTs, 2 x SPIs, 2 x I²Cs, GPIOs, and 2 x ISO-7816-3 for Smart card. The Nano102 Base line supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

The Nano112 LCD line, an ultra-low-power 32-bit microcontroller embedded with ARM® Cortex™-M0 core, operates at low voltage range from 1.8V to 3.6V and runs up to 32 MHz frequency with 16/32 Kbytes embedded flash and 4/8 Kbytes embedded SRAM and 4 Kbytes Flash loader memory for In-System Programming (ISP). It integrates 4 COM x 36 SEG or 6 COM x 34 SEG LCD controller, RTC, 8-channels 12-bit SAR ADC, 2 x Comparators and provides high performance connectivity peripheral interfaces such as 2 x Low Power UARTs, 2 x SPIs, 2 x I²Cs, GPIOs, and 2 x ISO-7816-3 for Smart card. The Nano112 LCD line supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

Product Line	UART	SPI	I ² C	ADC	ACMP	RTC	SC	Timer	LCD
Nano102	●	●	●	●	●	●	●	●	
Nano112	●	●	●	●	●	●	●	●	●

Table 1 - 1 Connectivity Support Table

2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 Nano102 Features – Base Line

- Low Supply Voltage Range: 1.8 V to 3.6 V
- Ultra-Low Power Consumption
 - ◆ Operation mode : 150 uA/MHz
 - ◆ Power-down mode : 1.5 uA (RTC on, RAM retention)
 - ◆ Deep power down mode : 650 nA (RAM retention)
- Fast Wake-Up From Standby Mode : Less than 6 μ s
- Core
 - ◆ ARM® Cortex™-M0 core running up to 32 MHz
 - ◆ One 24-bit system timer
 - ◆ Supports Low Power Sleep mode
 - ◆ Single-cycle 32-bit hardware multiplier
 - ◆ NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - ◆ Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Flash EPROM Memory
 - ◆ Runs up to 32 MHz with zero wait state for discontinuous address read access
 - ◆ 16/32 Kbytes application program memory (APROM)
 - ◆ 4 KB in system programming (ISP) loader program memory (LDROM)
 - ◆ Programmable data flash start address and memory size with 512 bytes page erase unit
 - ◆ In System Program (ISP)/In Application Program (IAP) to update on-chip Flash EPROM
- SRAM Memory
 - ◆ 4/8 Kbytes embedded SRAM
 - ◆ Supports DMA mode
- DMA: Supports 5 channels: 4 PDMA channels and one CRC channel
 - ◆ PDMA
 - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
 - Supports word boundary address
 - Supports word alignment transfer length in memory-to-memory mode
 - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
 - Supports word/half-word/byte transfer data width from/to peripheral
 - Supports address direction: increment, fixed, and wrap around
 - ◆ CRC

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
 - ◆ CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
 - ◆ CRC-8: $X^8 + X^2 + X + 1$
 - ◆ CRC-16: $X^{16} + X^{15} + X^2 + 1$
 - ◆ CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Clock Control
 - ◆ Flexible selection for different applications
 - ◆ Built-in 12/16 MHz OSC, can be trimmed to 1 % deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12/16 MHz OSC has 2 % deviation within all temperature range.
 - ◆ Low power 10 kHz OSC for watchdog and low power system operation
 - ◆ Supports one PLL, up to 32 MHz, for high performance system operation
External 4~24 MHz crystal input for precise timing operation
 - ◆ External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
 - ◆ Three I/O modes:
 - Push-Pull output
 - Open-Drain output
 - Input only with high impedance
 - ◆ All inputs with Schmitt trigger
 - ◆ I/O pin configured as interrupt source with edge/level setting
 - ◆ Supports High Driver and High Sink I/O mode
 - ◆ Supports input 5V tolerance, except PA.0 ~ PA.7, PA.12, PA.13, PF.0(X32I), PF.1(X32O).
- Timer
 - ◆ Supports 4 sets of 32-bit timers, each with 24-bit up-counting timer and one 8-bit pre-scale counter
 - ◆ Independent Clock Source for each timer
 - ◆ Provides one-shot, periodic, output toggle and continuous operation modes
 - ◆ Internal trigger event to ADC and PDMA
 - ◆ Supports PDMA mode
 - ◆ Wake system up from Power-down mode
- Watchdog Timer
 - ◆ Clock Source from LIRC (Internal 10 kHz Low Speed Oscillator Clock)
 - ◆ Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)
 - ◆ Interrupt or reset selectable when watchdog time-out

- ◆ Wake system up from Power-down mode
- Window Watchdog Timer(WWDT)
 - ◆ 6-bit down counter and 6-bit compare value to make the window period flexible
 - ◆ Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.
- RTC
 - ◆ Supports software compensation by setting frequency compensate register (FCR)
 - ◆ Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
 - ◆ Supports Alarm registers (second, minute, hour, day, month, year)
 - ◆ Selectable 12-hour or 24-hour mode
 - ◆ Automatic leap year recognition
 - ◆ Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
 - ◆ Wake system up from Power-down mode
 - ◆ Supports 80 bytes spare registers and a snoop pin to clear the content of these spare registers
 - ◆ Supports 1, 1/2, 1/4, 1/8, 1/16 Hz clock output
- PWM/Capture
 - ◆ Supports 1 PWM module with two 16-bit PWM generators
 - ◆ Provides four PWM outputs or two complementary paired PWM outputs
 - ◆ Each PWM generator equipped with one clock divider, one 8-bit prescaler, two clock selectors, and one Dead-zone generator for complementary paired PWM
 - ◆ (Shared with PWM timers) with four 16-bit digital capture timers provides four rising/ falling/both capture inputs.
 - ◆ Supports One-shot and Continuous mode
 - ◆ Supports Capture interrupt
- UART
 - ◆ Up to 1 Mbit/s baud rate and support 9600 baud rate @ 32kHz, low power mode
 - ◆ Up to two 16-byte FIFO UART controllers
 - ◆ UART ports with flow control (TX, RX, CTSn and RTSn)
 - ◆ Supports IrDA (SIR) function
 - ◆ Supports LIN function
 - ◆ Supports RS-485 9 bit mode and direction control.
 - ◆ Programmable baud rate generator
 - ◆ Supports PDMA mode
 - ◆ Wake system (CTS_n, received data or RS-485 address matched) up from Power-down mode
- SPI

- ◆ Up to two sets of SPI controllers
- ◆ Master up to 32 MHz, and Slave up to 16 MHz
- ◆ Supports SPI/MICROWIRE Master/Slave mode
- ◆ Full duplex synchronous serial data transfer
- ◆ Variable length of transfer data from 4 to 32 bits
- ◆ MSB or LSB first data transfer
- ◆ RX and TX on both rising or falling edge of serial clock independently
- ◆ Two slave/device select lines when SPI controller is used as the master, and 1 slave/device select line when SPI controller is used as the slave
- ◆ Supports byte suspend mode in 32-bit transmission
- ◆ Supports two channel PDMA requests, one for transmit and another for receive
- ◆ Supports three wire mode, no slave select signal, bi-direction interface
- ◆ Wake system up(SPI clock toggle) from Power-down mode
- I²C
 - ◆ Up to two sets of I²C device
 - ◆ Master/Slave up to 1 Mbit/s
 - ◆ Bi-directional data transfer between masters and slaves
 - ◆ Multi-master bus (no central master)
 - ◆ Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - ◆ Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
 - ◆ Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
 - ◆ Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows
 - ◆ Programmable clocks allowing for versatile rate control
 - ◆ Supports 7-bit addressing mode
 - ◆ Supports multiple address recognition (four slave addresses with mask option)
 - ◆ Wake system up(address match) from Power-down mode
- ADC
 - ◆ 12-bit SAR ADC up to 1Msps conversion rate
 - ◆ Up to 8-ch single-ended input from external pin (PA.0 ~ PA.7)
 - ◆ Four internal channels from internal reference voltage (Int_V_{REF}), Temperature sensor, AV_{DD}, and AV_{SS}.
 - ◆ Supports three reference voltage sources from V_{REF} pin, internal reference voltage (Int_V_{REF}), and AV_{DD}.
 - ◆ Supports Single Scan, Single Cycle Scan, and Continuous Scan mode
 - ◆ Each channel with individual result register
 - ◆ Only scan on enabled channels

- ◆ Threshold voltage detection (comparator function)
- ◆ Conversion started by software programming or external input
- ◆ Supports PDMA mode
- ◆ Supports up to four timer time-out events (TMR0, TMR1, TMR2 and TMR3) to enable ADC
- SmartCard (SC)
 - ◆ Compliant to ISO-7816-3 T=0, T=1
 - ◆ Supports up to two ISO-7816-3 ports
 - ◆ Separates receive/transmit 4 bytes entry FIFO for data payloads
 - ◆ Programmable transmission clock frequency
 - ◆ Programmable receiver buffer trigger level
 - ◆ Programmable guard time selection (11 ETU ~ 267 ETU)
 - ◆ A 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
 - ◆ Supports auto inverse convention function
 - ◆ Supports transmitter and receiver error retry and error limit function
 - ◆ Supports hardware activation sequence process
 - ◆ Supports hardware warm reset sequence process
 - ◆ Supports hardware deactivation sequence process
 - ◆ Supports hardware auto deactivation sequence when detect the card is removal
 - ◆ Supports UART mode (full-duplex)
- ACMP
 - ◆ Supports up to 2 analog comparators
 - ◆ Analog input voltage range: 0 ~ AV_{DD}
 - ◆ Supports Hysteresis function
 - ◆ Two analog comparators with optional internal reference voltage input at negative end
- Wake-up source
 - ◆ Support RTC, WDT, I²C, Timer, UART, SPI, BOD, GPIO
- One built-in temperature sensor with 1 °C resolution
- Brown-out
 - ◆ Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40°C~85°C
- Packages:
 - ◆ All Green package (RoHS)
 - ◆ LQFP 64-pin(7x7) / 48-pin(7x7)/ QFN33-pin(5x5)

2.2 Nano112 Features – LCD Line

- Low Supply Voltage Range: 1.8 V to 3.6 V
- Ultra-Low Power Consumption
 - ◆ Operation mode : 150 uA/MHz
 - ◆ Power-down mode : 1.5 uA (RTC on, RAM retention)
 - ◆ Deep power down mode : 650 nA (RAM retention)
- Fast Wake-Up From Standby Mode : Less than 6 μs
- Core
 - ◆ ARM® Cortex™-M0 core running up to 32 MHz
 - ◆ One 24-bit system timer
 - ◆ Supports Low Power Sleep mode
 - ◆ Single-cycle 32-bit hardware multiplier
 - ◆ NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - ◆ Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Flash EPROM Memory
 - ◆ Runs up to 32 MHz with zero wait state for discontinuous address read access.
 - ◆ 16/32 Kbytes application program memory (APROM)
 - ◆ 4 Kbytes In System Programming (ISP) loader program memory (LDROM)
 - ◆ Programmable data flash start address and memory size with 512 bytes page erase unit
 - ◆ In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM
- SRAM Memory
 - ◆ 4/8 Kbytes embedded SRAM
 - ◆ Supports DMA mode
- DMA : Supports 5 channels: 4 PDMA channels, and one CRC channel
 - ◆ PDMA
 - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
 - Supports word boundary address
 - Supports word alignment transfer length in memory-to-memory mode
 - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
 - Supports word/half-word/byte transfer data width from/to peripheral
 - Supports address direction: increment, fixed, and wrap around
 - ◆ CRC
 - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
 - ◆ CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$

- ◆ CRC-8: $X^8 + X^2 + X + 1$
- ◆ CRC-16: $X^{16} + X^{15} + X^2 + 1$
- ◆ CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Clock Control
 - ◆ Flexible selection for different applications
 - ◆ Built-in 12/16 MHz OSC, can be trimmed to 1 % deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12/16 MHz OSC has 2 % deviation within all temperature range.
 - ◆ Low power 10 kHz OSC for watchdog and low power system operation
 - ◆ Supports one PLL, up to 32 MHz, for high performance system operation
 - ◆ External 4~24 MHz crystal input for precise timing operation
 - ◆ External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
 - ◆ Three I/O modes:
 - Push-Pull output
 - Open-Drain output
 - Input only with high impedance
 - ◆ All inputs with Schmitt trigger
 - ◆ I/O pin configured as interrupt source with edge/level setting
 - ◆ Supports High Driver and High Sink I/O mode
 - ◆ Supports input 5V tolerance, except PA.0 ~ PA.7, PA.12, PA.13, P.0(X32I), PF.1(X32O)
- Timer
 - ◆ Supports 4 sets of 32-bit timers, each with 24-bit up-timer and one 8-bit pre-scale counter
 - ◆ Independent Clock Source for each timer
 - ◆ Provides one-shot, periodic, output toggle and continuous operation modes
 - ◆ Internal trigger event to ADC and PDMA
 - ◆ Supports PDMA mode
 - ◆ Wake system up from Power-down mode
- Watchdog Timer
 - ◆ Clock Source from LIRC (Internal 10 kHz Low Speed Oscillator Clock)
 - ◆ Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)
 - ◆ Interrupt or reset selectable when watchdog time-out
 - ◆ Wake system up from Power-down mode
- Window Watchdog Timer(WWDT)
 - ◆ 6-bit down counter and 6-bit compare value to make the window period flexible

- ◆ Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.
- RTC
 - ◆ Supports software compensation by setting frequency compensate register (FCR)
 - ◆ Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
 - ◆ Supports Alarm registers (second, minute, hour, day, month, year)
 - ◆ Selectable 12-hour or 24-hour mode
 - ◆ Automatic leap year recognition
 - ◆ Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
 - ◆ Wake system up from Power-down mode
 - ◆ Supports 80 bytes spare registers and a snoop pin to clear the content of these spare registers
 - ◆ Supports 1, 1/2, 1/4, 1/8, 1/16 Hz clock output
- PWM/Capture
 - ◆ Supports 1 PWM module with two 16-bit PWM generators
 - ◆ Provides four PWM outputs or two complementary paired PWM outputs
 - ◆ Each PWM generator equipped with one clock divider, one 8-bit prescaler, two clock selectors, and one Dead-zone generator for complementary paired PWM
 - ◆ (Shared with PWM timers) with four 16-bit digital capture timers provides four rising/ falling/both capture inputs.
 - ◆ Supports Capture interrupt
- UART
 - ◆ Up to 1 Mbit/s baud rate and support 9600 baud rate @ 32kHz, low power mode
 - ◆ Up to two 16-byte FIFO UART controllers
 - ◆ UART ports with flow control (TX, RX, CTSn and RTSn)
 - ◆ Supports IrDA (SIR) function
 - ◆ Supports LIN function
 - ◆ Supports RS-485 9 bit mode and direction control (Low Density Only)
 - ◆ Programmable baud rate generator
 - ◆ Supports PDMA mode
 - ◆ Wake system up (CTS, received data or RS-485 address matched) from Power-down mode
- SPI
 - ◆ Up to two sets of SPI controller
 - ◆ Master up to 32 MHz, and Slave up to 16 MHz
 - ◆ Supports SPI/MICROWIRE Master/Slave mode
 - ◆ Full duplex synchronous serial data transfer

- ◆ Variable length of transfer data from 4 to 32 bits
- ◆ MSB or LSB first data transfer
- ◆ RX and TX on both rising or falling edge of serial clock independently
- ◆ Two slave/device select lines when SPI controller is as the master, and 1 slave/device select line when SPI controller is as the slave
- ◆ Supports byte suspend mode in 32-bit transmission
- ◆ Supports two channel PDMA requests, one for transmit and another for receive
- ◆ Supports three wire mode, no slave select signal, bi-direction interface
- ◆ Wake system up (SPI clock toggle) from Power-down mode
- I²C
 - ◆ Up to two sets of I²C devices
 - ◆ Master/Slave up to 1Mbit/s
 - ◆ Bidirectional data transfer between masters and slaves
 - ◆ Multi-master bus (no central master)
 - ◆ Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - ◆ Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
 - ◆ Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
 - ◆ Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows
 - ◆ Programmable clocks allow versatile rate control
 - ◆ Supports 7-bit addressing mode
 - ◆ Supports multiple address recognition (four slave address with mask option)
 - ◆ Wake system up (address match) from Power-down mode
- ADC
 - ◆ 12-bit SAR ADC up to 1Msps conversion rate
 - ◆ Up to 7-ch single-ended input from external pin (PA.0 ~ PA.6)
 - ◆ Four internal channels from internal reference voltage (Int_V_{REF}), Temperature sensor, AV_{DD}, and AV_{SS}
 - ◆ Supports three reference voltage sources from V_{REF} pin, internal reference voltage (Int_V_{REF}), and AV_{DD}.
 - ◆ Single scan/single cycle scan/continuous scan
 - ◆ Each channel with individual result register
 - ◆ Only scan on enabled channels
 - ◆ Threshold voltage detection (comparator function)
 - ◆ Conversion start by software programming or external input
 - ◆ Supports PDMA mode
 - ◆ Supports up to four timer time-out events (TMR0, TMR1, TMR2, and TMR3) to

- enable ADC
- SmartCard (SC)
 - ◆ Compliant to ISO-7816-3 T=0, T=1
 - ◆ Supports up to two ISO-7816-3 ports
 - ◆ Separates receive / transmit 4 bytes entry FIFO for data payloads
 - ◆ Programmable transmission clock frequency
 - ◆ Programmable receiver buffer trigger level
 - ◆ Programmable guard time selection (11 ETU ~ 267 ETU)
 - ◆ A 24-bit and two 8-bit time-out counter for Answer to Request (ATR) and waiting times processing
 - ◆ Supports auto inverse convention function
 - ◆ Supports transmitter and receiver error retry and error limit function
 - ◆ Supports hardware activation sequence process
 - ◆ Supports hardware warm reset sequence process
 - ◆ Supports hardware deactivation sequence process
 - ◆ Supports hardware auto deactivation sequence when detect the card is removal
 - ◆ Supports UART mode (full-duplex)
- ACMP
 - ◆ Supports up to 2 analog comparators
 - ◆ Analog input voltage range: 0 ~ AV_{DD}
 - ◆ Supports Hysteresis function
 - ◆ Two analog comparators with optional internal reference voltage input at negative end
- Wake-up source
 - ◆ Support RTC, WDT, I²C, Timer, UART, SPI, BOD, GPIO
- LCD
 - ◆ LCD driver for up to 4 COM x 36 SEG or 6 COM x 34 SEG
 - ◆ Supports Static, 1/2 bias and 1/3 bias voltage
 - ◆ Six display modes; Static, 1/2 duty, 1/3 duty, 1/4 duty, 1/5 duty and 1/6 duty.
 - ◆ Selectable LCD frequency by frequency divider
 - ◆ Configurable frame frequency
 - ◆ Internal Charge pump, adjustable contrast adjustment
 - ◆ Configurable Charge pump frequency
 - ◆ Blinking capability
 - ◆ Supports R-type/C-type/External C-type method
 - ◆ Configurable internal R-ladder resistor value (200K/300K/400K)
 - ◆ LCD frame interrupt
- One built-in temperature sensor with 1 °C resolution

- Brown-out
 - ◆ Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40°C~85°C
- Packages:
 - ◆ All Green package (RoHS)
 - ◆ LQFP 100-pin(14x14) / 64-pin(10x10) / 64-pin(7x7) / 48-pin(7x7)

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12/16 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NTC	Negative Temperature Coefficient
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PTC	Positive Temperature Coefficient
PT1000	Thermal Resistance
PWM	Pulse Width Modulation

QEI	Quadrature Encoder Interface
SDIO	Secure Digital Input/Output
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro™ Nano102/112 Series Selection Code

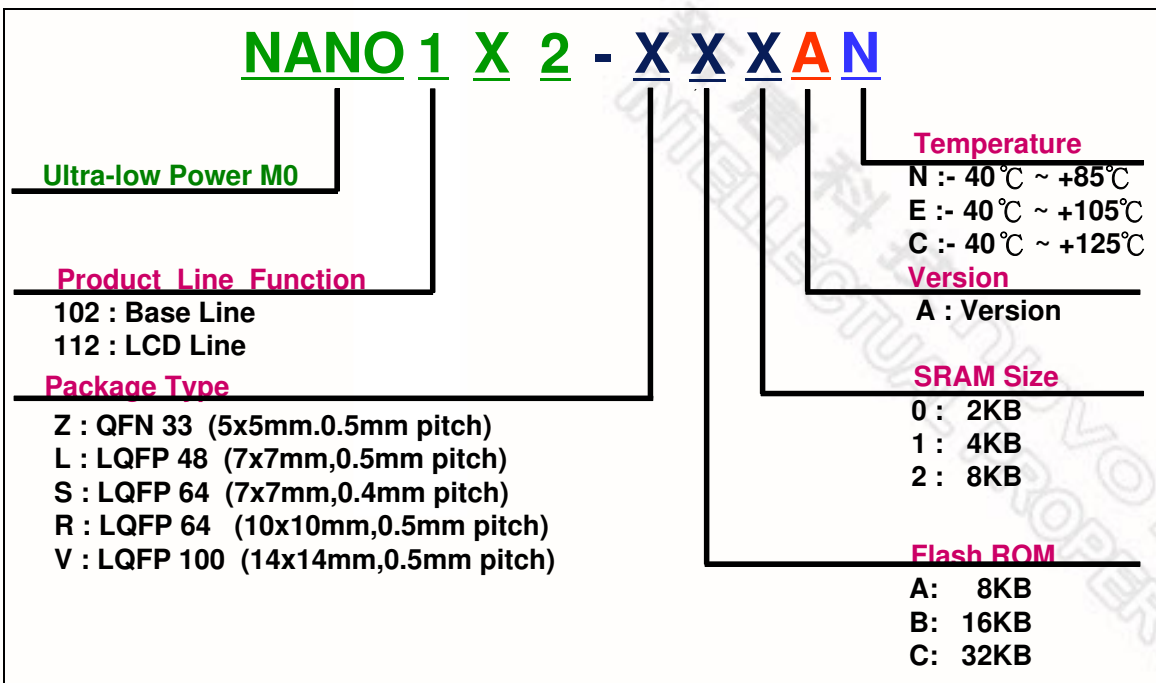


Figure 4-1 NuMicro™ Nano112 Series Selection Code

4.2 NuMicro™ Nano112 Products Selection Guide

4.2.1 NuMicro™ Nano102 Base Line Selection Guide

Part No.	Flash	SRAM	Data Flash	ISP ROM	IO	Timer (32-bit)	Connectivity			Comp	PWM (16-bit)	ADC (12-bit)	RTC	IRC 10 kHz / 12 MHz / 16 MHz	PDMA	LCD	ISO-7816-3	ISP ICP	Package	Maximum Operating Temp. Range (°C)
							UART	SPI	IC											
NANO102ZB1AN	16K	4K	Configurable	4K	up to 27	4	3	2	2	2	4	2	√	√	4	-	1	√	QFN33	-40 to +85
NANO102ZC2AN	32K	8K	Configurable	4K	up to 27	4	3	2	2	2	4	2	√	√	4	-	1	√	QFN33	-40 to +85
NANO102LB1AN	16K	4K	Configurable	4K	up to 40	4	4	2	2	2	4	7	√	√	4	-	2	√	LQFP48	-40 to +85
NANO102LC2AN	32K	8K	Configurable	4K	up to 40	4	4	2	2	2	4	7	√	√	4	-	2	√	LQFP48	-40 to +85
NANO102SC2AN	32K	8K	Configurable	4K	up to 58	4	4	2	2	2	4	7	√	√	4	-	2	√	LQFP64*	-40 to +85

QFN33: 5x5mm
LQFP48: 7x7mm
LQFP64*: 7x7mm

NUMICRO™ NANO102/112 SERIES PRELIMINARY DATASHEET

4.2.2 NuMicro™ Nano112 LCD Line Selection Guide

Part No.	Flash	SRAM	Data Flash	ISP ROM	IO	Timer (32-bit)	Connectivity			Comp	PWM (16-bit)	ADC (12-bit)	RTC	IRC 10KHz / 12MHz / 16MHz	PDMA	LCD	ISO 7816-3	ISP ICP	Package	Maximum Operating Temp. Range (°C)
							UART	SPI	I ² C											
NANO112LB1AN	16K	4K	Configurable	4K	up to 40	4	4	2	2	2	4	7	√	√	4	4x20, 6x18	2	√	LQFP48	-40 to +85
NANO112LC2AN	32K	8K	Configurable	4K	up to 40	4	4	2	2	2	4	7	√	√	4	4x20, 6x18	2	√	LQFP48	-40 to +85
NANO112SB1AN	16K	4K	Configurable	4K	up to 58	4	4	2	2	2	4	7	√	√	4	4x32, 6x30	2	√	LQFP64	-40 to +85
NANO112SC2AN	32K	8K	Configurable	4K	up to 58	4	4	2	2	2	4	7	√	√	4	4x32, 6x30	2	√	LQFP64	-40 to +85
NANO112RB1AN	16K	4K	Configurable	4K	up to 58	4	4	2	2	2	4	7	√	√	4	4x32, 6x30	2	√	LQFP64*	-40 to +85
NANO112RC2AN	32K	8K	Configurable	4K	up to 58	4	4	2	2	2	4	7	√	√	4	4x32, 6x30	2	√	LQFP64*	-40 to +85
NANO112VC2AN	32K	8K	Configurable	4K	up to 80	4	4	2	2	2	4	8	√	√	4	4x36, 6x34	2	√	LQFP100	-40 to +85

LQFP48: 7x7mm
 LQFP64: 7x7mm
 LQFP64*: 10x10mm

4.3 Pin Configuration

4.3.1 NuMicro™ Nano102 Pin Diagrams

4.3.1.1 NuMicro™ Nano102 LQFP 64-pin

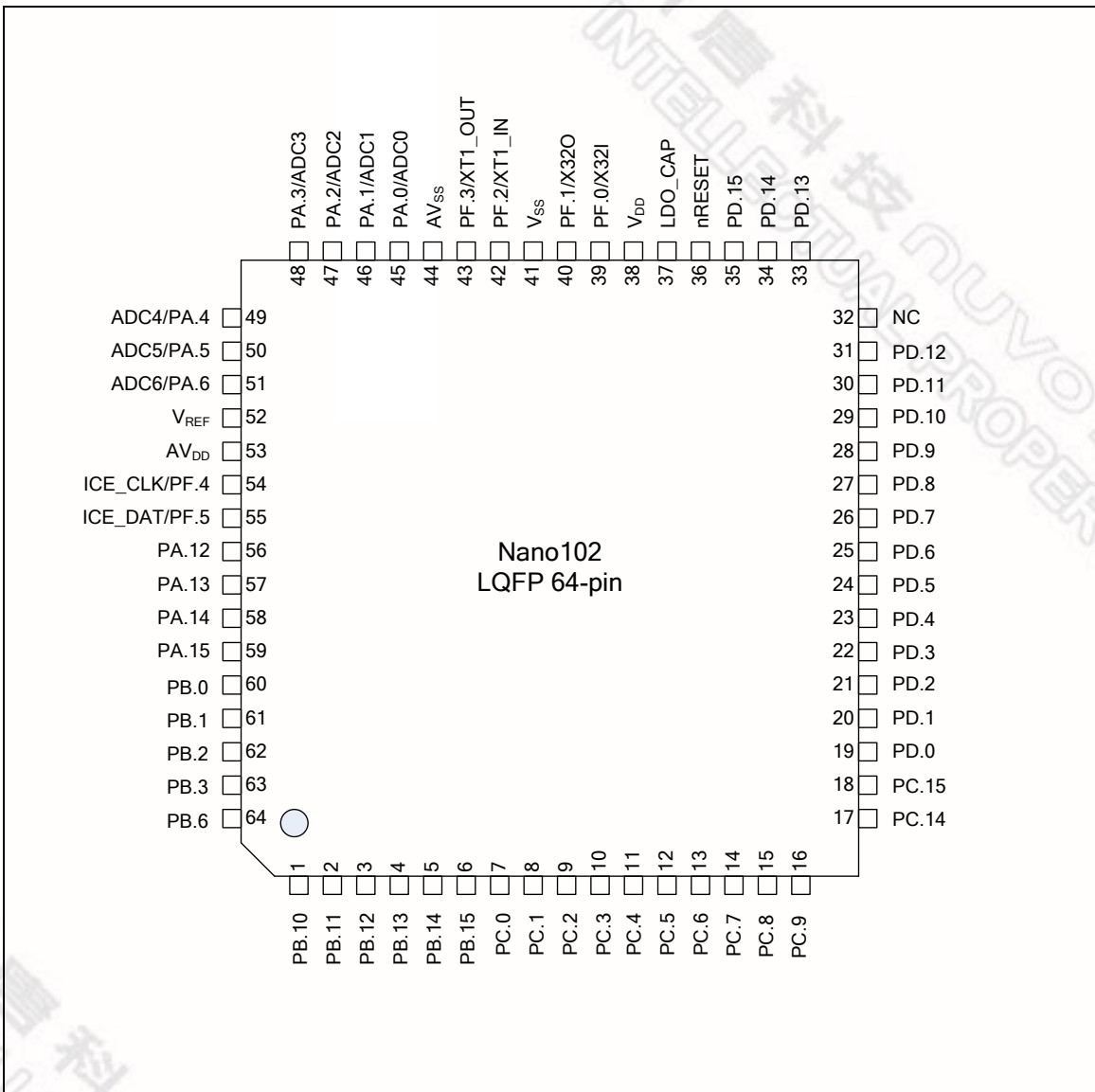


Figure 4- 2 NuMicro™ Nano102 LQFP 64-pin Diagram