



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



NVMFD5853NL

Power MOSFET

40 V, 10 mΩ, 34 A, Dual N-Channel Logic Level, Dual SO-8FL

Features

- Small Footprint (5x6 mm) for Compact Designs
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVMFD5853NLWF – Wettable Flanks Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free Device

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	40	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current $R_{\Psi J-mb}$ (Notes 1, 2, 3, 4)	Steady State	$T_{mb} = 25^\circ\text{C}$	34	A
		$T_{mb} = 100^\circ\text{C}$	24	
Power Dissipation $R_{\Psi J-mb}$ (Notes 1, 2, 3)	Steady State	$T_{mb} = 25^\circ\text{C}$	24	W
		$T_{mb} = 100^\circ\text{C}$	12	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3 & 4)	Steady State	$T_A = 25^\circ\text{C}$	12	A
		$T_A = 100^\circ\text{C}$	8.5	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 3)	Steady State	$T_A = 25^\circ\text{C}$	3.0	W
		$T_A = 100^\circ\text{C}$	1.5	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	165	A
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	34	A	
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}, V_{GS} = 10 \text{ V}, I_{L(pk)} = 28.3 \text{ A}, L = 0.1 \text{ mH}, R_G = 25 \Omega$)	E_{AS}	40	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Mounting Board (top) – Steady State (Notes 2, 3)	$R_{\Psi J-mb}$	6.2	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	51	
Junction-to-Ambient – Steady State (min footprint)		162	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second are higher but are dependent on pulse duration and duty cycle.

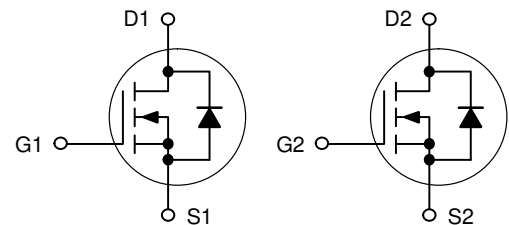


ON Semiconductor®

<http://onsemi.com>

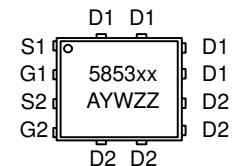
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
40 V	10 mΩ @ 10 V	34 A
	15 mΩ @ 4.5 V	

Dual N-Channel



DFN8 5x6
(SO8FL)
CASE 506BT

MARKING DIAGRAM



5853NL = Specific Device Code for NVMFD5853NL

5853LW = Specific Device Code for NVMFD5853NLWF

A = Assembly Location

Y = Year

W = Work Week

ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NVMFD5853NLT1G	DFN8 (Pb-Free)	1500 / Tape & Reel
NVMFD5853NLWFT1G	DFN8 (Pb-Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NVMFD5853NL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			37.1		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 40 V	T _J = 25°C		1.0	μA
			T _J = 125°C		100	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.4		2.4	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			5.9		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A		8.4	10	mΩ
		V _{GS} = 4.5 V, I _D = 15 A		12.7	15	
Forward Transconductance	g _{FS}	V _{DS} = 5 V, I _D = 5 A		22		S

CHARGES AND CAPACITANCES

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V		1100		pF
Output Capacitance	C _{oss}			152		
Reverse Transfer Capacitance	C _{rss}			100		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 32 V, I _D = 15 A		12.8		nC
Threshold Gate Charge	Q _{G(TH)}			1.0		
Gate-to-Source Charge	Q _{GS}			3.7		
Gate-to-Drain Charge	Q _{GD}			7.0		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 32 V, I _D = 15 A		23		nC

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 4.5 V, V _{DS} = 20 V, I _D = 15 A, R _G = 2.5 Ω		10		ns
Rise Time	t _r			53		
Turn-Off Delay Time	t _{d(off)}			17		
Fall Time	t _f			30		
Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V, V _{DS} = 20 V, I _D = 15 A, R _G = 2.5 Ω		9.0		ns
Rise Time	t _r			23		
Turn-Off Delay Time	t _{d(off)}			22		
Fall Time	t _f			4.3		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 20 A	T _J = 25°C	0.84	1.1	V
			T _J = 125°C	0.69		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, d _{IS} /d _t = 100 A/μs, I _S = 15 A		20		ns
Charge Time	t _a			12		
Discharge Time	t _b			8.1		
Reverse Recovery Charge	Q _{RR}			12.1		

5. Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

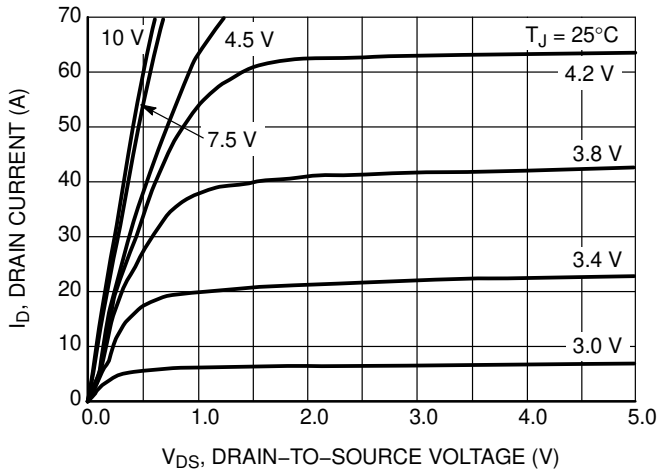


Figure 1. On-Region Characteristics

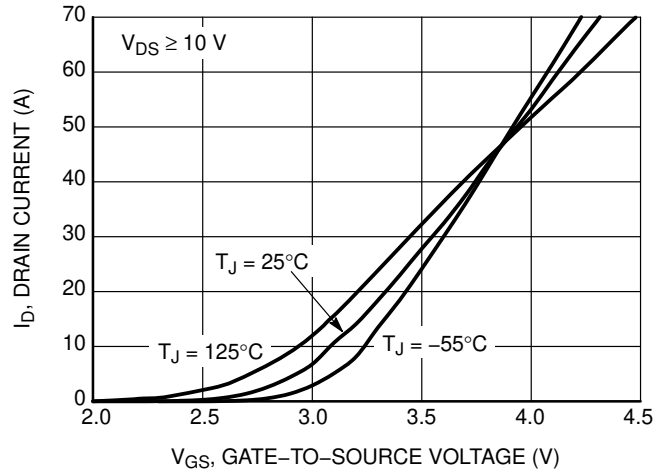


Figure 2. Transfer Characteristics

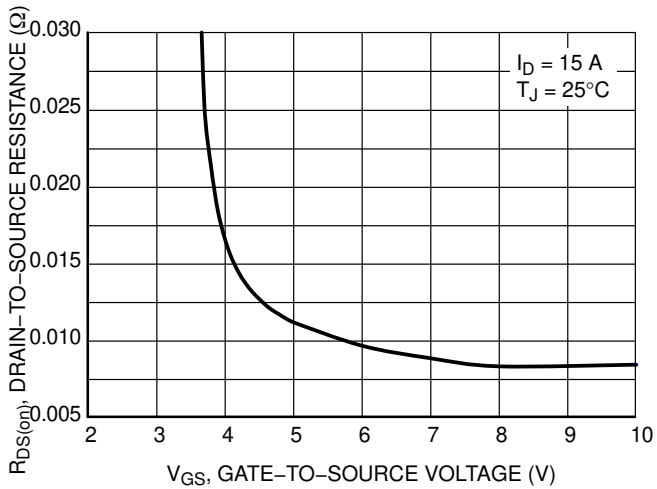


Figure 3. On-Resistance vs. V_{GS}

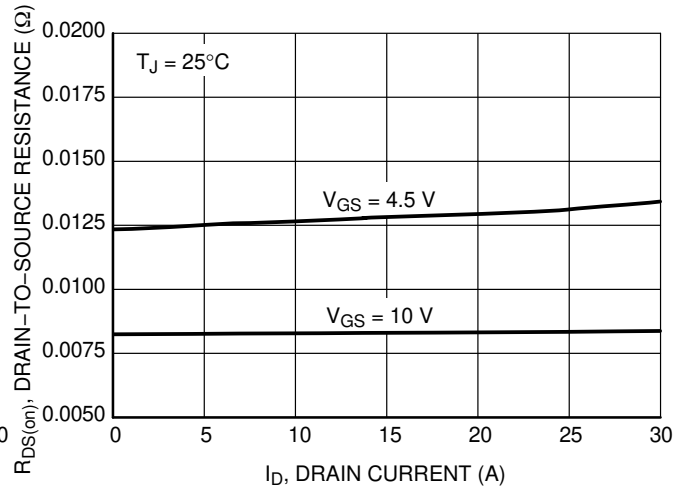


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

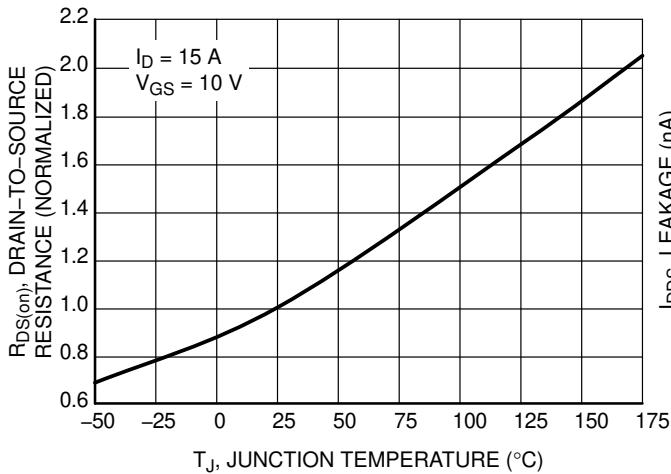


Figure 5. On-Resistance Variation with Temperature

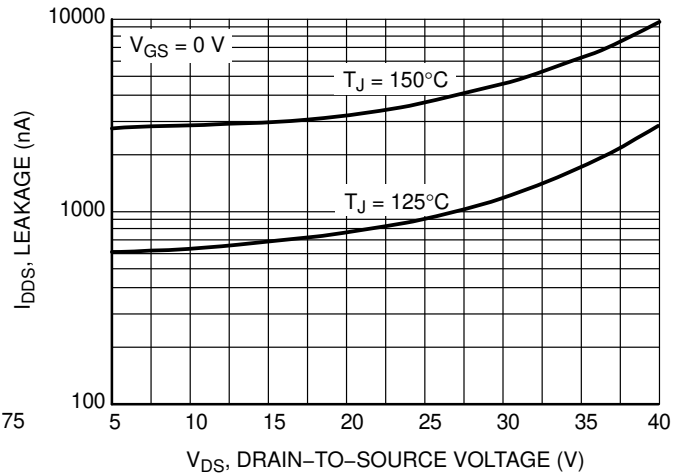


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

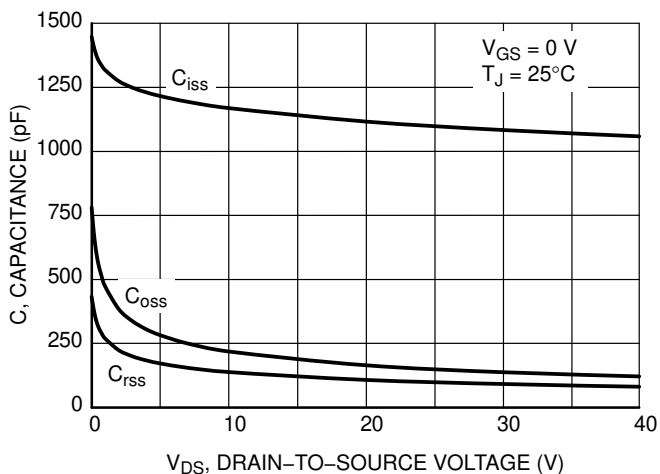


Figure 7. Capacitance Variation

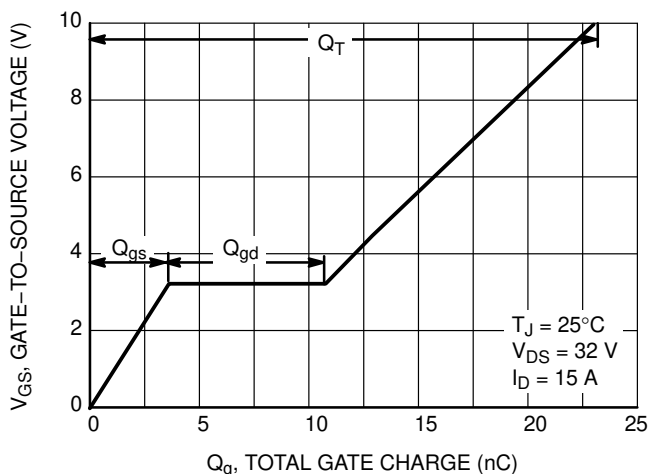


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

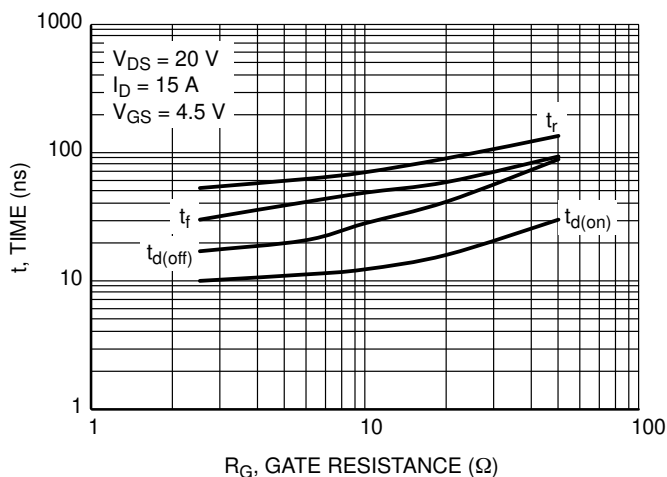


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

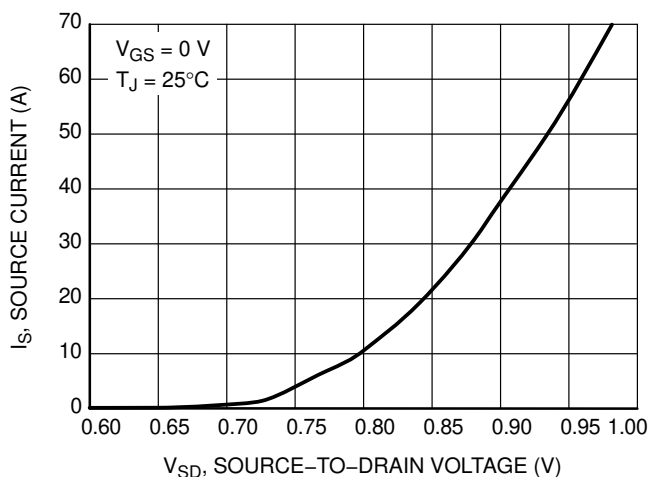


Figure 10. Diode Forward Voltage vs. Current

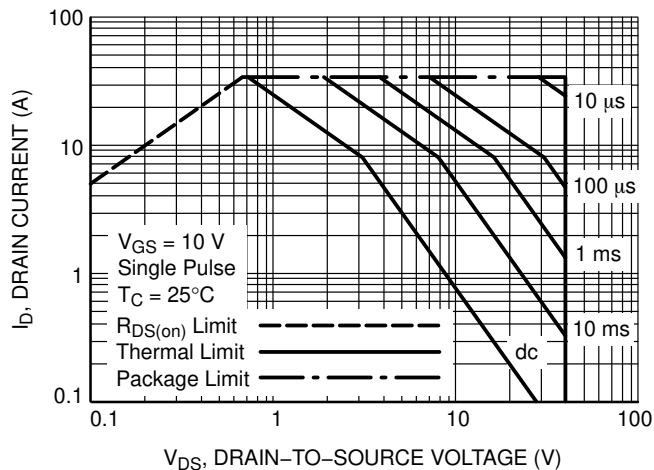


Figure 11. Maximum Rated Forward Biased Safe Operating Area

NVMFD5853NL

TYPICAL CHARACTERISTICS

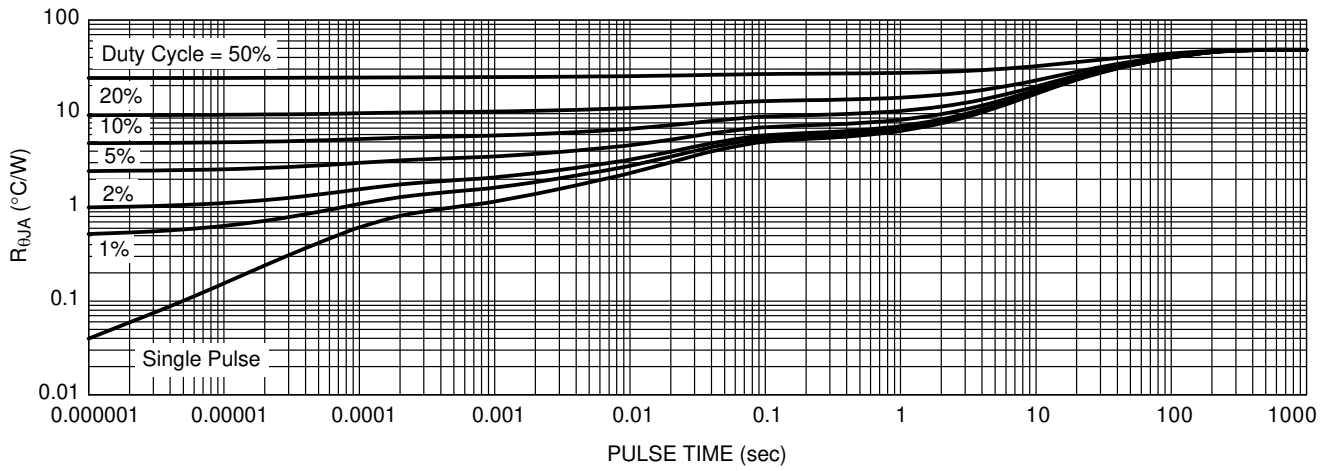


Figure 12. Thermal Response

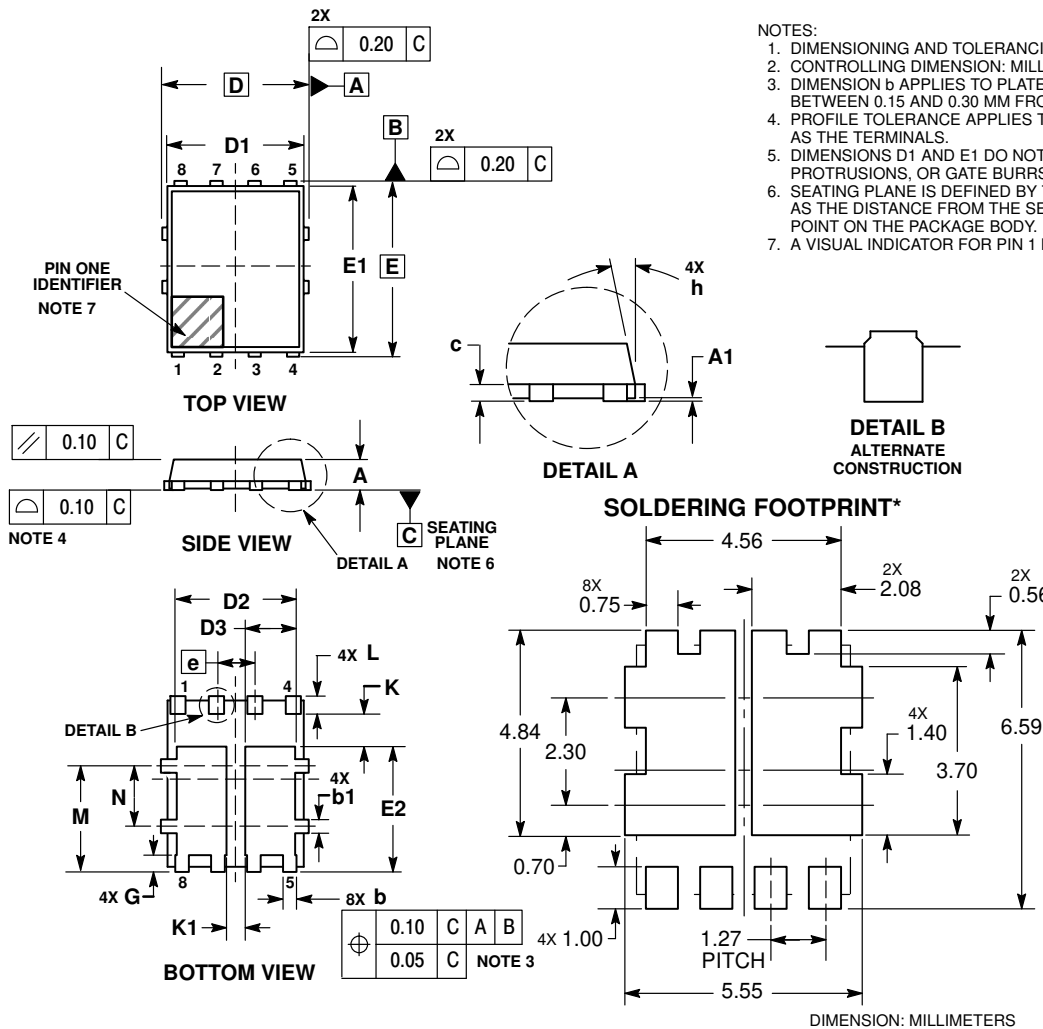
NVMFD5853NL

PACKAGE DIMENSIONS

DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual)

CASE 506BT

ISSUE E



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative