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Power MOSFET

60 V, 4.2 m Ω , 111 A, Dual N-Channel

Features

- Small Footprint (5x6 mm) for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFD5C650NLWF Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

| Parameter | | | Symbol | Value | Unit |
|--|------------------|----------------------------|-----------------------------------|-----------------|------|
| Drain-to-Source Voltage | | | V_{DSS} | 60 | V |
| Gate-to-Source Voltage | | | V _{GS} | ±20 | V |
| Continuous Drain | | T _C = 25°C | I _D | 111 | Α |
| Current R _{θJC} (Notes 1, 2, 3) | Steady | T _C = 100°C | | 88 | |
| Power Dissipation | State | T _C = 25°C | P_{D} | 125 | W |
| R _{θJC} (Notes 1, 2) | | T _C = 100°C | | 62 | |
| Continuous Drain | | T _A = 25°C | I _D | 21 | Α |
| Current R _{θJA} (Notes 1, 2, 3) | Steady | T _A = 100°C | | 15 | |
| Power Dissipation | State | T _A = 25°C | P_{D} | 3.5 | W |
| R _{θJA} (Notes 1 & 2) | | T _A = 100°C | | 1.8 | |
| Pulsed Drain Current | $T_A = 25^\circ$ | °C, t _p = 10 μs | I _{DM} | 502 | Α |
| Operating Junction and Storage Temperature | | | T _J , T _{stg} | –55 to + 175 | °C |
| Source Current (Body Diode) | | | I _S | 91 | Α |
| Single Pulse Drain-to-Source Avalanche Energy (T _J = 25°C, I _{L(pk)} = 6 A) | | | E _{AS} | 186 | mJ |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | | | TL | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|-----------------|-------|------|
| Junction-to-Case - Steady State | $R_{\theta JC}$ | 1.37 | °C/W |
| Junction-to-Ambient - Steady State (Note 2) | $R_{\theta JA}$ | 46.9 | |

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
- 3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

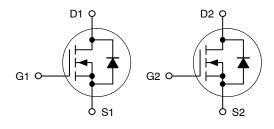


ON Semiconductor®

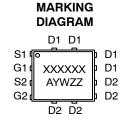
www.onsemi.com

| V _{(BR)DSS} | R _{DS(ON)} MAX | I _D MAX |
|----------------------|-------------------------|--------------------|
| 60 V | 4.2 mΩ @ 10 V | 444. A |
| 00 V | 5.8 mΩ @ 4.5 V | 111 A |

Dual N-Channel







A = Assembly Location

Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

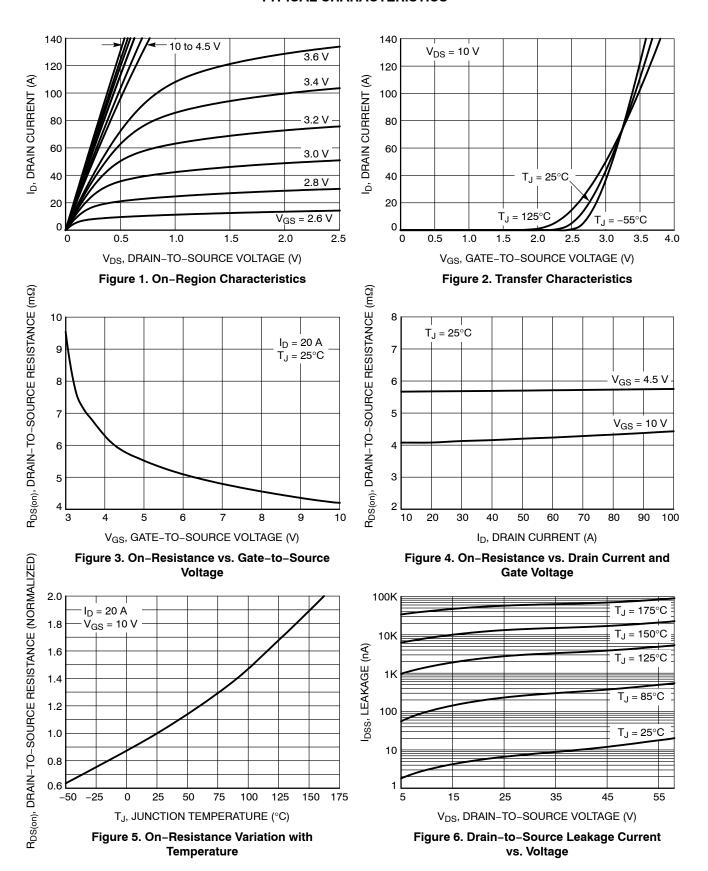
| Parameter | Symbol | Test Condition | | Min | Тур | Max | Unit |
|--|-------------------------------------|---|------------------------|-----|------|-----|-------|
| OFF CHARACTERISTICS | • | | | - | - | - | - |
| Drain-to-Source Breakdown Voltage | V _{(BR)DSS} | $V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$ | | 60 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | V _{(BR)DSS} / | | | | 27.1 | | mV/°C |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{GS} = 0 V, | T _J = 25 °C | | | 10 | μΑ |
| | | V _{DS} = 60 V | T _J = 125°C | | | 100 | |
| Gate-to-Source Leakage Current | I _{GSS} | V _{DS} = 0 V, V _{GS} | = 20 V | | | 100 | nA |
| ON CHARACTERISTICS (Note 4) | | | | | | • | |
| Gate Threshold Voltage | V _{GS(TH)} | $V_{GS} = V_{DS}, I_D = 98 \mu A$ | | 1.2 | | 2.2 | V |
| Negative Threshold Temperature Coefficient | V _{GS(TH)} /T _J | | | | -5.0 | | mV/°C |
| Drain-to-Source On Resistance | R _{DS(on)} | V _{GS} = 10 V | I _D = 20 A | | 3.5 | 4.2 | _ |
| | | V _{GS} = 4.5 V | I _D = 20 A | | 4.6 | 5.8 | mΩ |
| Forward Transconductance | 9FS | V _{DS} = 15 V, I _D = 50 A | | | 120 | | S |
| CHARGES, CAPACITANCES & GATE RESIS | STANCE | | | | • | • | |
| Input Capacitance | C _{ISS} | V _{GS} = 0 V, f = 1 MHz, V _{DS} = 25 V | | | 2546 | | pF |
| Output Capacitance | C _{OSS} | | | | 1258 | | |
| Reverse Transfer Capacitance | C _{RSS} | | | | 17 | | |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 4.5 V, V _{DS} = 48 V; I _D = 50 A | | | 16 | | |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 10 V, V _{DS} = 48 V; I _D = 50 A | | | 37 | | 1 |
| Threshold Gate Charge | Q _{G(TH)} | V _{GS} = 4.5 V, V _{DS} = 48 V; I _D = 50 A | | | 4.3 | | nC |
| Gate-to-Source Charge | Q_{GS} | | | | 8.3 | | |
| Gate-to-Drain Charge | Q_{GD} | | | | 3.1 | | |
| Plateau Voltage | V_{GP} | | | | 3.3 | | V |
| SWITCHING CHARACTERISTICS (Note 5) | | | | | | • | |
| Turn-On Delay Time | t _{d(ON)} | V_{GS} = 4.5 V, V_{DS} = 48 V, I_{D} = 5 A, R_{G} = 1.0 Ω | | | 13 | | - ns |
| Rise Time | t _r | | | | 24 | | |
| Turn-Off Delay Time | t _{d(OFF)} | | | | 37 | | |
| Fall Time | t _f | | | | 13 | | |
| DRAIN-SOURCE DIODE CHARACTERISTIC | cs | | | | • | • | |
| Forward Diode Voltage | V_{SD} | $V_{GS} = 0 \text{ V},$ $I_{S} = 20 \text{ A}$ $T_{J} = 25^{\circ}\text{C}$ $T_{J} = 125^{\circ}\text{C}$ | T _J = 25°C | | 0.9 | 1.2 | |
| | | | | 0.8 | | V | |
| Reverse Recovery Time | t _{RR} | V_{GS} = 0 V, dIS/dt = 50 A/ μ s, I_{S} = 50 A | | | 44 | | |
| Charge Time | t _a | | | | 22 | | ns |
| Discharge Time | t _b | | | | 22 | | 1 |
| Reverse Recovery Charge | Q _{RR} | | | | 35 | | nC |
| | | | | | · | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300~\mu s$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

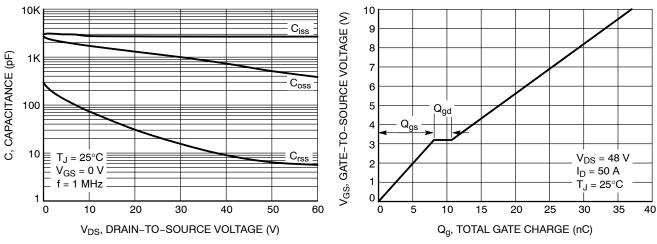


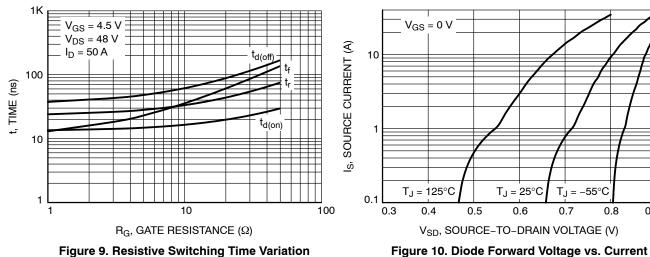
Figure 7. Capacitance Variation

Figure 8. Gate-to-Source vs. Total Charge

 $T_J = -55^{\circ}C$

0.9

0.7



10 μs

100

Figure 9. Resistive Switching Time Variation vs. Gate Resistance

1000

100

10

0.1

0.1

T_C = 25°C V_{GS} ≤ 10 V

Single Pulse

ID, DRAIN CURRENT (A)

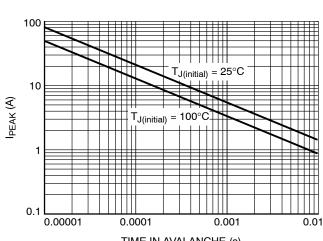


Figure 11. Maximum Rated Forward Biased Safe Operating Area

10

V_{DS}, DRAIN-TO-SOURCE VOLTAGE (V)

 $R_{DS(on)}$ Limit Thermal Limit Package Limit

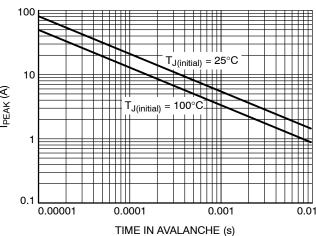


Figure 12. Maximum Drain Current vs. Time in **Avalanche**

1000

TYPICAL CHARACTERISTICS

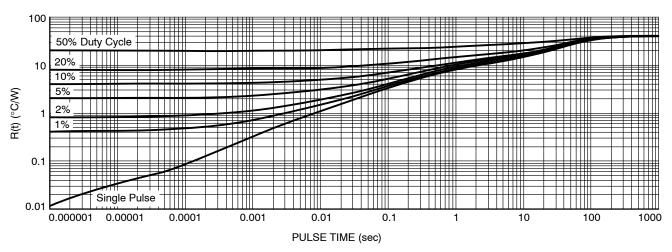


Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

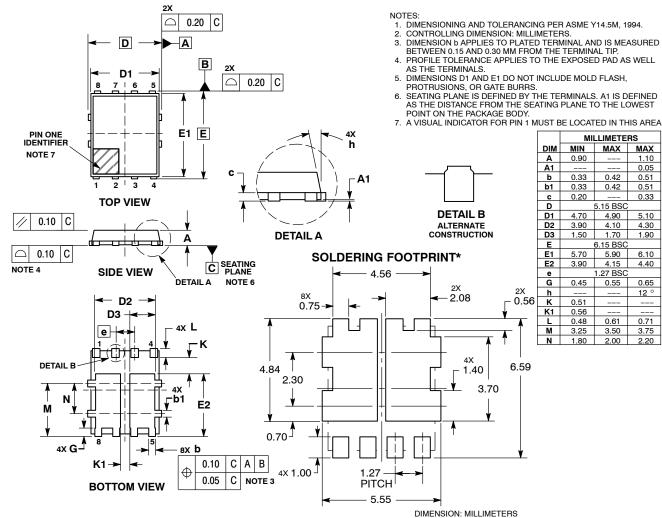
| Device | Marking | Package | Shipping [†] |
|-------------------|---------|------------------------------------|-----------------------|
| NVMFD5C650NLT1G | 5C650L | DFN8 (Pb-Free) | 1500 / Tape & Reel |
| NVMFD5C650NLWFT1G | 650LWF | DFN8 (Pb-Free, Wettable Flanks) | 1500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual)

CASE 506BT **ISSUE E**



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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0.71

3.75

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