imall

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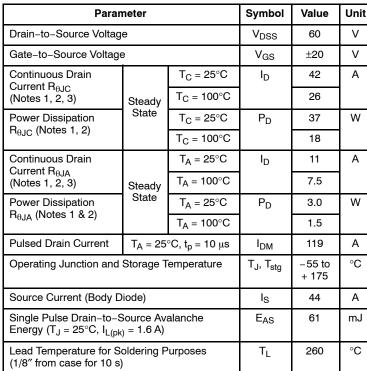
Power MOSFET

60 V, 14.4 m Ω , 42 A, Dual N–Channel

Features

- Small Footprint (5x6 mm) for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFD5C674NLWF Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)



Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	2.86	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	49	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.

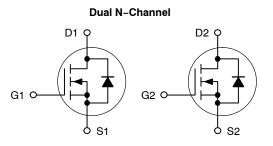
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

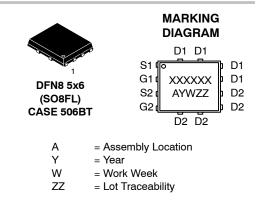


ON Semiconductor®

www.onsemi.com

V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
60 V	14.4 m Ω @ 10 V	40.4
60 V	20.4 mΩ @ 4.5 V	42 A





ORDERING INFORMATION

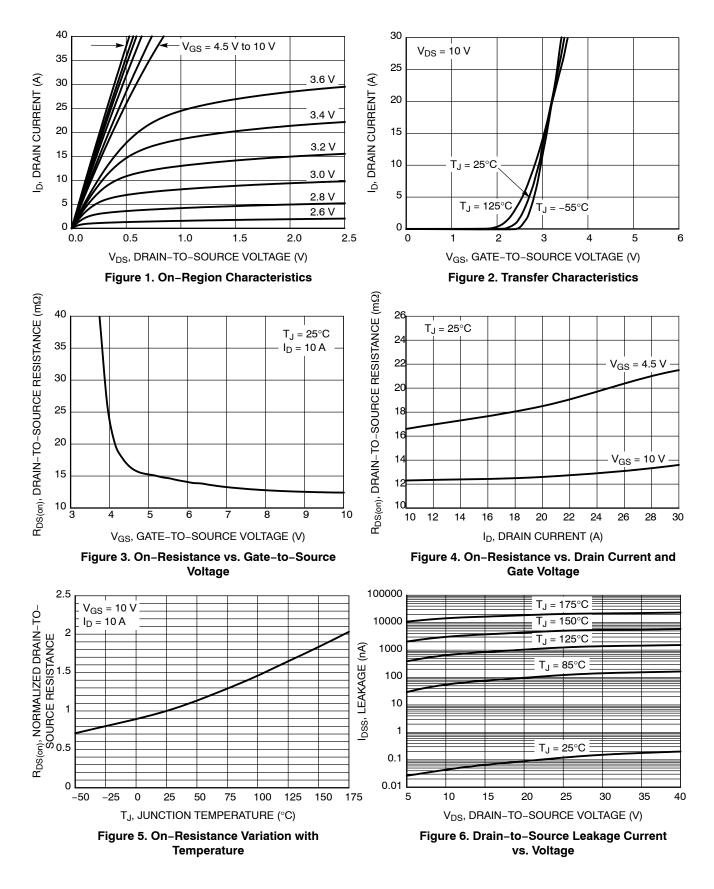
See detailed ordering, marking and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25° C unless otherwise specified)

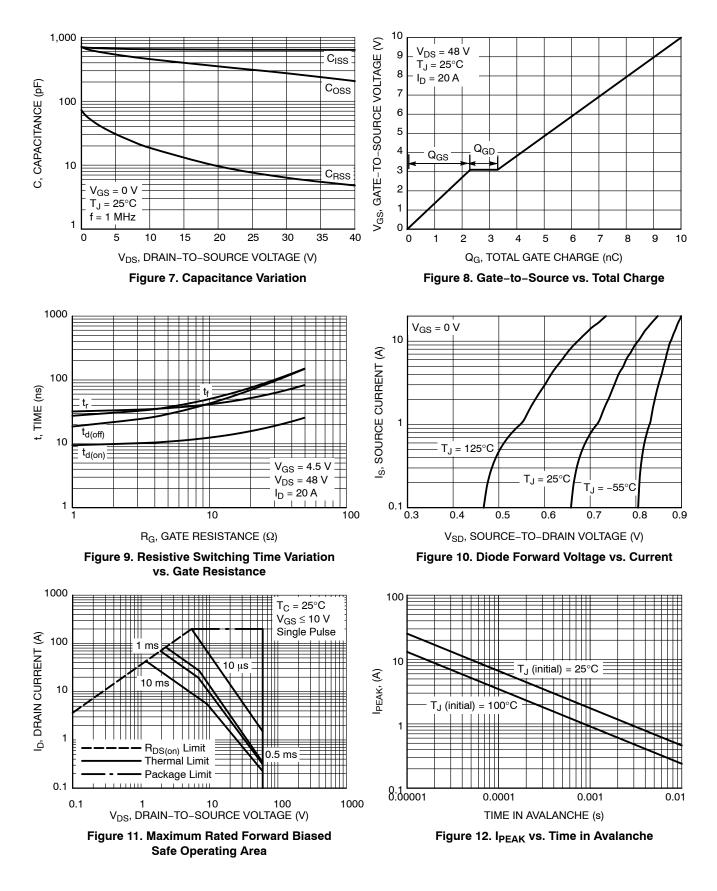
Parameter	Symbol	Test Condi	tion	Min	Тур	Max	Unit
OFF CHARACTERISTICS					1	1	
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA		60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} / T _J				28		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 V,$	T _J = 25 °C			10	Ι.
		$V_{DS} = 60 V$	T _J = 125°C			100	μΑ
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}$, $I_D = 25 \ \mu A$		1.2		2.2	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				-4.6		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 10 A		11.7	14.4	0
		V _{GS} = 4.5 V	I _D = 10 A		16.4	20.4	μ mΩ
Forward Transconductance	9 _{FS}	V _{DS} = 15 V, I _D	= 10 A		27.5		S
CHARGES, CAPACITANCES & GATE RESIS	TANCE			-		-	-
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 25 V			640		pF
Output Capacitance	C _{OSS}				313		
Reverse Transfer Capacitance	C _{RSS}				7.7		
Total Gate Charge	Q _{G(TOT)}	V_{GS} = 4.5 V, V_{DS} = 48 V; I_{D} = 20 A			4.7		
Total Gate Charge	Q _{G(TOT)}	V_{GS} = 10 V, V_{DS} = 48 V; I_{D} = 20 A			10		
Threshold Gate Charge	Q _{G(TH)}				1.4		nC
Gate-to-Source Charge	Q _{GS}	V_{GS} = 4.5 V, V_{DS} = 48 V; I_{D} = 10 A			2.3		
Gate-to-Drain Charge	Q _{GD}				1.0		
Plateau Voltage	V _{GP}				3.1		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn-On Delay Time	t _{d(ON)}	V _{GS} = 4.5 V, V _{DS} = 48 V, I _D = 5 A, R _G = 1.0 Ω			9.5		
Rise Time	t _r				32.1		- ns
Turn-Off Delay Time	t _{d(OFF)}				18.6		
Fall Time	t _f				27.5		
DRAIN-SOURCE DIODE CHARACTERISTIC	s			-		-	-
Forward Diode Voltage	V _{SD}	$V_{GS} = 0 V,$ $I_{S} = 10 A$	$T_J = 25^{\circ}C$		0.9	1.2	
			T _J = 125°C		0.8		V
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dIS/dt = 20 A/μs, I _S = 5 A			23.8		
Charge Time	t _a				11.5		ns
Discharge Time	t _b				12.3		
Reverse Recovery Charge	Q _{RR}				11.2		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. Pulse Test: pulse width ≤ 300 µs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

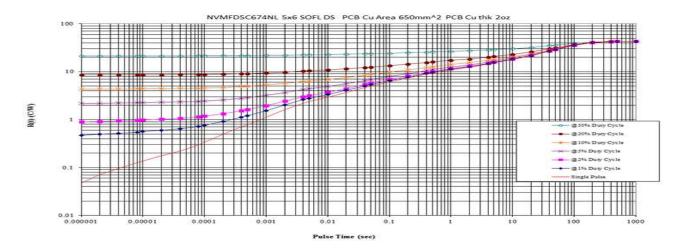


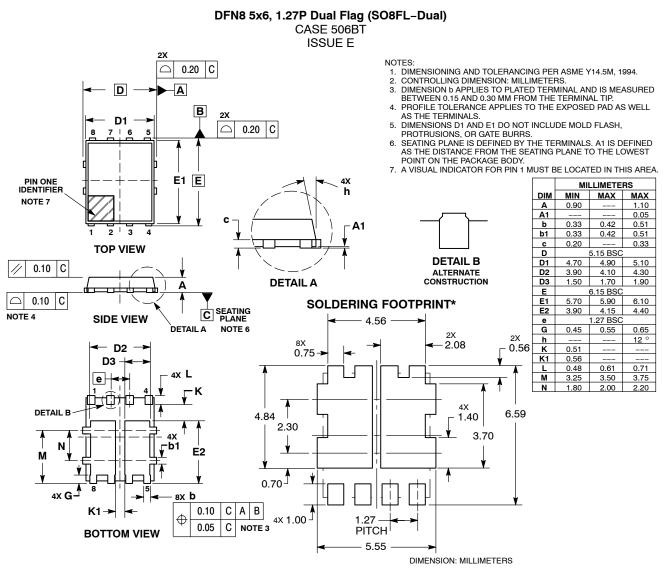
Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMFD5C674NLT1G	5C674L	DFN8 (Pb–Free)	1500 / Tape & Reel
NVMFD5C674NLWFT1G	674LWF	DFN8 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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