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NVTFS4C05N

Power MOSFET

30 V, 3.6 mΩ, 102 A, Single N-Channel, μ8FL

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- NVTFS4C05NWF – Wettable Flanks Product
- NVT Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit			
Drain-to-Source Voltage	V_{DSS}	30	V			
Gate-to-Source Voltage	V_{GS}	± 20	V			
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 4)	Steady State	$T_A = 25^\circ\text{C}$	I_D	22	A	
		$T_A = 100^\circ\text{C}$		15.7		
		$T_A = 25^\circ\text{C}$	P_D		3.2	W
					1.6	
		$T_C = 25^\circ\text{C}$	I_D		102	A
					72	
Power Dissipation $R_{\psi JC}$ (Notes 1, 3, 4)	Steady State	$T_C = 25^\circ\text{C}$	P_D	68	W	
		$T_C = 100^\circ\text{C}$		34		
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	433	A		
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to +175		$^\circ\text{C}$		
Source Current (Body Diode)	I_S	65		A		
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}, V_{GS} = 10 \text{ V}, I_L = 18.8 \text{ A}, L = 0.5 \text{ mH}$)	E_{AS}	88		mJ		
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260		$^\circ\text{C}$		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) (Notes 1, 3)	$R_{\psi JC}$	2.2	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Notes 1, 2)	$R_{\theta JA}$	47	

1. The entire application environment impacts the thermal resistance values shown; they are not constants and are valid for the specific conditions noted.
2. Surface-mounted on FR4 board using 650 mm², 2 oz. Cu Pad.
3. Assumes heat-sink sufficiently large to maintain constant case temperature independent of device power.
4. Continuous DC current rating. Maximum current for pulses as long as one second is higher but dependent on pulse duration and duty cycle.

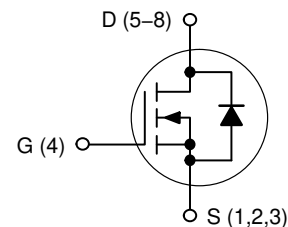


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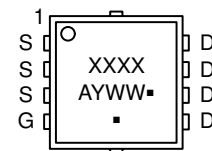
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
30 V	3.6 mΩ @ 10 V	102 A
	5.1 mΩ @ 4.5 V	

N-Channel MOSFET



MARKING DIAGRAM



- 4C05 = Specific Device Code for NVMTS4C05N
- 05WF = Specific Device Code of NVTFS4C05NWF
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NVTFS4C05N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			11.7		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 24 V			1.0	μA
		T _J = 25°C T _J = 125°C			10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.3		2.2	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-5.0		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 30 A	2.9	3.6	mΩ
		V _{GS} = 4.5 V	I _D = 30 A	4.1	5.1	
Forward Transconductance	g _{FS}	V _{DS} = 1.5 V, I _D = 15 A		68		S
Gate Resistance	R _G	T _A = 25°C		1.0		Ω

CHARGES AND CAPACITANCES

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 15 V		1988		pF
Output Capacitance	C _{OSS}			1224		
Reverse Transfer Capacitance	C _{RSS}			71		
Capacitance Ratio	C _{RSS} /C _{ISS}	V _{GS} = 0 V, V _{DS} = 15 V, f = 1 MHz		0.036		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 15 V; I _D = 30 A		14.5		nC
Threshold Gate Charge	Q _{G(TH)}			2.9		
Gate-to-Source Charge	Q _{GS}			5.2		
Gate-to-Drain Charge	Q _{GD}			5.5		
Gate Plateau Voltage	V _{GP}			3.1		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 15 V; I _D = 30 A		31		nC

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 4.5 V, V _{DS} = 15 V, I _D = 15 A, R _G = 3.0 Ω		11		ns
Rise Time	t _r			30		
Turn-Off Delay Time	t _{d(OFF)}			20		
Fall Time	t _f			8.0		
Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 15 V, I _D = 15 A, R _G = 3.0 Ω		8.0		ns
Rise Time	t _r			25		
Turn-Off Delay Time	t _{d(OFF)}			26		
Fall Time	t _f			5.0		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 10 A	T _J = 25°C T _J = 125°C	0.77 0.62	1.1	V
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 30 A		42.4		ns
Charge Time	t _a			21.1		
Discharge Time	t _b			21.3		
Reverse Recovery Charge	Q _{RR}			34.4		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

NVTFS4C05N

TYPICAL CHARACTERISTICS

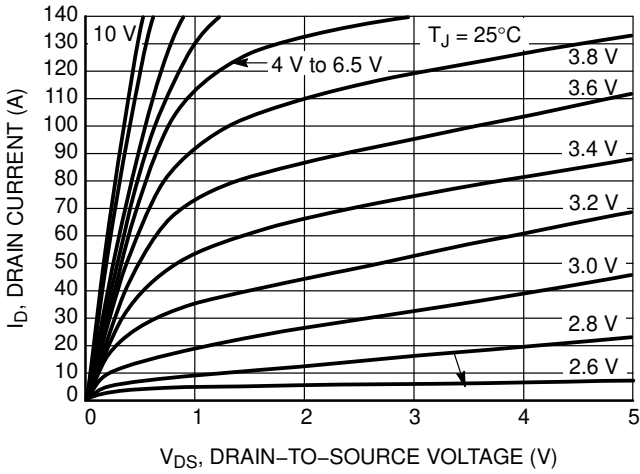


Figure 1. On-Region Characteristics

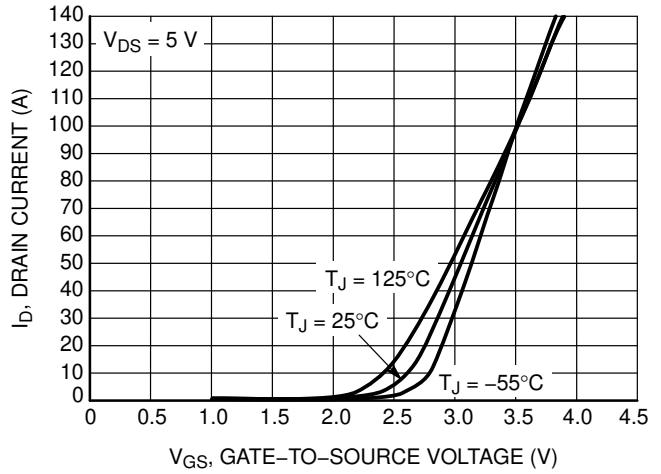


Figure 2. Transfer Characteristics

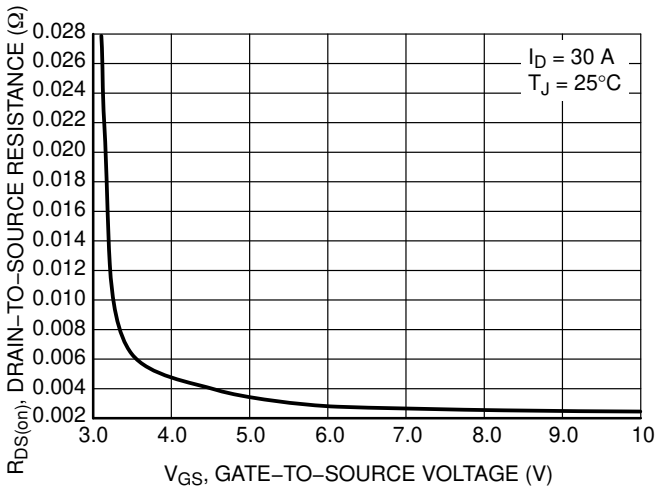


Figure 3. On-Resistance vs. V_{GS}

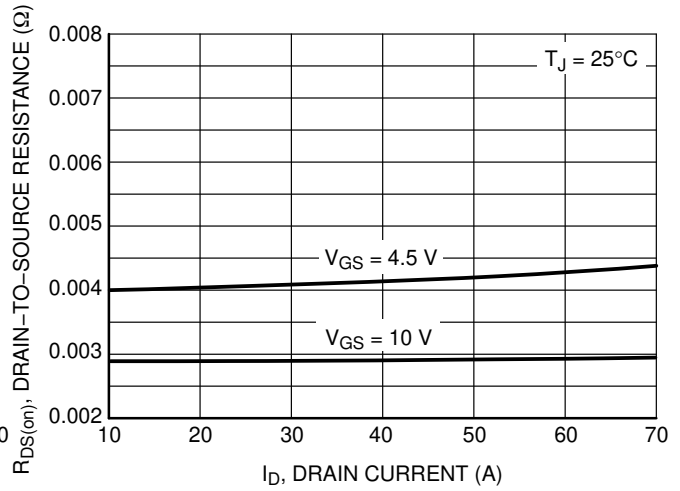


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

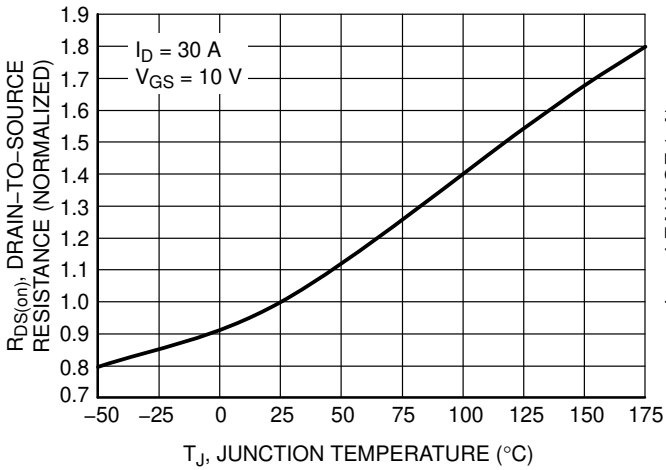


Figure 5. On-Resistance Variation with Temperature

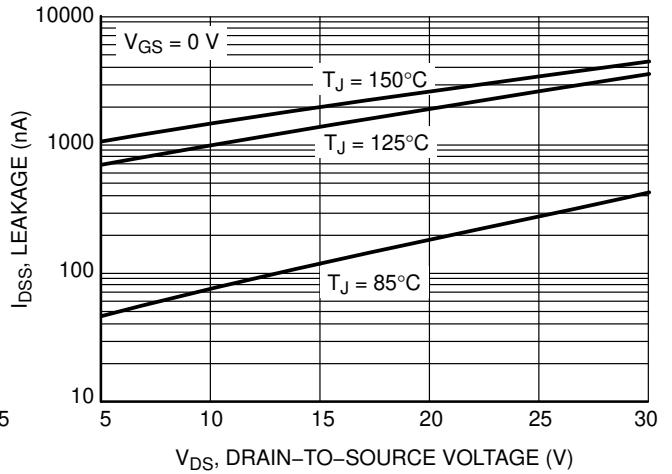


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NVTFS4C05N

TYPICAL CHARACTERISTICS

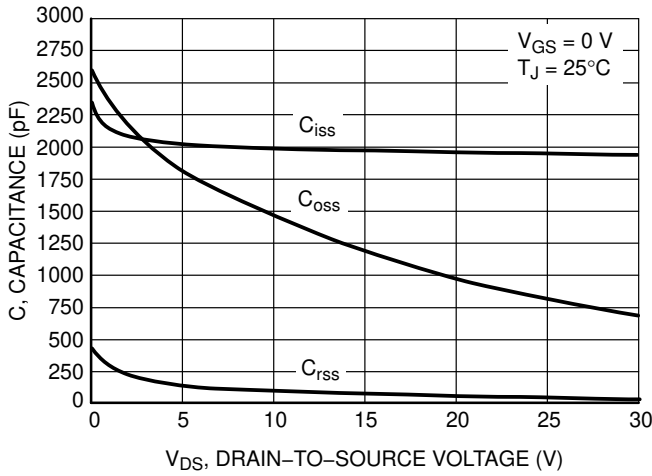


Figure 7. Capacitance Variation

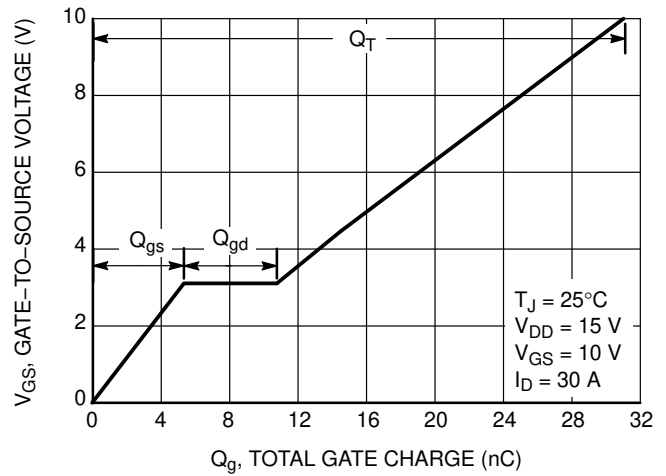


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

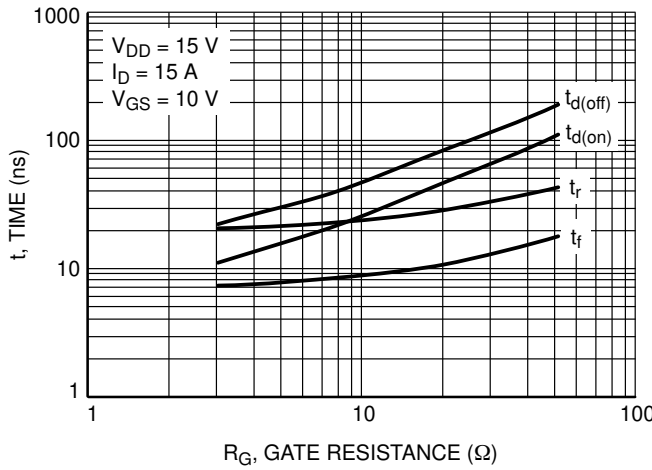


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

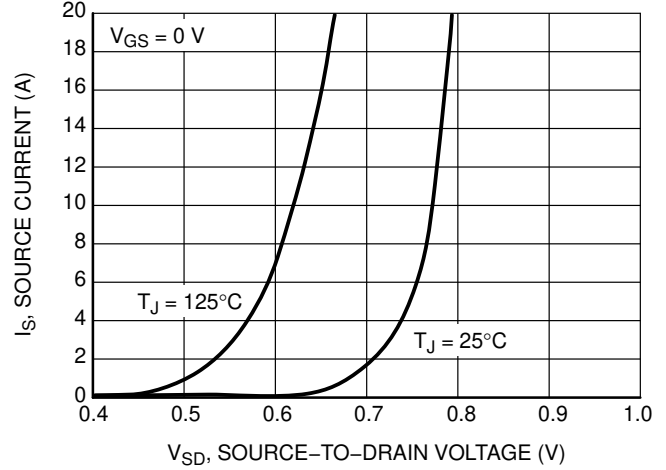


Figure 10. Diode Forward Voltage vs. Current

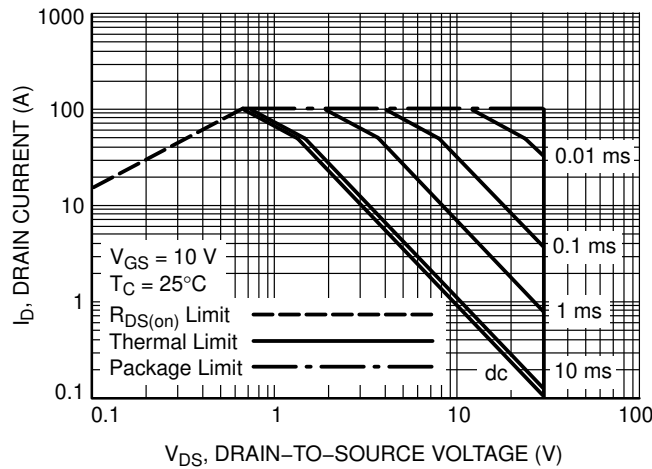


Figure 11. Maximum Rated Forward Biased Safe Operating Area

NVTFS4C05N

TYPICAL CHARACTERISTICS

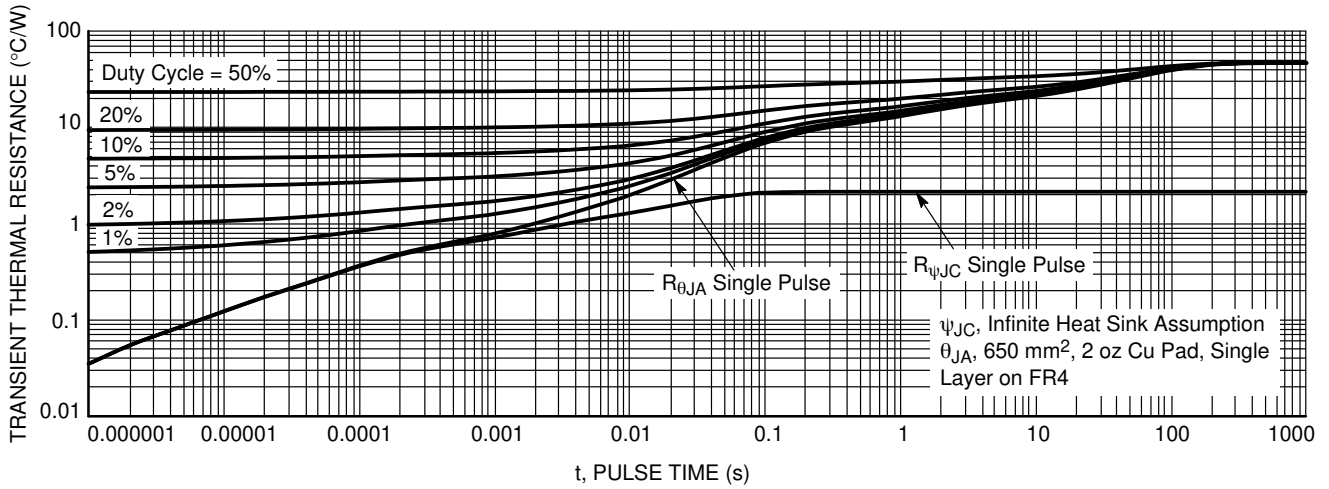


Figure 12. Thermal Response

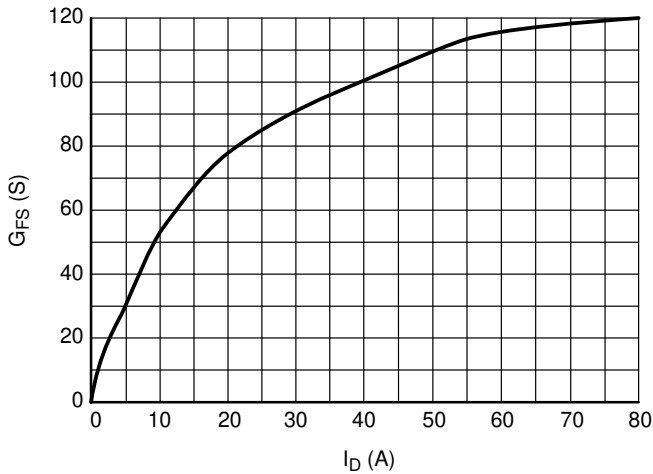


Figure 13. G_{FS} vs. I_D

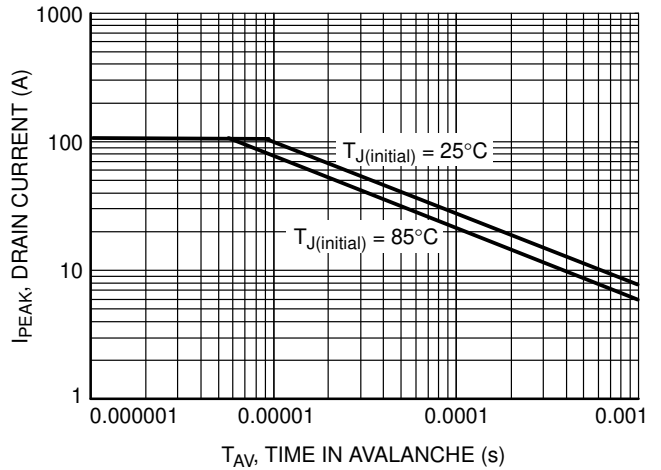


Figure 14. Avalanche Characteristics

ORDERING INFORMATION

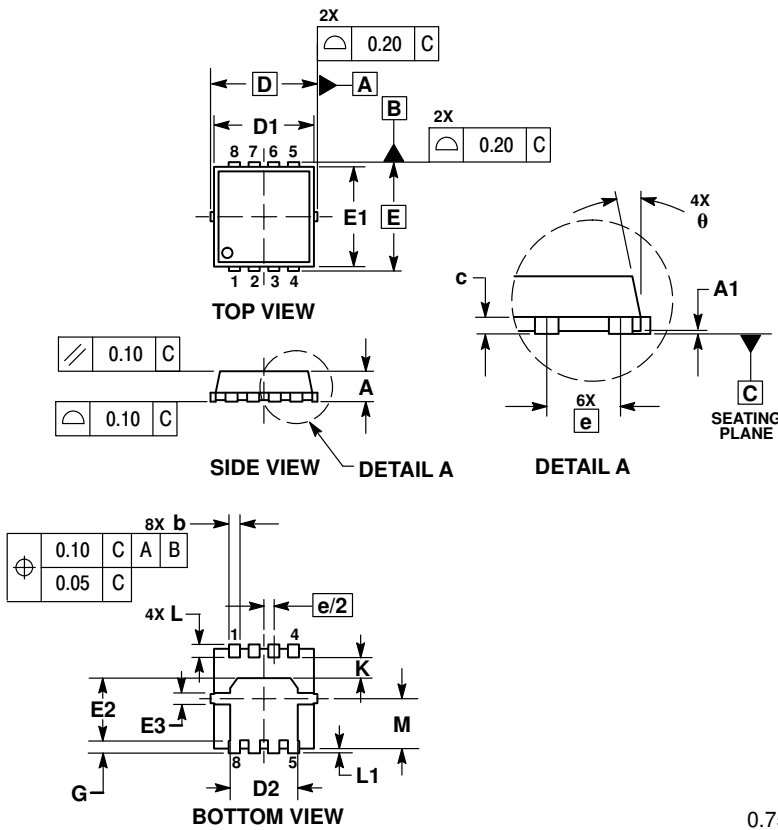
Device	Package	Shipping†
NVTFS4C05NTAG	WDFN8 (Pb-Free)	1500 / Tape & Reel
NVTFS4C05NWFTAG	WDFN8 (Pb-Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NVTF54C05N

PACKAGE DIMENSIONS

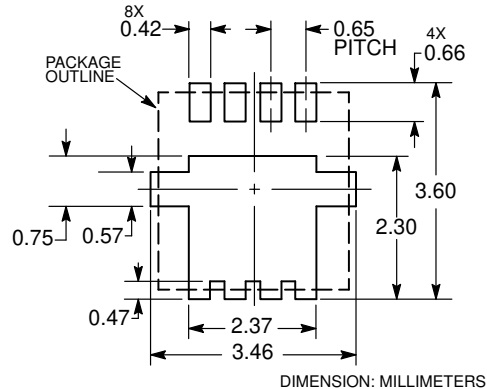
WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0°	---	12°	0°	---	12°

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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