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NX2305

SINGLE SUPPLY 12V SYNCHRONOUS PWM CONTROLLER WITH NMOS LDO CONTROLLER, POWER GOOD & ENABLES

PRELIMINARY DATA SHEET

Pb Free Product

DESCRIPTION

The NX2305 controller IC is a combination synchronous Buck and LDO controller IC designed to convert single 12V supply to low cost dual on board supply applications. The synchronous controller is used for high current high efficiency step down DC to DC converter applications while the LDO controller in conjunction with an external low cost N ch MOSFET can be used as a very low drop out regulator in applications such as converting 3.3V to 2.5V output. Internal UVLO keeps both regulators off until the supply voltage exceeds 9V where independent internal digital soft starts get initiated to ramp up both outputs.The switching section has hiccup current limit by sensing the Rdson of synchronous MOSFET. The LDO controller has Feedback Under Voltage Lock Out as a short circuit protection.Other features includes: 12V gate drive capability , Adaptive dead band control, Power good flag for the switcher controller and separate Enable pins for independent power sequencing.

FEATURES

- 12V PWM controller plus LDO controller
- Hiccup current limit by sensing Rdson of MOSFET
- 12V high side and low side driver
- Fixed internal 300kHz for switching controller
- Dual Independent Digital Soft Start Function
- Adaptive Deadband Control
- Enable pin available to program the Vbus UVLO
- Shut Down switching and LDO via pulling down EnSW or ENLDO pins
- Pb-free and RoHS compliant

APPLICATIONS

- PCI Graphic Card on board converters
- Mother board On board DC to DC applications
- On board Single Supply 12V DC to DC such as 12V to 3.3V, 2.5V or 1.8V
- Set Top Box and LCD Display

TYPICAL APPLICATION

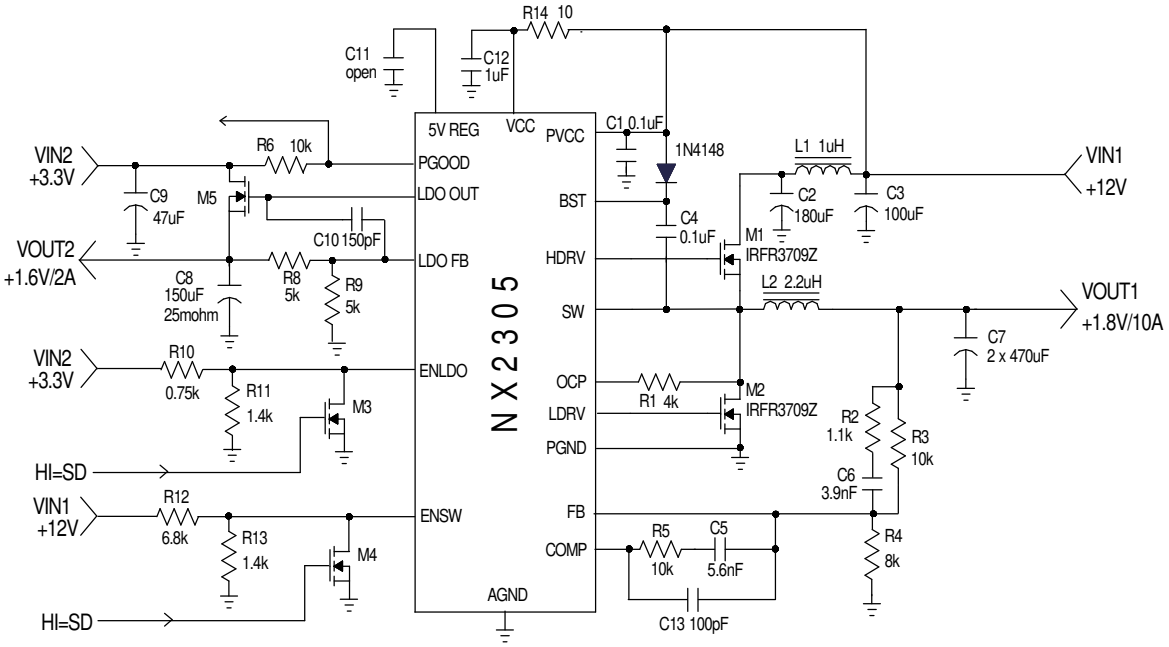

Figure1 - Typical application of NX2305

ORDERING INFORMATION

Device	Temperature	Package	Frequency	Pb-Free
NX2305CMTR	0 to 70°C	MLPQ-16L	300kHz	Yes
NX2305CSTR	0 to 70°C	SOIC -16L	300kHz	Yes

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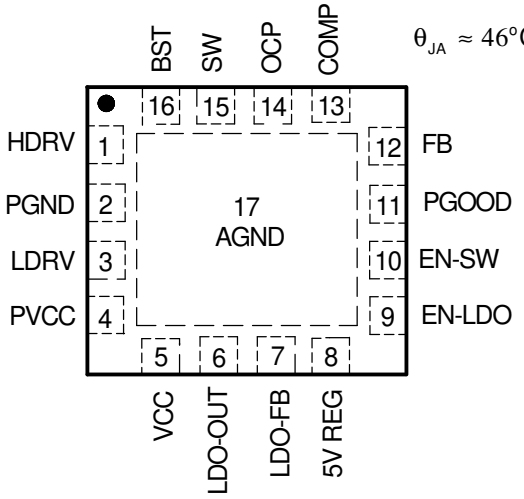
ABSOLUTE MAXIMUM RATINGS

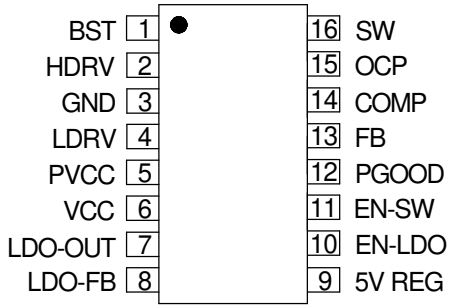
Vcc to PGND & BST to SW voltage ..... -0.3V to 16V
BST to PGND Voltage ..... -0.3V to 35V
SW to PGND ..... -2V to 35V
All other pins ..... -0.3V to 6.5V
Storage Temperature Range ..... -65°C to 150°C
Operating Junction Temperature Range ..... -40°C to 125°C

CAUTION: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

PACKAGE INFORMATION

16-LEAD PLASTIC MLPQ	16-LEAD PLASTIC SOIC
$\theta_{JA} \approx 46°C/W$	$\theta_{JA} \approx 83°C/W$





ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc =12V, V_{BST}-V_{SW}=12V, ENSW=ENLDO=3V, and T_A = 0 to 70°C. Typical values refer to T_A = 25°C.

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Reference Voltage						
Ref Voltage	V_{REF}			0.8		V
Ref Voltage line regulation		10V<=Vcc<=14V		0.2		%
Supply Voltage(Vcc&V_{BST})						
V_{CC} Voltage Range	V_{CC}		8.2		14	V
V_{CC} Supply Current (Static)	I_{CC} (Static)	ENSW=LOW ENLDO=LOW		8		mA
PV_{CC} Supply Current (Dynamic)	I_{CC} (Dynamic)	C_L=3300pF		8.5		mA
V_{BST} Voltage Range	V_{BST} to V_{SW}		8.2		14	V
V_{BST} Supply Current(Static)	V_{BST} (Static)	ENSW=LOW ENLDO=LOW		0.2		mA

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PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
V_{BST} Supply Current (Dynamic)	V_{BST} (dynamic)	C_L=3300PF		9.2		mA
Under Voltage Lockout						
V_{CC}-Threshold	V_{CC}_UVLO	V_{CC} Rising (NOTE1)		6.8		V
V_{CC} hysterises		V_{CC} Falling (NOTE1)		300		mV
Oscillator (Rt)						
Frequency	F_S			300		KHz
Ramp-Amplitude Voltage	V_{RAMP}			1.1		V
Max Duty Cycle				94		%
Min duty Cycle					0	%
Error Amplifiers						
Open Loop Gain			50	65		dB
Transconductance	gm			2000		umho
Comp SD threshold				0.2		V
Input Bias Current	Ib				100	nA
EN & SS						
Soft Start time	Tss			6.8		mS
Enable HI Threshold	V_{ENTHH}			1.24		V
Enable Hysterises	V_{ENTHL}			30		mV
High Side Driver, Hdrv, BST, SW (C_L=3300pF)						
Output Impedance , Sourcing Current	R_{source}(Hdrv)	I=200mA		3.6		ohm
Output Impedance , Sinking Current	R_{sink}(Hdrv)	I=200mA		1		ohm
Rise Time	THdrv(Rise)	10% to 90%		30		ns
Fall Time	THdrv(Fall)	90% to 10%		20		ns
Deadband Time	Tdead(L to H)	Ldrv going Low to Hdrv going High, 10% to 10%		50		ns
Low Side Driver , Ldrv, PVcc, Pgnd(C_L=3300pF)						
Output Impedance, Sourcing Current	R_{source}(Ldrv)	I=200mA		2.2		ohm
Output Impedance, Sinking Current	R_{sink}(Ldrv)	I=200mA		1		ohm
Rise Time	TLdrv(Rise)	10% to 90%		30		ns
Fall Time	TLdrv(Fall)	90% to 10%		20		ns
Deadband Time	Tdead(H to L)	SW going Low to Ldrv going High, 10% to 10%		50		ns
LDO Controller						
FB Pin- Bias Current					1	uA
High Output Voltage				11.1		V
Low Output Voltage				0.2		V
High Output Source Current				1.9		mA

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PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Open Loop Gain		GBNT(Note 2)	50			dB
FB Under Voltage trip point				50		%
Power Good(Pgood) Threshold Voltage as % of Vref		FB ramping up		90		%
Hysteresis				5		%
OCP Adjust OCP Current Setting				40		uA

NOTE1: VCC is connected to ENSW pin via a resistor divider. In VCC UVLO test, ENSW pin is open.
NOTE2: This parameter is guaranteed by design but not tested in production(GBNT).

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PIN DESCRIPTIONS

PIN SYMBOL	PIN DESCRIPTION
VCC	IC's supply voltage. This pin biases the internal logic circuits. A high freq 1uF ceramic capacitor is placed as close as possible to and connected to this pin and ground pin. The maximum rating of this pin is 16V.
BST	This pin supplies voltage to high side FET driver. A high freq 0.1uF ceramic capacitor is placed as close as possible to and connected to these pins and SW pin.
ENLDO	A resistor divider is connected from the LDO bus voltage to this pin that holds off the LDO soft start until this threshold is reached. An external low cost MOSFET can be connected to this pin for external enable control.
ENSW	A resistor divider is connected from the respective switcher BUS voltage to this pin that holds off the controller's soft start until this threshold is reached. An external low cost MOSFET can be connected to this pin for external enable control.
FB	This pin is the error amplifier inverting input. This pin is connected via resistor divider to the output of the switching regulator to set the output DC voltage.
COMP	This pin is the output of error amplifier and is used to compensate the voltage control feedback loop.
OCP	This pin is connected to the drain of the external low side MOSFET and is the input of the over current protection(OCP) comparator. An internal current source 40uA is flown to the external resistor which sets the OCP voltage across the Rdson of the low side MOSFET. Current limit point is this voltage divided by the Rds-on. Once this threshold is reached the Hdrv and Ldrv pins are switched low and an internal hiccup circuit is set that recycles the soft start circuit after 2048 switching cycles.
SW	This pin is connected to source of high side FET and provides return path for the high side driver. It is also used to hold the low side driver low until this pin is brought low by the action of high side turning off. LDRV can only go high if SW is below 1V threshold .
HDRV	High side gate driver output.
LDRV	Low side gate driver output.
PVCC	Supply voltage for the low side fet driver. A high frequency 1uF ceramic cap must be connected from this pin to the PGND pin as close as possible.
LDO_FB	LDO controller feedback input. This pin is connected via resistor divider to the output of the switching regulator to set the output DC voltage.If the LDOFB pin is pulled below 0.4V, an internal comparator after a delay pulls down LDOOUT pin and initiates the HICCUP circuitry. During the startup this latch is not activated, allowing the LDOFB pin to come up and follow the soft started Vref voltage.
LDO_OUT	LDO controller output. This pin is controlling the gate of an external NCH MOSFET. The maximum rating of this pin is 16V.
5V REG	Output of an internal 5V regulator.

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PIN SYMBOL	PIN DESCRIPTION
PGOOD	An open drain output that requires a pull up resistor to Vcc or a voltage lower than Vcc. When FB pin reaches 90% of the reference voltage PGOOD transitions from LO to HI state.
PGND	Power ground pin for low side driver. In SOIC16 package, PGND and AGND are combined together called GND.
AGND	Analog ground. In MLPD16 package, pad is AGND.

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BLOCK DIAGRAM

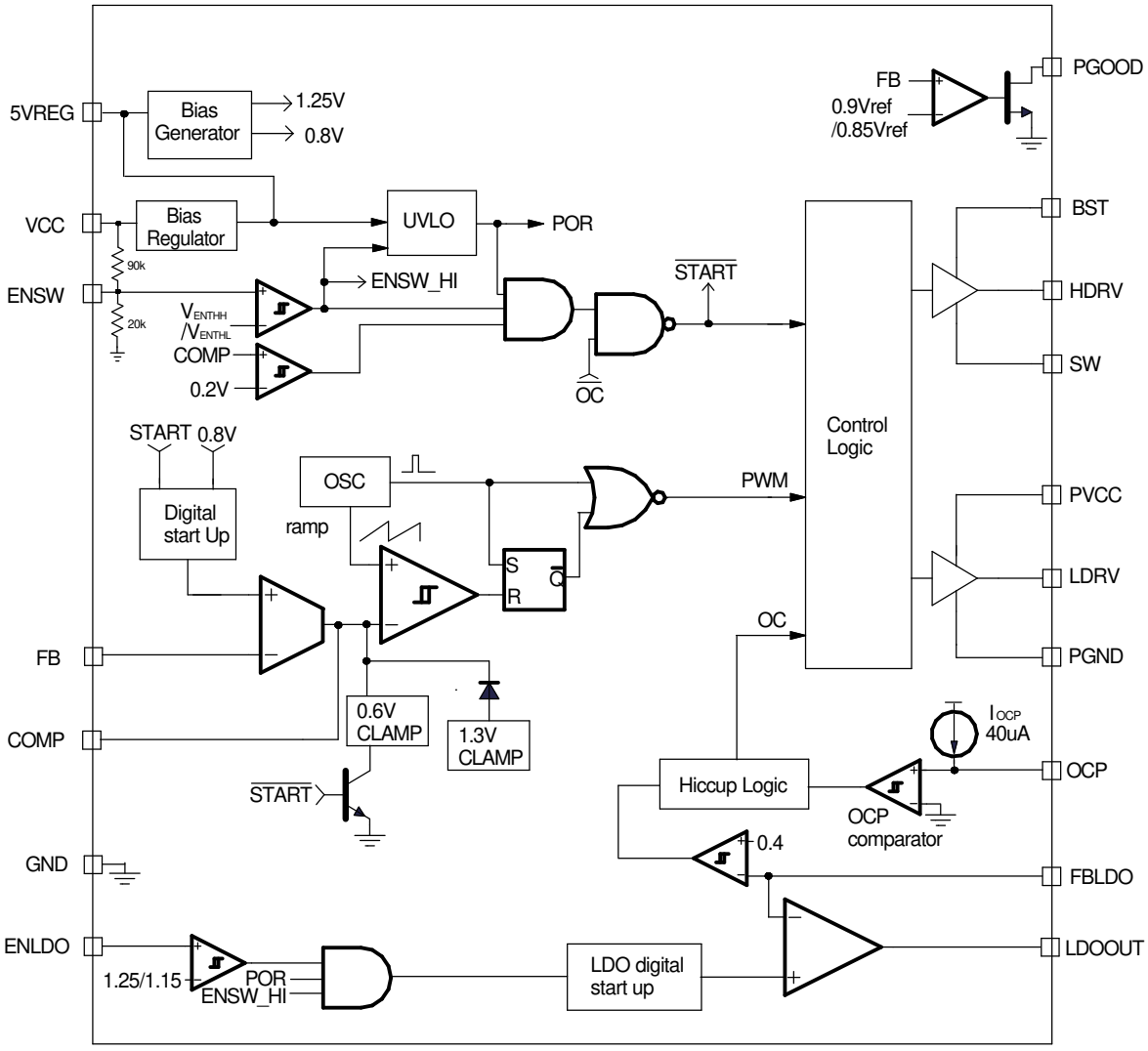

Figure 2 - Simplified block diagram of the NX2305

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APPLICATION INFORMATION

Symbol Used In Application Information:

V_{IN} - Input voltage
V_{OUT} - Output voltage
I_{OUT} - Output current
ΔV_{RIPPLE} - Output voltage ripple
F_S - Switching frequency
ΔI_{RIPPLE} - Inductor current ripple

Design Example

Power stage design requirements:
V_{IN}=12V
V_{OUT}=1.8V
I_{OUT}=10A
ΔV_{RIPPLE} <=20mV
ΔV_{TRAN}<=100mV @ 10A step
F_S=300kHz

Output Inductor Selection

The selection of inductor value is based on inductor ripple current, power rating, working frequency and efficiency. Larger inductor value normally means smaller ripple current. However if the inductance is chosen too large, it brings slow response and lower efficiency. Usually the ripple current ranges from 20% to 40% of the output current. This is a design freedom which can be decided by design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT}=\frac{V_{IN}-V_{OUT}}{I_{RIPPLE}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S} \quad ...(1)$$

$$I_{RIPPLE}=k\times I_{OUTPUT}$$

where k is between 0.2 to 0.4.
Select k=0.3, then

$$L_{OUT}=\frac{12V-1.8V}{0.3\times 10A}\times\frac{1.8V}{12V}\times\frac{1}{300kHz}$$

L_{OUT}=1.7uH

Choose L_{OUT}=2.2uH, then coilcraft inductor DO5010P-222HC is a good choice.

Current Ripple is calculated as

$$I_{RIPPLE}=\frac{V_{IN}-V_{OUT}}{L_{OUT}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S}$$
$$=\frac{12V-1.8V}{2.2uH}\times\frac{1.8V}{12V}\times\frac{1}{300kHz}=2.3A \quad ...(2)$$

Output Capacitor Selection

Output capacitor is basically decided by the amount of the output voltage ripple allowed during steady state(DC) load condition as well as specification for the load transient. The optimum design may require a couple of iterations to satisfy both condition.

Based on DC Load Condition

The amount of voltage ripple during the DC load condition is determined by equation(3).

$$\Delta V_{RIPPLE}=ESR\times\Delta I_{RIPPLE}+\frac{\Delta I_{RIPPLE}}{8\times F_S\times C_{OUT}} \quad ...(3)$$

Where ESR is the output capacitors' equivalent series resistance,C_{OUT} is the value of output capacitors.

Typically when large value capacitors are selected such as Aluminum Electrolytic,POSCAP and OSCON types are used, the amount of the output voltage ripple is dominated by the first term in equation(3) and the second term can be neglected.

For this example, POSCAP are chosen as output capacitors, the ESR and inductor current typically determines the output voltage ripple.

$$ESR_{desire}=\frac{\Delta V_{RIPPLE}}{\Delta I_{RIPPLE}}=\frac{20mV}{2.3A}=8.7m\Omega \quad ...(4)$$

If low ESR is required, for most applications, multiple capacitors in parallel are better than a big capacitor. For example, for 20mV output ripple, POSCAP 2R5TPE470M9 with 9mΩ are chosen.

$$N=\frac{ESR_E\times\Delta I_{RIPPLE}}{\Delta V_{RIPPLE}} \quad ...(5)$$

Number of Capacitor is calculated as

$$N=\frac{9m\Omega\times 2.3A}{20mV}$$

N =1.03

The number of capacitor has to be round up to a integer. Choose N =2.

If ceramic capacitors are chosen as output capacitors, both terms in equation (3) need to be evaluated to determine the overall ripple. Usually when this type of capacitors are selected, the amount of capacitance per single unit is not sufficient to meet the transient specification, which results in parallel configuration of multiple capacitors.

For example, one 100uF, X5R ceramic capacitor with $2m\Omega$ ESR is used. The amount of output ripple is

$$\Delta V_{RIPPLE} = 2m\Omega \times 2.3A + \frac{2.3A}{8 \times 300kHz \times 100uF}$$
$$= 4.6mV + 9.6mV = 14.2mV$$

Although this meets DC ripple spec, however it needs to be studied for transient requirement.

Based On Transient Requirement

Typically, the output voltage droop during transient is specified as

$\Delta V_{droop} < \Delta V_{tran}$ @step load ΔI_{STEP}

During the transient, the voltage droop during the transient is composed of two sections. One section is dependent on the ESR of capacitor, the other section is a function of the inductor, output capacitance as well as input, output voltage. For example, for the overshoot when load from high load to light load with a ΔI_{STEP} transient load, if assuming the bandwidth of system is high enough, the overshoot can be estimated as the following equation.

$$\Delta V_{overshoot} = ESR \times \Delta I_{step} + \frac{V_{OUT}}{2 \times L \times C_{OUT}} \times \tau^2 \quad ...(6)$$

where τ is the a function of capacitor,etc.

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \frac{L \times \Delta I_{step}}{V_{OUT}} - ESR \times C_{OUT} & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(7)$$

where

$$L_{crit} = \frac{ESR \times C_{OUT} \times V_{OUT}}{\Delta I_{step}} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} \quad ...(8)$$

where ESR_E and C_E represents ESR and capacitance of each capacitor if multiple capacitors are used in parallel.

The above equation shows that if the selected output inductor is smaller than the critical inductance, the voltage droop or overshoot is only dependent on the ESR of output capacitor. For low frequency capacitor such as electrolytic capacitor, the product of ESR and capacitance is high and $L \le L_{crit}$ is true. In that case, the transient spec is mostly like to dependent on the ESR of capacitor.

Most case, the output capacitor is multiple capacitor in parallel. The number of capacitor can be calculated by the following

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2 \quad ...(9)$$

where

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \frac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(10)$$

For example, assume voltage droop during transient is 100mV for 10A load step.

If the POSCAP 2R5TPE470M9 (470uF, 9mohm ESR) is used, the crticial inductance is given as

$$L_{crit} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} =$$
$$\frac{9m\Omega \times 470\mu F \times 1.8V}{10A} = 0.76\mu H$$

The selected inductor is 2.2uH which is bigger than critical inductance. In that case, the output voltage transient not only dependent on the ESR, but also capacitance.

number of capacitor is

$$\tau = \frac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E$$
$$= \frac{2.2\mu H \times 10A}{1.8V} - 9m\Omega \times 470\mu F = 7.97us$$

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2$$
$$= \frac{9m\Omega \times 10A}{100mV} + \frac{1.8V}{2 \times 2.2\mu H \times 470\mu F \times 100mV} \times (7.97us)^2$$
$$= 1.44$$

The number of capacitors has to satisfied both ripple and transient requirement. Overall, we choose N=2.

It should be considered that the proposed equation is based on ideal case, in reality, the droop or overshoot is typically more than the calculation. The equation gives a good start. For more margin, more capacitors have to be chosen after the test. Typically, for high frequency capacitor such as high quality POSCAP especially ceramic capacitor, 20% to 100% (for ceramic) more capacitors have to be chosen since the ESR of capacitors is so low that the PCB parasitic can affect the results tremendously. More capacitors have to be selected to compensate these parasitic parameters.

Compensator Design

Due to the double pole generated by LC filter of the power stage, the power system has 180° phase shift , and therefore, is unstable by itself. In order to achieve accurate output voltage and fast transient response, compensator is employed to provide highest possible bandwidth and enough phase margin. Ideally, the Bode plot of the closed loop system has crossover frequency between 1/10 and 1/5 of the switching frequency, phase margin greater than 50° and the gain crossing 0dB with -20dB/decade. Power stage output capacitors usually decide the compensator type. If electrolytic capacitors are chosen as output capacitors, type II compensator can be used to compensate the system, because the zero caused by output capacitor ESR is lower than crossover frequency. Otherwise type III compensator should be chosen.

A. Type III compensator design

For low ESR output capacitors, typically such as Sanyo oscap and poscap, the frequency of ESR zero caused by output capacitors is higher than the crossover frequency. In this case, it is necessary to compensate the system with type III compensator. The following figures and equations show how to realize the type III compensator by transconductance amplifier.

$$F_{Z1} = \frac{1}{2\times\pi\times R_4\times C_2} \quad ...(11)$$

$$F_{Z2} = \frac{1}{2\times\pi\times(R_2+R_3)\times C_3} \quad ...(12)$$

$$F_{P1} = \frac{1}{2\times\pi\times R_3\times C_3} \quad ...(13)$$

$$F_{P2} = \frac{1}{2\times\pi\times R_4\times\frac{C_1\times C_2}{C_1+C_2}} \quad ...(14)$$

where F_{Z1},F_{Z2},F_{P1} and F_{P2} are poles and zeros in the compensator.

The transfer function of type III compensator for transconductance amplifier is given by:

$$\frac{V_e}{V_{OUT}} = \frac{1-g_m\times Z_f}{1+g_m\times Z_{in}+Z_{in}/R_1}$$

For the voltage amplifier, the transfer function of compensator is

$$\frac{V_e}{V_{OUT}} = \frac{-Z_f}{Z_{in}}$$

To achieve the same effect as voltage amplifier, the compensator of transconductance amplifier must satisfy this condition: R4>>2/gm. And it would be desirable if R1||R2||R3>>1/gm can be met at the same time.

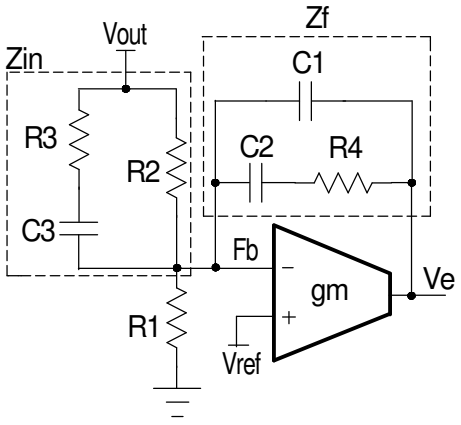

Figure 3 - Type III compensator using transconductance amplifier

Case 1: $F_{LC}<F_O<F_{ESR}$

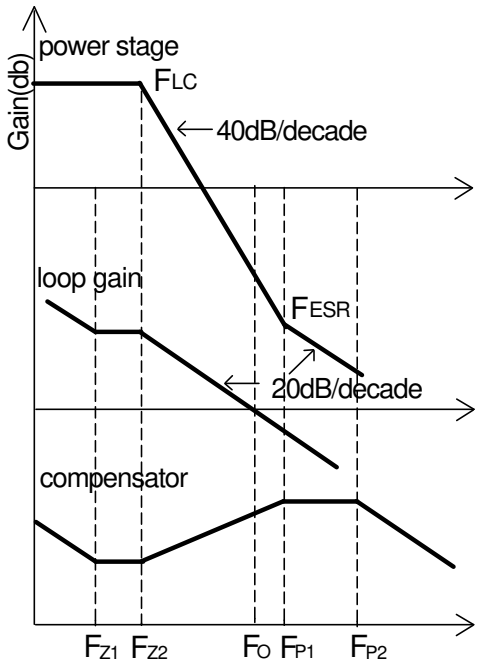

Figure 4 - Bode plot of Type III compensator ($F_{LC}<F_O<F_{ESR}$)

Typical design example of type III compensator in which the crossover frequency is selected as $F_{LC}<F_O<F_{ESR}$ and $F_O<=1/10\sim1/5F_s$ is shown as the following steps.

1. Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC}=\frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}=\frac{1}{2\times\pi\times\sqrt{2.2uH\times940uF}}=3.5kHz$$

$$F_{ESR}=\frac{1}{2\times\pi\times ESR\times C_{OUT}}=\frac{1}{2\times\pi\times4.5m\Omega\times940uF}=37.6kHz$$

2. Set R_2 equal to 10kΩ.

$$R_1=\frac{R_2\times V_{REF}}{V_{OUT}-V_{REF}}=\frac{10k\Omega\times0.8V}{1.8V-0.8V}=8k\Omega$$

Choose R_1=8kΩ.

3. Set zero $F_{Z2}=F_{LC}$ and $F_{p1}=F_{ESR}$.

4. Calculate R_4 and C_3 with the crossover frequency at 1/10~ 1/5 of the switching frequency. Set F_O=25kHz.

$$C_3=\frac{1}{2\times\pi\times R_2}\times\left(\frac{1}{F_{z2}}-\frac{1}{F_{p1}}\right)=\frac{1}{2\times\pi\times10k\Omega}\times\left(\frac{1}{3.5kHz}-\frac{1}{37.6kHz}\right)=4.1nF$$

$$R_4=\frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L}{C_3}\times C_{out}=\frac{1.1V}{12V}\times\frac{2\times\pi\times25kHz\times2.2uH}{3.9nF}\times940uF=10.4k\Omega$$

Choose C_3=3.9nF, R_4=10.2k.

5. Calculate C_2 with zero F_{z1} at 75% of the LC double pole by equation (11).

$$C_2=\frac{1}{2\times\pi\times F_{Z1}\times R_4}=\frac{1}{2\times\pi\times0.75\times3.5kHz\times10.2k\Omega}=5.95nF$$

Choose C_2=5.6nF.

6. Calculate C_1 by equation (14) with pole F_{p2} at half the switching frequency.

$$C_1=\frac{1}{2\times\pi\times R_4\times F_{P2}}=\frac{1}{2\times\pi\times10.2k\Omega\times150kHz}=104pF$$

Choose C_1=100pF.

7. Calculate R_3 by equation (13).

$$R_3=\frac{1}{2\times\pi\times F_{P1}\times C_3}=\frac{1}{2\times\pi\times37.6kHz\times3.9nF}=1.1k\Omega$$

Choose R_3=1.1kΩ.

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Case 2: $F_{LC}<F_{ESR}<F_O$

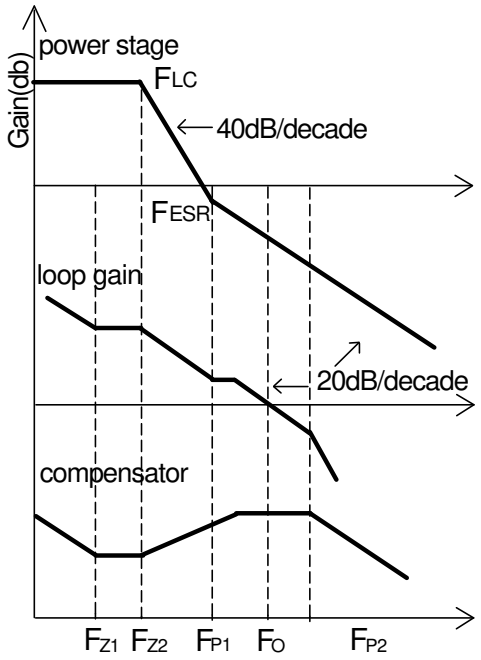

Figure 5 - Bode plot of Type III compensator ($F_{LC}<F_{ESR}<F_O$)

If electrolytic capacitors are used as output capacitors, typical design example of type III compensator in which the crossover frequency is selected as $F_{LC}<F_{ESR}<F_O$ and $F_O<=1/10\sim1/5F_s$ is shown as the following steps. Here one SANYO MV-WG1500 with 13 mΩ is chosen as output capacitor.

1. Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC}=\frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}=\frac{1}{2\times\pi\times\sqrt{2.2uH\times1500uF}}=2.77kHz$$

$$F_{ESR}=\frac{1}{2\times\pi\times ESR\times C_{OUT}}=\frac{1}{2\times\pi\times13m\Omega\times1500uF}=8.16kHz$$

2. Set R_2 equal to 15kΩ.

$$R_1=\frac{R_2\times V_{REF}}{V_{OUT}-V_{REF}}=\frac{15k\Omega\times0.8V}{1.8V-0.8V}=12k\Omega$$

Choose R_1=12kΩ.

3. Set zero $F_{Z2}=F_{LC}$ and $F_{p1}=F_{ESR}$.

4. Calculate C_3.

$$C_3=\frac{1}{2\times\pi\times R_2}\times\left(\frac{1}{F_{z2}}-\frac{1}{F_{p1}}\right)=\frac{1}{2\times\pi\times15k\Omega}\times\left(\frac{1}{2.77kHz}-\frac{1}{8.16kHz}\right)=2.5nF$$

Choose C_3=2.7nF.

5. Calculate R_3.

$$R_3=\frac{1}{2\times\pi\times F_{P1}\times C_3}=\frac{1}{2\times\pi\times8.16kHz\times2.7nF}=7.22k\Omega$$

Choose R_3=7.32kΩ.

6. Calculate R_4 with F_O=30kHz.

$$R_4=\frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L}{ESR}\times\frac{R_2\times R_3}{R_2+R_3}=\frac{1.1V}{12V}\times\frac{2\times\pi\times30kHz\times2.2uH}{13m\Omega}\times\frac{15k\Omega\times7.32k\Omega}{15k\Omega+7.32k\Omega}=14.3k\Omega$$

Choose R_4=14.3kΩ.

5. Calculate C_2 with zero F_{z1} at 75% of the LC double pole by equation (11).

$$C_2=\frac{1}{2\times\pi\times F_{Z1}\times R_4}=\frac{1}{2\times\pi\times0.75\times2.77kHz\times14.3k\Omega}=3.9nF$$

Choose C_2=3.9nF.

6. Calculate C_1 by equation (14) with pole F_{p2} at half the switching frequency.

$$C_1=\frac{1}{2\times\pi\times R_4\times F_{P2}}=\frac{1}{2\times\pi\times14.3k\Omega\times150kHz}=74pF$$

Choose C_1=82pF.

B. Type II compensator design

If the electrolytic capacitors are chosen as power stage output capacitors, usually the Type II compensator can be used to compensate the system.

For this type of compensator, F_O has to satisfy $F_{LC}<F_{ESR}<<F_O<=1/10~1/5F_s$.

Case 1:

Type II compensator can be realized by simple RC circuit as shown in figure 7. R_3 and C_1 introduce a zero to cancel the double pole effect. C_2 introduces a pole to suppress the switching noise.

To achieve the same effect as voltage amplifier, the compensator of transconductance amplifier must satisfy this condition: $R_3>>1/gm$ and $R_1||R_2>>1/gm$. The following equations show the compensator pole zero location and constant gain.

$$Gain=\frac{R_3}{R_2} \quad \text{... (15)}$$

$$F_z=\frac{1}{2\times\pi\times R_3\times C_1} \quad \text{... (16)}$$

$$F_p \approx \frac{1}{2\times\pi\times R_3\times C_2} \quad \text{... (17)}$$

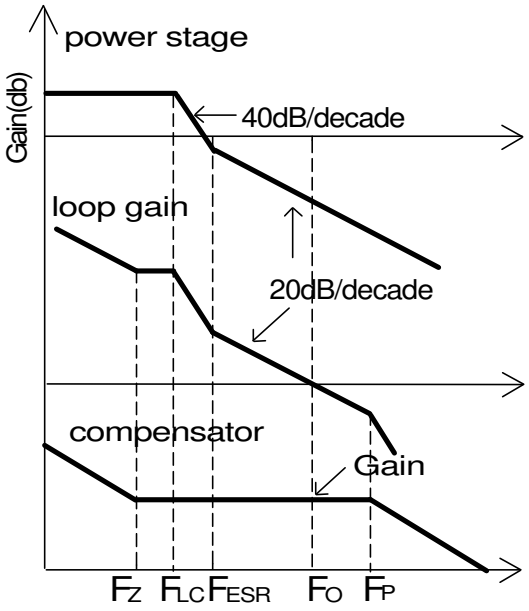

Figure 6 - Bode plot of Type II compensator

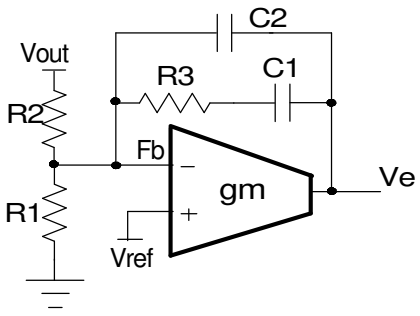

Figure 7 - Type II compensator with transconductance amplifier(case 1)

The following parameters are used as an example for type II compensator design, three 1500uF with 19mohm Sanyo electrolytic CAP 6MV1500WGL are used as output capacitors. Coilcraft DO5010P-152HC 1.5uH is used as output inductor. See figure 19. The power stage information is that:
V_{IN}=12V, V_{OUT}=1.2V, I_{OUT} =12A, F_S=300kHz.

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC}=\frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}$$
$$=\frac{1}{2\times\pi\times\sqrt{1.5uH\times 4500uF}}$$
$$=1.94kHz$$

$$F_{ESR}=\frac{1}{2\times\pi\times ESR\times C_{OUT}}$$
$$=\frac{1}{2\times\pi\times 6.33m\Omega\times 4500uF}$$
$$=5.6kHz$$

2.Set crossover frequency F_O=30kHz>>F_{ESR}.

3. Set R_2 equal to10kΩ. Based on output voltage, using equation 21, the final selection of R_1 is 20kΩ.

4.Calculate R_3 value by the following equation.

$$R_3=\frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L}{ESR}\times R_2$$
$$=\frac{1.1V}{12V}\times\frac{2\times\pi\times 30kHz\times 1.5uH}{6.33m\Omega}\times 10k\Omega$$
$$=37.2k\Omega$$

Choose R_3 =37.4kΩ.

5. Calculate C_1 by setting compensator zero F_Z at 75% of the LC double pole.

$$C_1=\frac{1}{2\times\pi\times R_3\times F_z}$$
$$=\frac{1}{2\times\pi\times 37.4k\Omega\times 0.75\times 1.94kHz}$$
$$=2.9nF$$

Choose C_1=2.7nF.

6. Calculate C_2 by setting compensator pole F_p at half the swithing frequency.

$$C_2=\frac{1}{\pi\times R_3\times F_s}$$
$$=\frac{1}{\pi\times 37.4k\Omega\times 150kHz}$$
$$=57pF$$

Choose C_2=56pF.

Case 2:

Type II compensator can also be realized by simple RC circuit without feedback as shown in figure 9. R3 and C1 introduce a zero to cancel the double pole effect. C2 introduces a pole to suppress the switching noise. The following equations show the compensator pole zero location and constant gain.

$$Gain=g_m\times\frac{R_1}{R_1+R_2}\times R_3 \quad \text{... (18)}$$

$$F_z=\frac{1}{2\times\pi\times R_3\times C_1} \quad \text{... (19)}$$

$$F_p\approx\frac{1}{2\times\pi\times R_3\times C_2} \quad \text{... (20)}$$

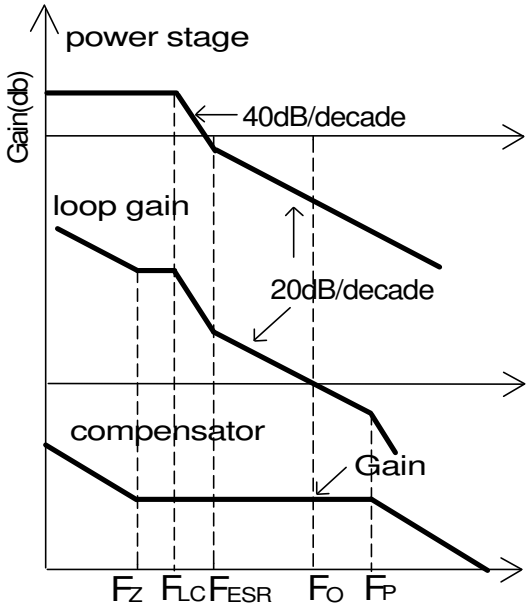

Figure 8 - Bode plot of Type II compensator

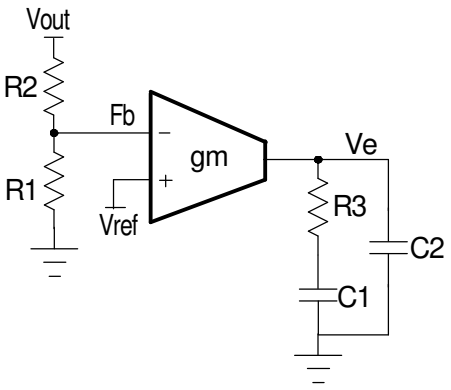

Figure 9 - Type II compensator with transconductance amplifier

For this type of compensator, F_O has to satisfy $F_{LC}<F_{ESR}<<F_O<=1/10\sim1/5F_s$.

The following is parameters for type II compensator design. Input voltage is 12V, output voltage is 3.3V, output inductor is 1.5uH, output capacitors are two 680uF with 41mΩ electrolytic capacitors.

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC} = \frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}$$
$$= \frac{1}{2\times\pi\times\sqrt{1.5uH\times 1360uF}}$$
$$= 3.5kHz$$

$$F_{ESR} = \frac{1}{2\times\pi\times ESR\times C_{OUT}}$$
$$= \frac{1}{2\times\pi\times 20.5m\Omega\times 1360uF}$$
$$= 5.7kHz$$

2.Set R_2 equal to10.2kΩ. Using equation 21, the final selection of R_1 is 3.24kΩ.

3. Set crossover frequency at 1/10~ 1/5 of the swithing frequency, here F_O=30kHz.

4.Calculate R_3 value by the following equation.

$$R_3 = \frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L}{R_{ESR}}\times\frac{1}{g_m}\times\frac{R_1+R_2}{R_1}$$
$$= \frac{1.1V}{12}\times\frac{2\times\pi\times 30kHz\times 1.5uH}{20.5\Omega}\times\frac{1}{2mA/V}$$
$$\times\frac{10.2k\Omega+3.24k\Omega}{3.24k\Omega}$$
$$=2.6k\Omega$$

Choose R_3 =2.61kΩ.

5. Calculate C_1 by setting compensator zero F_z at 75% of the LC double pole.

$$C_1 = \frac{1}{2\times\pi\times R_3\times F_z}$$
$$= \frac{1}{2\times\pi\times 2.61k\Omega\times 0.75\times 3.5kHz}$$
$$=23nF$$

Choose C_1=22nF.

6. Calculate C_2 by setting compensator pole F_p at half the swithing frequency.

$$C_2 = \frac{1}{\pi\times R_3\times F_s}$$
$$= \frac{1}{\pi\times 2.61k\Omega\times 300kHz}$$
$$= 406pF$$

Choose C_1=390pF.

Output Voltage Calculation

Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed at 0.8V. The divider consists of two ratioed resistors so that the output voltage applied at the Fb pin is 0.8V when the output voltage is at the desired value. The following equation and picture show the relationship between V_{OUT} , V_{REF} and voltage divider.

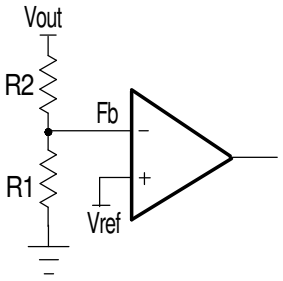

Figure 10 - Voltage divider

$$R_1 = \frac{R_2\times V_{REF}}{V_{OUT}-V_{REF}} \qquad ...(21)$$

where R_2 is part of the compensator, and the value of R_1 value can be set by voltage divider.

See compensator design for R_1 and R_2 selection.

Input Capacitor Selection

Input capacitors are usually a mix of high frequency ceramic capacitors and bulk capacitors. Ceramic capacitors bypass the high frequency noise, and bulk capacitors supply current to the MOSFETs. Usually 1uF ceramic capacitor is chosen to decouple the high frequency noise.The bulk input capacitors are decided by voltage rating and RMS current rating. The RMS current in the input capacitors can be calculated as:

$$I_{RMS} = I_{OUT}\times\sqrt{D}\times\sqrt{1-D}$$
$$D = \frac{V_{OUT}}{V_{IN}} \qquad ...(22)$$

V_{IN} = 12V, V_{OUT}=1.8V, I_{OUT}=10A, using equation (22), the result of input RMS current is 3.6A.

For higher efficiency, low ESR capacitors are recommended.

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One Sanyo OS-CON 16SVP180M 16V 180uF 20mΩ with 3.64A RMS rating are chosen as input bulk capacitors.

Power MOSFETs Selection

The NX2305 requires two N-Channel power MOSFETs. The selection of MOSFETs is based on maximum drain source voltage, gate source voltage, maximum current rating, MOSFET on resistance and power dissipation. The main consideration is the power loss contribution of MOSFETs to the overall converter efficiency. In this design example, two IRFR3709Z are used. They have the following parameters: V_{DS}=30V,R_{DSON} =6.5mΩ,Q_{GATE} =17nC.

There are two factors causing the MOSFET power loss:conduction loss, switching loss.

Conduction loss is simply defined as:

$$P_{HCON}=I_{OUT}^{2}\times D\times R_{DS(ON)}\times K$$

$$P_{LCON}=I_{OUT}^{2}\times(1-D)\times R_{DS(ON)}\times K \quad ...(23)$$

$$P_{TOTAL}=P_{HCON}+P_{LCON}$$

where the $R_{DS(ON)}$ will increases as MOSFET junction temperature increases, K is $R_{DS(ON)}$ temperature dependency. As a result, $R_{DS(ON)}$ should be selected for the worst case, in which K approximately equals to 1.4 at 125°C according to IRFR3709Z datasheet. Conduction loss should not exceed package rating or overall system thermal budget.

Switching loss is mainly caused by crossover conduction at the switching transition. The total switching loss can be approximated.

$$P_{SW}=\frac{1}{2}\times V_{IN}\times I_{OUT}\times T_{SW}\times F_S \quad ...(24)$$

where I_{OUT} is output current, T_{SW} is the sum of T_R and T_F which can be found in mosfet datasheet, and F_S is switching frequency. Switching loss P_{SW} is frequency dependent.

Also MOSFET gate driver loss should be considered when choosing the proper power MOSFET. MOSFET gate driver loss is the loss generated by discharging the gate capacitor and is dissipated in driver circuits.It is proportional to frequency and is defined as:

$$P_{gate}=(Q_{HGATE}\times V_{HGS}+Q_{LGATE}\times V_{LGS})\times F_S \quad ...(25)$$

where Q_{HGATE} is the high side MOSFETs gate charge,Q_{LGATE} is the low side MOSFETs gate charge,V_{HGS} is the high side gate source voltage, and V_{LGS} is the low side gate source voltage.

This power dissipation should not exceed maximum power dissipation of the driver device.

Soft Start and Enable

NX2305 has digital soft start for switching controller and has one enable pin for this start up. When the Power Ready (POR) signal is high and the voltage at enable pin is above $V_{ENTHH,}$ the internal digital counter starts to operate and the voltage at positive input of Error amplifier starts to increase, the feedback network will force the output voltage follows the reference and starts the output slowly. After 2048 cycles, the soft start is complete and the output voltage is regulated to the desired voltage decided by the feedback resistor divider.

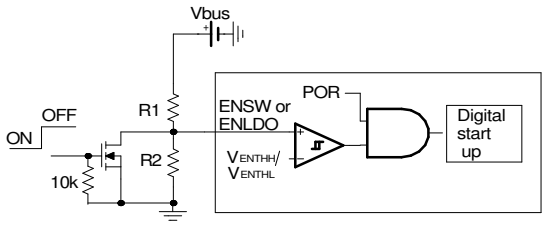

Figure 11 - Enable and Shut down the NX2305 with Enable pin.

The start up of NX2305 can be programmed through resistor divider at Enable pin. For example, if the input bus voltage is 12V and we want NX2305 starts when Vbus is above 8V. We can select

$$R_1=\frac{(8V-V_{ENTHH})\times R_2}{V_{ENTHH}}$$

The NX2305 can be turned off by pulling down the Enable pin by extra signal MOSFET as shown in the above Figure. When Enable pin is below $V_{ENTHL,}$ the digital soft start is reset to zero. In addition, all the high side and low side driver is off and no negative spike will be generated during the turn off.

Over Current Protection

Over current protection for NX2305 is achieved by sensing current through the low side MOSFET. An internal current source of 40uA flows through an external resistor connected from OCP pin to SW node sets the over current protection threshold. When synchronous FET is on, the voltage at node SW is given as

V_{SW}=-$I_L \times R_{DSON}$

The voltage at pin OCP is given as

$I_{OCP} \times R_{OCP}+V_{SW}$

When the voltage is below zero, the over current occurss as shown in figure 12.

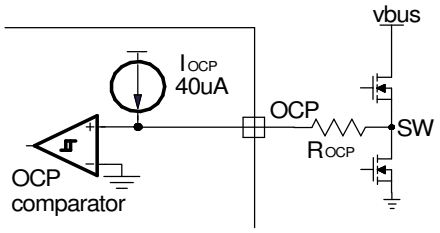

Figure 12 - Over current protection

The over current limit can be set by the following equation

$I_{SET} = I_{OCP} \times R_{OCP}/R_{DSON}$

If the MOSFET R_{DSON}=9mΩ, and the current limit is set at 15A, then

$$R_{OCP} = \frac{I_{SET} \times R_{DSON}}{I_{OCP}} = \frac{15A \times 9m\Omega}{40uA} = 3.375k\Omega$$

Choose R_{OCP}=4kΩ

LDO Selection Guide

NX2305 offers a LDO controller. The selection of MOSFET to meet LDO is more straight forward. The selection is that the Rdson of MOSFET should meet the dropout requirement. For example.

V_{LDOIN} =3.3V

V_{LDOOUT} =2.5V

I_{Load} =2A

The maximum Rdson of MOSFET should be

$$R_{RDSON} = (V_{LDOIN} - V_{LDOOUT}) \times I_{LOAD}$$
$$= (3.3V - 2.5V)/2A = 0.4\Omega$$

Most of MOSFETs can meet the requirement. More important is that MOSFET has to be selected right package to handle the thermal capability. For LDO, maximum power dissipation is given as

$$P_{LOSS} = (V_{LDOIN} - V_{LDOOUT}) \times I_{LOAD}$$
$$= (3.3V - 2.5V) \times 2A = 1.6W$$

Select IR MOSFET IRFR3706 with 9mΩ R_{DSON} is sufficient.

LDO Compensation

The diagram of LDO controller including VCC regulator is shown in figure 13.

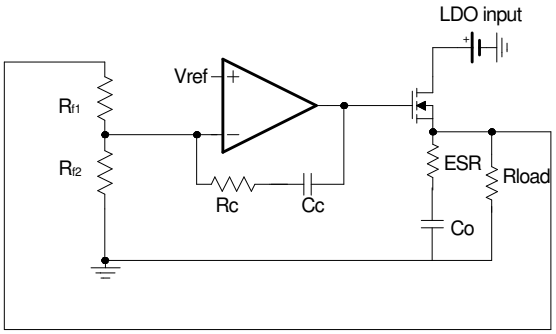

Figure 13 - NX2305 LDO controller.

For most low frequency capacitor such as electrolytic, POSCAP, OSCON, etc, the compensation parameter can be calculated as follows.

$$C_C = \frac{1}{4 \times \pi \times F_O \times R_{f1}} \times \frac{g_m \times ESR}{1 + g_m \times ESR}$$

where F_O is the desired crossover frequency.

Typically, in this LDO compensation, crossover frequency F_O has to be higher than zero caused by ESR. F_O is typically around several tens kHz to a few hundred kHz. For this example, we select Fo=100kHz. g_m is the forward trans-conductance of MOSFET.

For IRFR3706, g_m=53.

Select R_{f1}=5kohm.

Output capacitor is Sanyo POSCAP 4TPE150MI with 150uF, ESR=18mohm.

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$$C_C = \frac{1}{4\times\pi\times 100kHz\times 5k\Omega}\times\frac{53\times 18m\Omega}{1+53\times 18m\Omega} = 77pF$$

Choose C_C=82pF. For electrolytic or POSCAP, R_C is typically selected to be zero.

R_{f2} is determined by the desired output voltage.

$$R_{f2} = \frac{R_{f1}\times V_{REF}}{V_{LDOOUT} - V_{REF}} = \frac{5k\Omega\times 0.8V}{1.6V - 0.8V} = 5k\Omega$$

Choose R_{f2}=5kΩ.

When ceramic capacitors or some low ESR bulk capacitors are chosen as LDO output capacitors, the zero caused by output capacitor ESR is so high that crossover frequency F_O has to be chosen much higher than zero caused by R_C and C_C and much lower than zero caused by ESR. For example, 10uF ceramic is used as output capacitor. We select Fo=100kHz, R_{f1}=5kohm and select MOSFET MTD3055(g_m=5). R_C and C_C can be calculated as follows.

$$R_C = R_{f1}\times\frac{2\times\pi\times F_O\times C_O}{0.5\times g_m} = 5k\Omega\times\frac{2\times\pi\times 100kHz\times 10uF}{0.5\times 5S} = 12.56k\Omega$$

Choose R_C=12.7kΩ.

$$C_C = \frac{10\times C_O}{R_C\times g_m} = \frac{10\times 10uF}{12.7k\Omega\times 5S} = 1.6nF$$

Choose C_C=1.5nF.

Current Limit for LDO

Current limit of LDO is achieved by sensing the LDO feedback voltage. When LDO_FB pin is below 0.4V, the IC goes into hiccup mode. The IC will turn off all the channel for 2048 cycles and start to restart system again.

Layout Considerations

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

There are two sets of components considered in the layout which are power components and small signal components. Power components usually consist of input capacitors, high-side MOSFET, low-side MOSFET, inductor and output capacitors. A noisy environment is generated by the power components due to the switching power. Small signal components are connected to sensitive pins or nodes. A multilayer layout which includes power plane, ground plane and signal plane is recommended .

Layout guidelines:

1. First put all the power components in the top layer connected by wide, copper filled areas. The input capacitor, inductor, output capacitor and the MOSFETs should be close to each other as possible. This helps to reduce the EMI radiated by the power loop due to the high switching currents through them.

2. Low ESR capacitor which can handle input RMS ripple current and a high frequency decoupling ceramic cap which usually is 1uF need to be practically touching the drain pin of the upper MOSFET, a plane connection is a must.

3. The output capacitors should be placed as close as to the load as possible and plane connection is required.

4. Drain of the low-side MOSFET and source of the high-side MOSFET need to be connected thru a plane ans as close as possible. A snubber nedds to be placed as close to this junction as possible.

5. Source of the lower MOSFET needs to be connected to the GND plane with multiple vias. One is not enough. This is very important. The same applies to the output capacitors and input capacitors.

6. Hdrv and Ldrv pins should be as close to MOSFET gate as possible. The gate traces should be

wide and short. A place for gate drive resistors is needed to fine tune noise if needed.

7. Vcc capacitor, BST capacitor or any other by-passing capacitor needs to be placed first around the IC and as close as possible. The capacitor on comp to GND or comp back to FB needs to be place as close to the pin as well as resistor divider.

8. The output sense line which is sensing output back to the resistor divider should not go through high frequency signals.

9. All GNDs need to go directly thru via to GND plane.

10. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC.

11. In multilayer PCB, separate power ground and analog ground. These two grounds must be connected together on the PC board layout at a single point. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function.

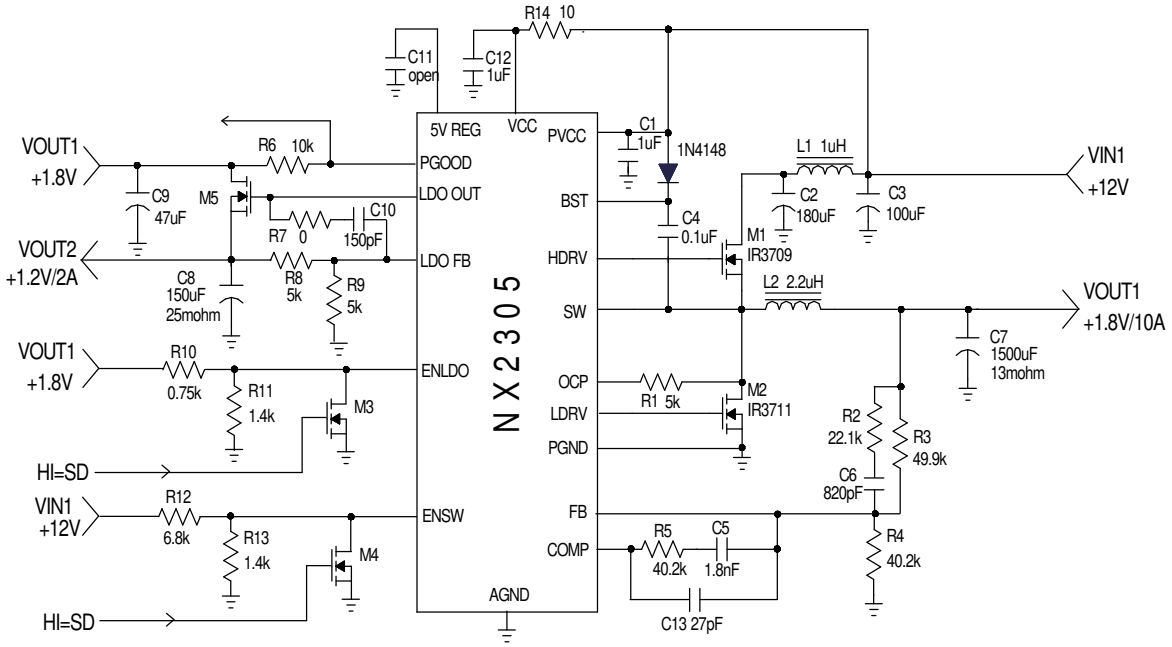

Figure 14 - Typical application of NX2305 with single power supply

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