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Triple low-ohmic single-pole double-throw analog switch

Rev. 1 — 18 April 2013

Product data sheet

1. General description

The NX3L4053-Q100 is a triple low-ohmic single-pole double-throw analog switch, suitable for use as an analog or digital multiplexer/demultiplexer. Each switch has a digital select input (nS), two independent inputs/outputs (nY0 and nY1) and a common input/output (nZ). All three switches share an enable input (\overline{E}). A digital enable pin \overline{E} is common to all switches. When \overline{E} is HIGH, the switches are turned off.

Schmitt trigger action at the digital inputs makes the circuit tolerant to slower input rise and fall times. Low threshold digital inputs allow this device to be driven by 1.8 V logic levels in 3.3 V applications without significant increase in supply current I_{CC}. This makes it possible for the NX3L4053-Q100 to switch 4.3 V signals with a 1.8 V digital controller, eliminating the need for logic level translation. The NX3L4053-Q100 allows signals with amplitude up to V_{CC} to be transmitted from nZ to nY0 or nY1; or from nY0 or nY1 to nZ. Its low ON resistance (0.5 Ω) and flatness (0.13 Ω) ensures minimal attenuation and distortion of transmitted signals.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.4 V to 4.3 V
- Very low ON resistance (peak):
 - 1.8 Ω (typical) at V_{CC} = 1.4 V
 - 1.0 Ω (typical) at V_{CC} = 1.65 V
 - 0.6 Ω (typical) at V_{CC} = 2.3 V
 - 0.6 Ω (typical) at V_{CC} = 2.7 V
 - 0.5 Ω (typical) at V_{CC} = 4.3 V
- Break-before-make switching
- High noise immunity
- ESD protection:
 - MIL-STD-883, method 3015 Class 3A exceeds 4000 V
 - HBM JESD22-A114F Class 3A exceeds 4000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
 - CDM AEC-Q100-011 revision B exceeds 1000 V
 - IEC61000-4-2 contact discharge exceeds 6000 V for switch ports
- CMOS low-power consumption
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A



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- 1.8 V control logic at V_{CC} = 3.6 V
- Control input accepts voltages above supply voltage
- Very low supply current, even when input is below V_{CC}
- High current handling capability (350 mA continuous current under 3.3 V supply)

3. Applications

- Cell phone
- PDA
- Portable media player
- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

4. Ordering information

Table 1.	Ordering information
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Type number	Package						
	Temperature range	Name	Description	Version			
NX3L4053HR-Q100	–40 °C to +125 °C	HXQFN16	plastic thermal enhanced extremely thin quad flat package; no leads; 16 terminals; body $3 \times 3 \times 0.5$ mm	SOT1039-2			
NX3L4053PW-Q100	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1			

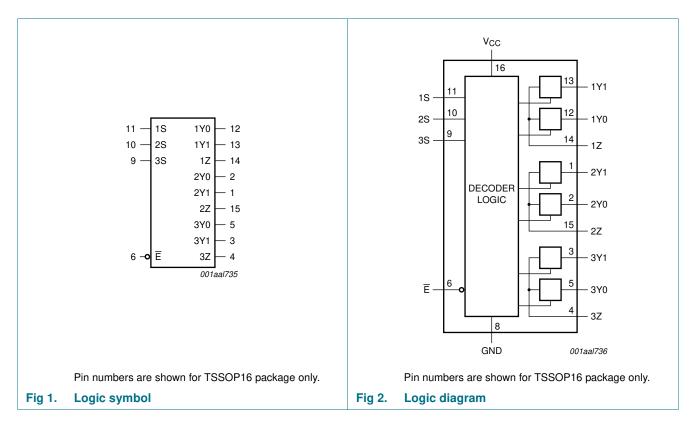
5. Marking

Table 2.Marking codes

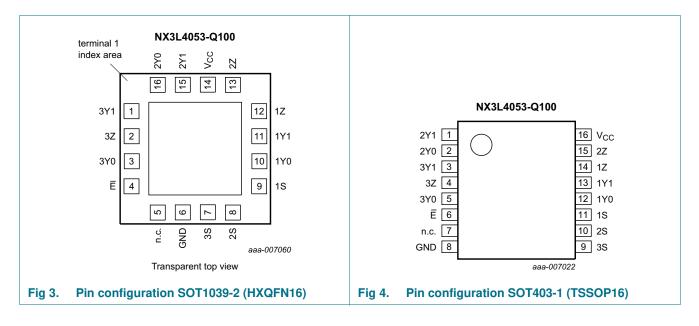
Type number	Marking code
NX3L4053HR-Q100	M43
NX3L4053PW-Q100	X3L4053

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6. Functional diagram



7. Pinning information



7.1 Pinning

Triple low-ohmic single-pole double-throw analog switch

7.2 Pin description

. . . .

Symbol	Pin		Description
	SOT1039-2	SOT403-1	
Ē	4	6	enable input (active LOW)
n.c.	5	7	not connected
GND	6	8	ground (0 V)
1S, 2S, 3S	9, 8, 7	11, 10 ,9	select input
1Y0, 2Y0, 3Y0	10, 16, 3	12, 2, 5	independent input or output
1Y1, 2Y1, 3Y1	11, 15, 1	13, 1, 3	independent input or output
1Z , 2Z, 3Z	12, 13, 2	14, 15, 4	independent output or input
V _{CC}	14	16	supply voltage

8. Functional description

Table 4.	Function table		
Inputs			Channel on
E		nS	
L		L	nY0 to nZ
L		Н	nY1 to nZ
Н		X	switches off

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
VI	input voltage	nS and E	[1] -0.5	+4.6	V
V _{SW}	switch voltage		2 -0.5	$V_{CC} + 0.5$	V
I _{IK}	input clamping current	$V_{I} < -0.5 V$	-50	-	mA
I _{SK}	switch clamping current	$V_{I} < -0.5$ V or $V_{I} > V_{CC} + 0.5$ V	-	±50	mA
I _{SW}	switch current	V_{SW} > -0.5 V or V_{SW} < V_{CC} + 0.5 V; source or sink current	-	±350	mA
		V_{SW} > -0.5 V or V_{SW} < V_{CC} + 0.5 V; pulsed at 1 ms duration, < 10 % duty cycle; peak current	-	±500	mA
T _{stg}	storage temperature		-65	+150	°C

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Table 5. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Мах	Unit
P _{tot}	total power dissipation	$T_{amb} = -40 \text{ °C to } +125 \text{ °C}$			
		HXQFN16	<u>[3]</u> _	250	mW
		TSSOP16	[4] _	500	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed but may not exceed 4.6 V.

[3] For HXQFN16 package: above 135 °C the value of P_{tot} derates linearly with 16.9 mW/K.

[4] For TSSOP16 package: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		1.4	4.3	V
VI	input voltage	nS and \overline{E}	0	4.3	V
V_{SW}	switch voltage		[1] 0	V _{CC}	V
T _{amb}	ambient temperature		-40	+125	°C
$\Delta t / \Delta V$	input transition rise and fall rate	nS and \overline{E} ; V _{CC} = 1.4 V to 4.3 V	-	200	ns/V

[1] To avoid sinking GND current from terminal nZ when switch current flows in terminal nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no GND current flows from terminal nYn. In this case, there is no limit for the voltage drop across the switch.

11. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	Tai	_{mb} = 25	°C	T _{amb} = ·	–40 °C to	+125 °C	Unit
			Min	Тур	Мах	Min	Max (85 °C)	Max (125 °C)	
V _{IH}	HIGH-level	$V_{CC} = 1.4 V$ to 1.6 V	0.9	-	-	0.9	-	-	V
	input voltage	$V_{CC} = 1.65 \text{ V}$ to 1.95 V	0.9	-	-	0.9	-	-	V
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	1.1	-	-	1.1	-	-	V
		$V_{CC} = 2.7 \text{ V} \text{ to } 3.6 \text{ V}$	1.3	-	-	1.3	-	-	V
		$V_{CC} = 3.6 \text{ V} \text{ to } 4.3 \text{ V}$	1.4	-	-	1.4	-	-	V
V _{IL}	LOW-level input voltage	$V_{CC} = 1.4 \text{ V}$ to 1.6 V	-	-	0.3	-	0.3	0.3	V
		$V_{CC} = 1.65 \text{ V}$ to 1.95 V	-	-	0.4	-	0.4	0.3	V
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	-	-	0.4	-	0.4	0.4	V
		$V_{CC} = 2.7 \text{ V} \text{ to } 3.6 \text{ V}$	-	-	0.5	-	0.5	0.5	V
		$V_{CC} = 3.6 \text{ V to } 4.3 \text{ V}$	-	-	0.6	-	0.6	0.6	V
lı	input leakage current	nS and \overline{E} ; V _I = GND to 4.3 V; V _{CC} = 1.4 V to 4.3 V	-	-	-	-	±0.5	±1	μA

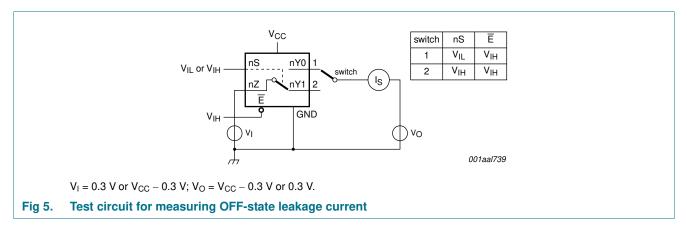
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Static characteristics ... continued Table 7.

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

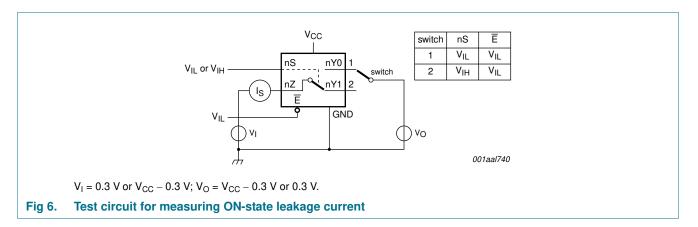
Symbol	Parameter	Conditions	Ta	_{amb} = 25	°C	T _{amb} =	–40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max (85 °C)	Max (125 °C)	
I _{S(OFF)}	OFF-state leakage	nY0 and nY1 port; see <u>Figure 5</u>		1		1			
	current	V_{CC} = 1.4 V to 3.6 V	-	-	±5	-	±50	±500	nA
		$V_{CC} = 3.6 \text{ V to } 4.3 \text{ V}$	-	-	±10	-	±50	±500	nA
I _{S(ON)}	ON-state leakage current	nZ port; V _{CC} = 1.4 V to 3.6 V; see <u>Figure 6</u>							
		$V_{CC} = 1.4 \text{ V} \text{ to } 3.6 \text{ V}$	-	-	±5	-	±50	±500	nA
		V_{CC} = 3.6 V to 4.3 V	-	-	±10	-	±50	±500	nA
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $V_{SW} = GND$ or V_{CC}							
		$V_{CC} = 3.6 V$	-	-	100	-	500	5000	nA
		$V_{CC} = 4.3 V$	-	-	150	-	800	6000	nA
ΔI_{CC}	additional	$V_{SW} = GND \text{ or } V_{CC}$							
	supply current	$V_{I} = 2.6 \text{ V}; V_{CC} = 4.3 \text{ V}$	-	2.0	4.0	-	7	7	μA
		$V_{I} = 2.6 \text{ V}; V_{CC} = 3.6 \text{ V}$	-	0.35	0.7	-	1	1	μA
		$V_{I} = 1.8 \text{ V}; V_{CC} = 4.3 \text{ V}$	-	7.0	10.0	-	15	15	μA
		$V_{I} = 1.8 V; V_{CC} = 3.6 V$	-	2.5	4.0	-	5	5	μA
		$V_{I} = 1.8 \text{ V}; V_{CC} = 2.5 \text{ V}$	-	50	200	-	300	500	nA
CI	input capacitance	nS and \overline{E}	-	1.0	-	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance		-	35	-	-	-	-	pF
C _{S(ON)}	ON-state capacitance		-	130	-	-	-	-	pF

11.1 Test circuits



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11.2 ON resistance

Table 8. ON resistance^[1]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see Figure 8 to Figure 14.

Symbol	Parameter	Conditions	T _{amb} =	–40 °C to	o +85 °C	$T_{amb} = -40$ °	C to +125 °C	Unit	
			Min	Typ ^[2]	Max	Min	Max		
$R_{ON(peak)}$	ON resistance (peak)	$V_I = GND$ to V_{CC} ; $I_{SW} = 100$ mA; see Figure 7							
		$V_{CC} = 1.4 V$	-	1.8	3.8	-	4.2	Ω	
		$V_{CC} = 1.65 V$	-	1.0	1.7	-	1.8	Ω	
		$V_{CC} = 2.3 V$	-	0.6	0.9	-	1.0	Ω	
		$V_{CC} = 2.7 V$	-	0.6	0.80	-	1.0	Ω	
		$V_{CC} = 4.3 V$	-	0.5	0.80	-	1.0	Ω	
ΔR_{ON}	ON resistance mismatch	$V_{I} = GND \text{ to } V_{CC};$ $I_{SW} = 100 \text{ mA}$	1						
	between	$V_{CC} = 1.4 \text{ V}; V_{SW} = 0.4 \text{ V}$	-	0.23	0.38	-	0.38	Ω	
	channels	$V_{CC} = 1.65 \text{ V}; V_{SW} = 0.5 \text{ V}$	-	0.23	0.28	-	0.38	Ω	
		$V_{CC} = 2.3 \text{ V}; V_{SW} = 0.7 \text{ V}$	-	0.12	0.15	-	0.18	Ω	
		$V_{CC} = 2.7 \text{ V}; V_{SW} = 0.8 \text{ V}$	-	0.12	0.15	-	0.18	Ω	
		$V_{CC} = 4.3 \text{ V}; V_{SW} = 0.8 \text{ V}$	-	0.12	0.15	-	0.18	Ω	
$R_{ON(flat)}$	ON resistance (flatness)	$V_{I} = GND \text{ to } V_{CC};$ [4] $I_{SW} = 100 \text{ mA}$	1						
		$V_{CC} = 1.4 V$	-	1.0	3.3	-	3.6	Ω	
		V _{CC} = 1.65 V	-	0.5	1.2	-	1.3	Ω	
		$V_{CC} = 2.3 V$	-	0.15	0.3	-	0.35	Ω	
		$V_{CC} = 2.7 V$	-	0.13	0.3	-	0.35	Ω	
		$V_{CC} = 4.3 V$	-	0.2	0.4	-	0.45	Ω	

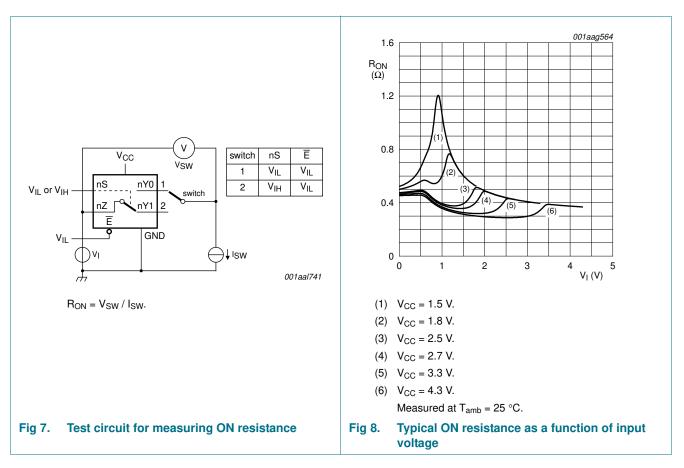
[1] For NX3L4053PW-Q100 (TSSOP16 package), all ON resistance values are up to 0.05 Ω higher.

[2] Typical values are measured at $T_{amb} = 25 \text{ °C}$.

[3] Measured at identical V_{CC} , temperature and input voltage.

[4] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

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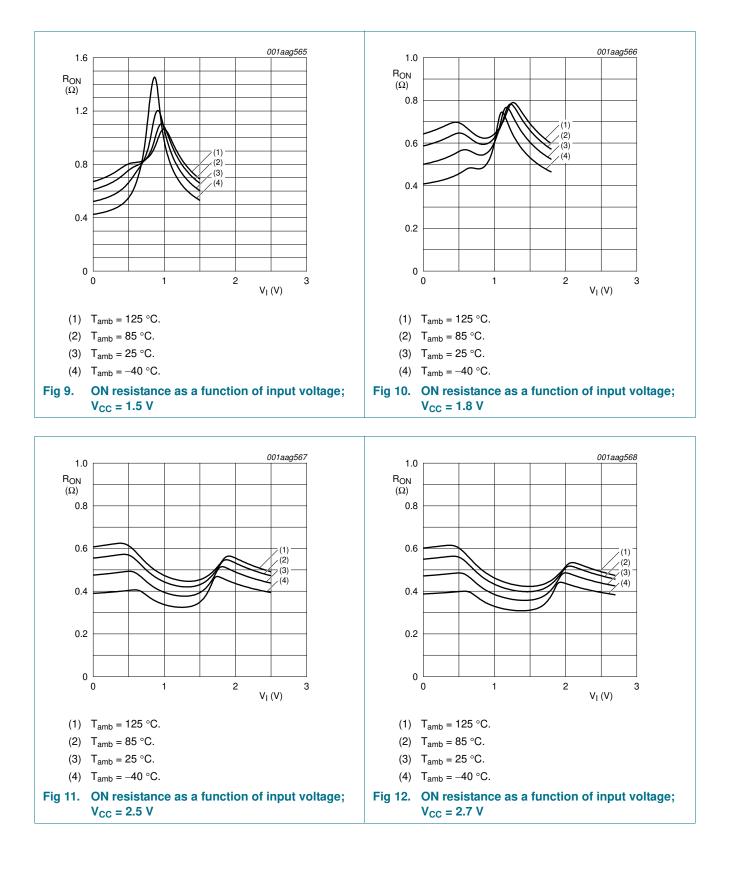


11.3 ON resistance test circuit and graphs

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NX3L4053-Q100

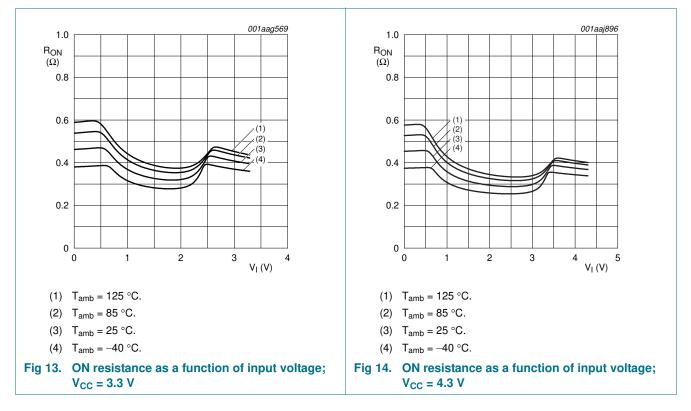
Triple low-ohmic single-pole double-throw analog switch



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Triple low-ohmic single-pole double-throw analog switch



12. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for load circuit see Figure 17.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +125 °C			Unit
			Min	Typ <mark>[1]</mark>	Max	Min	Max (85 °C)	Max (125 °C)	
t _{en}	enable time	Ē, nS to nZ or nYn; see <u>Figure 15</u>							
		$V_{CC} = 1.4 \text{ V} \text{ to } 1.6 \text{ V}$	-	49	90	-	120	120	ns
		V _{CC} = 1.65 V to 1.95 V	-	35	70	-	80	90	ns
		V_{CC} = 2.3 V to 2.7 V	-	23	45	-	50	55	ns
		V_{CC} = 2.7 V to 3.6 V	-	21	40	-	45	50	ns
		V_{CC} = 3.6 V to 4.3 V	-	21	40	-	45	50	ns
t _{dis}	disable time	Ē, nS to nZ or nYn; see <u>Figure 15</u>							
		$V_{CC} = 1.4 \text{ V} \text{ to } 1.6 \text{ V}$	-	32	70	-	80	90	ns
		V _{CC} = 1.65 V to 1.95 V	-	17	55	-	60	65	ns
		V_{CC} = 2.3 V to 2.7 V	-	11	25	-	30	35	ns
		V_{CC} = 2.7 V to 3.6 V	-	8	20	-	25	30	ns
		V_{CC} = 3.6 V to 4.3 V	-	8	20	-	25	30	ns

ns

ns

ns

ns

ns

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T_{amb} = -40 °C to +125 °C Symbol Parameter Conditions T_{amb} = 25 °C Unit Min Typ^[1] Max Min Max Max (85 °C) (125 °C) [2] break-before-make see Figure 16 t_{b-m} time $V_{CC} = 1.4$ V to 1.6 V 9 19 _ _ -_ $V_{CC} = 1.65 \text{ V}$ to 1.95 V 17 7 ---- $V_{CC} = 2.3 \text{ V}$ to 2.7 V 13 4 _ _ _ _ $V_{CC} = 2.7 \text{ V} \text{ to } 3.6 \text{ V}$ 10 3 _ _ _ _ $V_{CC} = 3.6 V \text{ to } 4.3 V$ 9 2 ----

Table 9. Dynamic characteristics ... continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for load circuit see Figure 17.

[1] Typical values are measured at $T_{amb} = 25$ °C and $V_{CC} = 1.5$ V, 1.8 V, 2.5 V, 3.3 V and 4.3 V respectively.

Break-before-make guaranteed by design. [2]

12.1 Waveform and test circuits

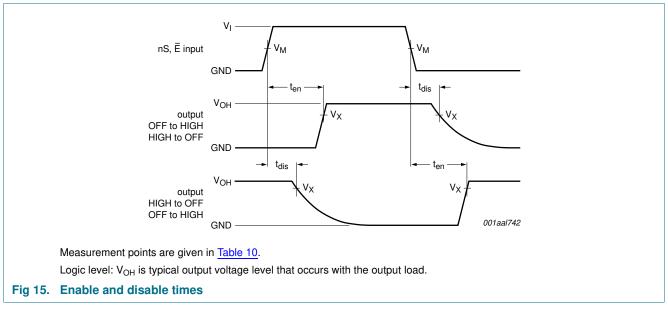
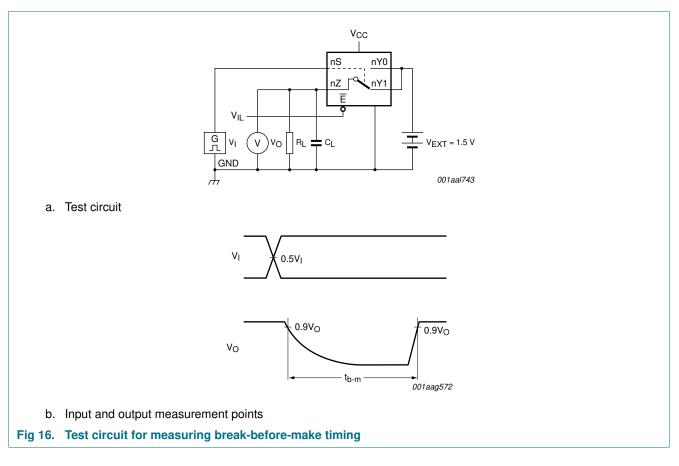
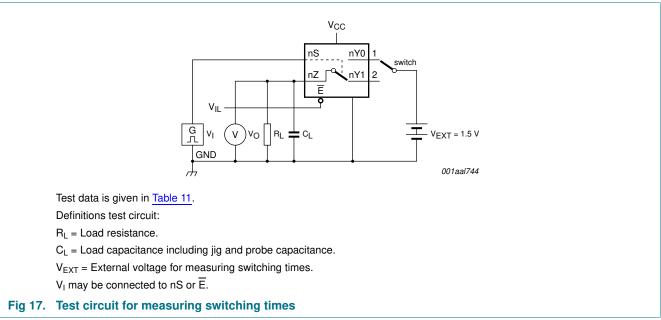


Table 10. Measurement points

Supply voltage	Input	Output
V _{cc}	V _M	V _X
1.4 V to 4.3 V	0.5V _{CC}	0.9V _{OH}

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Table 11. Test data

Supply voltage	Input		Load		
V _{cc}	VI	t _r , t _f	CL	R _L	
1.4 V to 4.3 V	V _{CC}	\leq 2.5 ns	35 pF	50 Ω	

12.2 Additional dynamic characteristics

Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $V_I = GND$ or V_{CC} (unless otherwise specified); $t_r = t_f \le 2.5$ ns; $T_{amb} = 25$ °C.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
THD	total harmonic	f_i = 20 Hz to 20 kHz; R_L = 32 Ω ; see Figure 18	<u>[1]</u>			
	distortion	V _{CC} = 1.4 V; V _I = 1 V (p-p)	-	0.15	-	%
		V _{CC} = 1.65 V; V _I = 1.2 V (p-p)	-	0.10	-	%
		V _{CC} = 2.3 V; V _I = 1.5 V (p-p)	-	0.02	-	%
		V _{CC} = 2.7 V; V _I = 2 V (p-p)	-	0.02	-	%
		V _{CC} = 4.3 V; V _I = 2 V (p-p)	-	0.02	-	%
f _(-3dB)	-3 dB frequency	$R_L = 50 \Omega$; see Figure 19	<u>[1]</u>			
	response	V _{CC} = 1.4 V to 4.3 V	-	60	-	MHz
α_{iso}	isolation (OFF-state)	$f_i = 100 \text{ kHz}; \text{ R}_L = 50 \Omega; \text{ see } \frac{\text{Figure 20}}{100 \text{ kHz}}$	<u>[1]</u>			
		V _{CC} = 1.4 V to 4.3 V	-	-90	-	dB
V _{ct}	crosstalk voltage	between digital inputs and switch; $f_i = 1 \text{ MHz}$; $C_L = 50 \text{ pF}$; $R_L = 50 \Omega$; see Figure 21				
		V _{CC} = 1.4 V to 3.6 V	-	0.2	-	V
		V _{CC} = 3.6 V to 4.3 V	-	0.3	-	V
Xtalk	crosstalk	between switches; $f_i = 100 \text{ kHz}$; $R_L = 50 \Omega$; see Figure 22	[1]			
		V _{CC} = 1.4 V to 4.3 V	-	-90	-	dB
Q _{inj}	charge injection	$f_i = 1 \text{ MHz}; C_L = 0.1 \text{ nF}; R_L = 1 \text{ M}\Omega; V_{gen} = 0 \text{ V}; R_{gen} = 0 \Omega; \text{ see } \frac{\text{Figure 23}}{2}$				
		V _{CC} = 1.5 V	-	3	-	рС
		V _{CC} = 1.8 V	-	4	-	рС
		$V_{CC} = 2.5 V$	-	6	-	рС
		$V_{CC} = 3.3 V$	-	9	-	рС
		$V_{CC} = 4.3 V$	-	15	-	рС

[1] f_i is biased at 0.5V_{CC}.

Triple low-ohmic single-pole double-throw analog switch

12.3 Test circuits

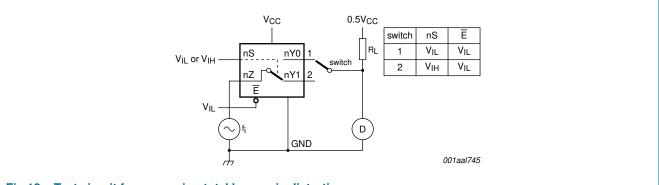
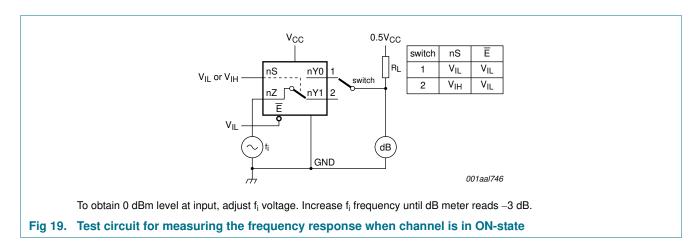
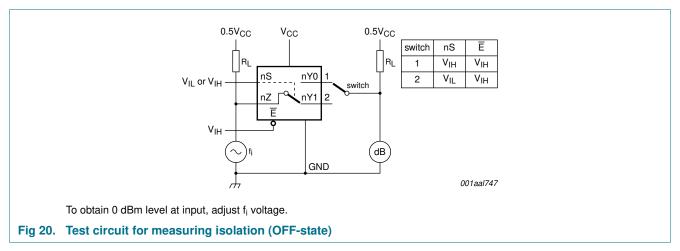
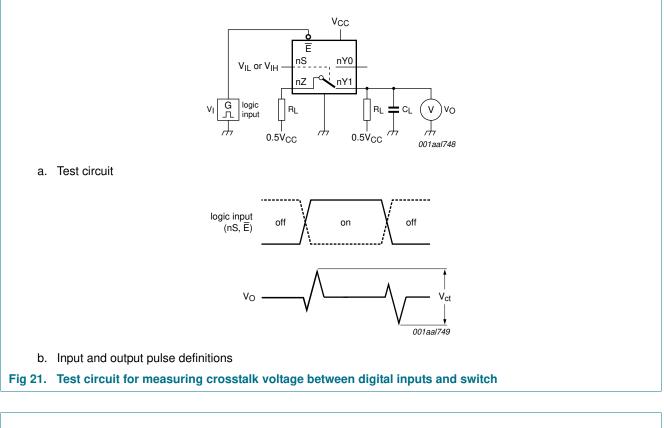


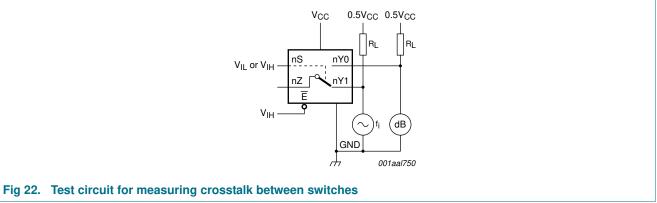
Fig 18. Test circuit for measuring total harmonic distortion



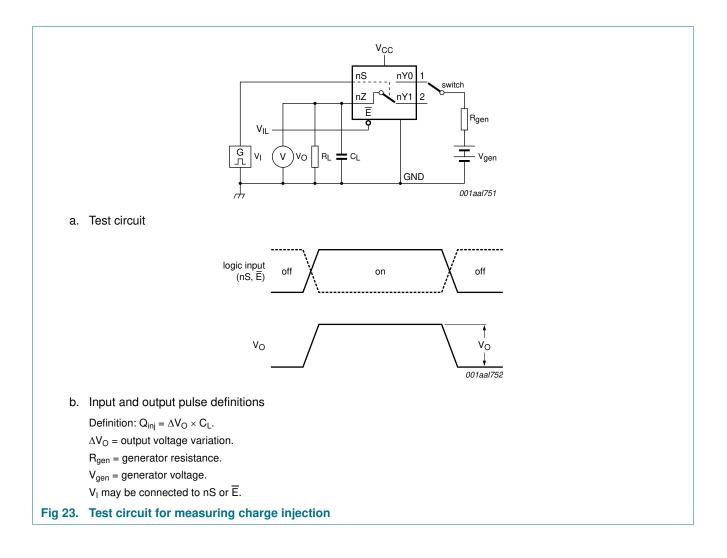


Triple low-ohmic single-pole double-throw analog switch





Triple low-ohmic single-pole double-throw analog switch



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13. Package outline

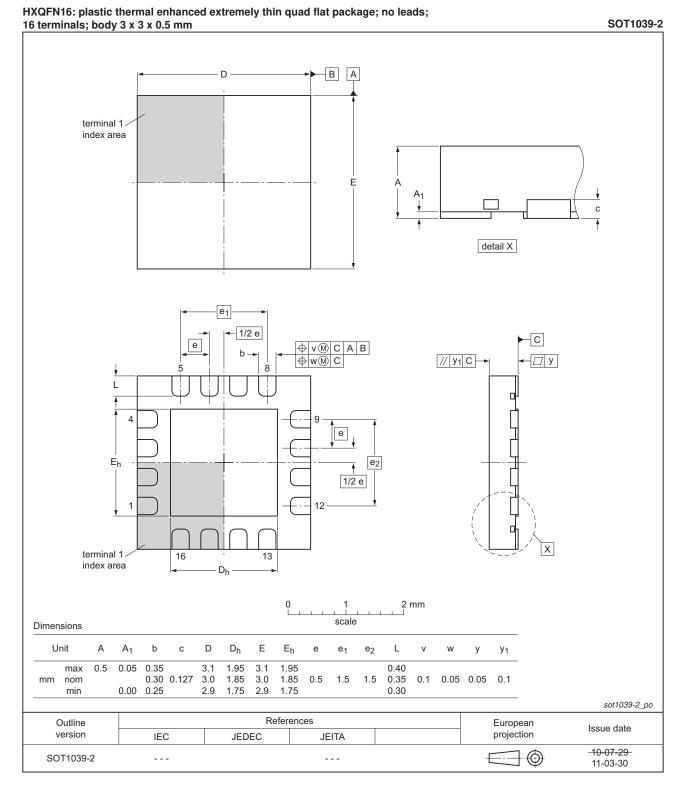


Fig 24. Package outline SOT1039-2 (HXQFN16)

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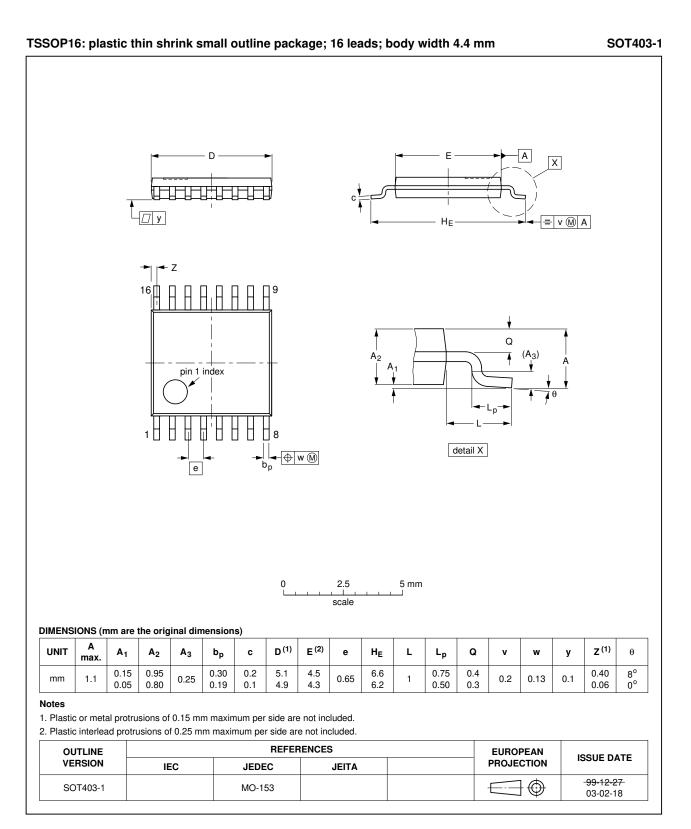


Fig 25. Package outline SOT403-1 (TSSOP16)

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14. Abbreviations

Table 13.	Abbreviations
Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
PDA	Personal Digital Assistant

15. Revision history

Table 14. Revision history						
Document ID	Release date	Data sheet status	Change notice	Supersedes		
NX3L4053_Q100 v.1	20130418	Product data sheet	-	-		

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 18 April 2013 Document identifier: NX3L4053_Q100