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# NX5DV713E

## Dual supply 1-of-2 VGA switch

Rev. 1 — 24 November 2011

Product data sheet

## 1. General description

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The NX5DV713E is a dual supply 1-to-2 VGA switch. It integrates high-bandwidth SPDT switches with level-translating buffers and level translating switches to provide switching of input RGB, H-sync, V-sync and DDC signals to either of two output channels.

The NX5DV713E is characterized for operation from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

## 2. Features and benefits

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- RGB switches:
  - ◆ Low ON resistance ( $4\ \Omega$  typical)
  - ◆ Low ON capacitance (12 pF typical)
  - ◆ Low output skew (50 ps)
- Low power consumption ( $< 2\ \mu\text{A}$ )
- Level translation of sync and DDC signals
- Over-voltage tolerant inputs
- ESD protection:
  - ◆ HBM JESD22-A114F Class 3A exceeds 4 kV
  - ◆ MM JESD22-A115-A exceeds 200 V
  - ◆ CDM JESD22-C101D exceeds 1000 V
  - ◆ IEC61000-4-2 contact discharge exceeds 4 kV for I/Os
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

## 3. Applications

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- Notebook Computers
- Docking stations
- Digital projectors
- Computer monitors
- Servers
- Storage



### 4. Ordering information

Table 1. Ordering information

Type number	Package		Description	Version
	Temperature range	Name		
NX5DV713EHF	-40 °C to +85 °C	HWQFN32	plastic thermal enhanced very very thin quad flat package; no leads; 32 terminals; body 3 × 6 × 0.75 mm	SOT1180-1

### 5. Functional diagram

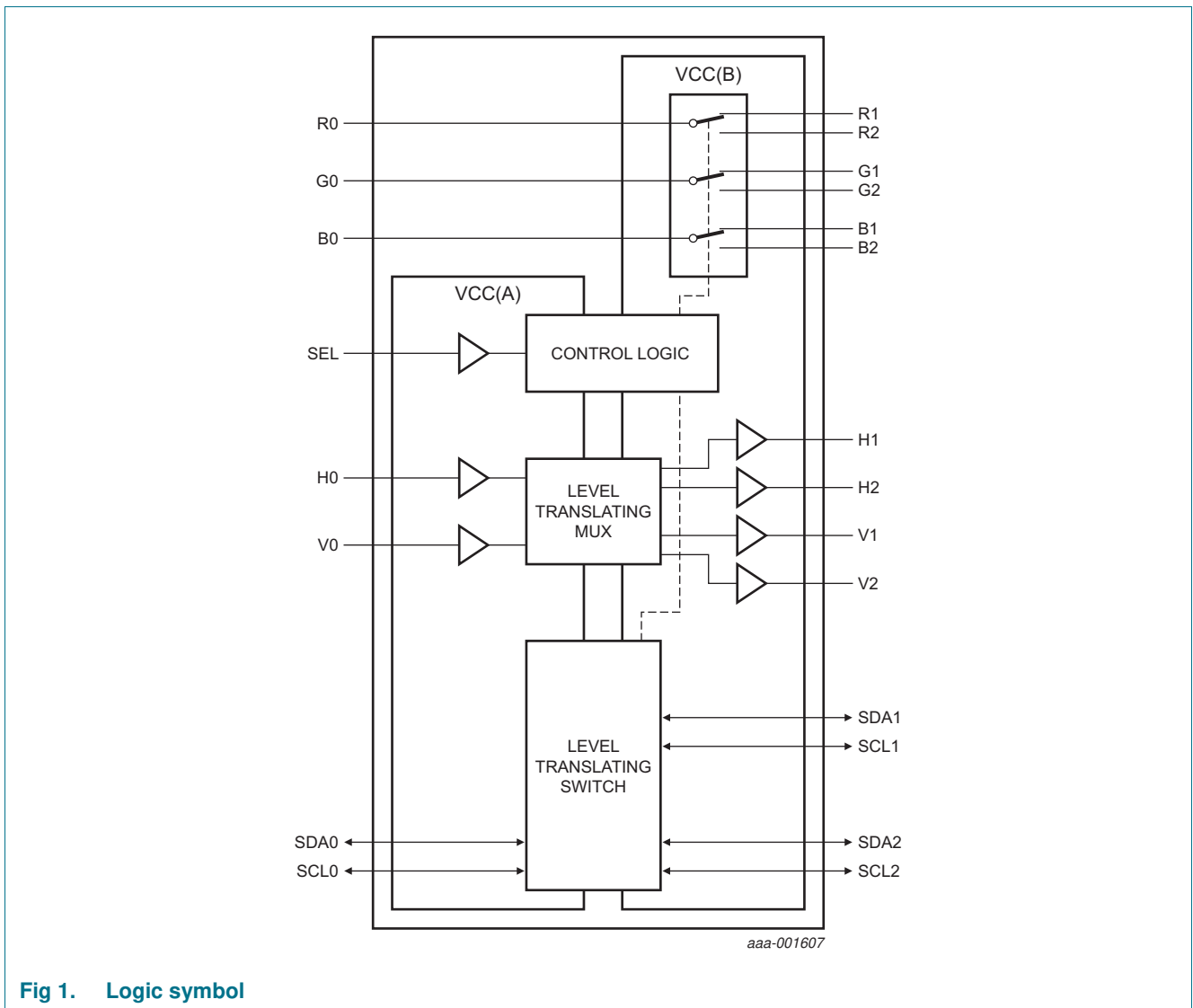
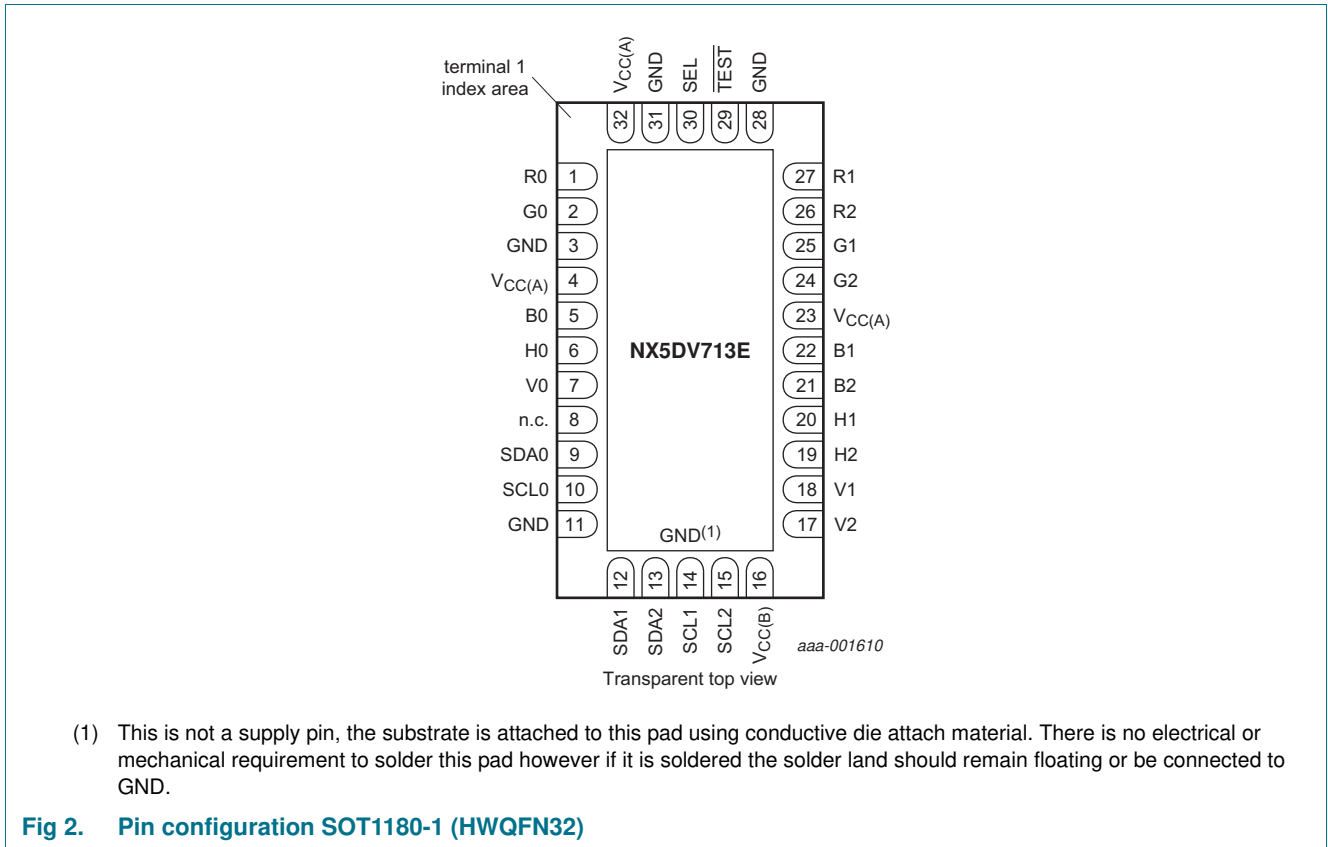


Fig 1. Logic symbol

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

**Table 2. Pin description**

Symbol	Pin	Description
R0, G0, B0	1, 2, 5	RGB input or output
GND	3, 11, 28, 31	ground (0 V)
V <sub>CC(A)</sub>	4, 23, 32	supply voltage A
H0	6	horizontal sync input
V0	7	vertical sync input
n.c.	8	not connected
SDA0	9	SDA0 input or output
SCL0	10	SCL0 input or output
SDA1, SDA2	12, 13	SDAn input or output
SCL1, SCL2	14, 15	SCLn input or output
V <sub>CC(B)</sub>	16	supply voltage B
V1, V2	18, 17	vertical sync output
H1, H2	20, 19	horizontal sync output

**Table 2.** Pin description ...continued

Symbol	Pin	Description
R1, G1, B1, R2, G2, B2	27, 25, 22, 26, 24, 21	RGB input or output
TEST <sup>[1]</sup>	29	test pin (active LOW)
SEL	30	select input

[1] Test pin used to enable test mode. For normal usage, this pin must be connected to  $V_{CC(A)}$ .

## 7. Functional description

The NX5DV713E integrates high-bandwidth SPDT switches, level-translating buffers and level translating SPDT switches to provide a complete solution for 1-to-2 switching of VGA signals. An select input (SEL) is used to determine which output is selected.

### 7.1 RGB switches

The NX5DV713E provides three identical single pole double throw high-bandwidth switches to route standard VGA RGB signals (see [Table 3](#)).

**Table 3.** Function table RGB

*H = HIGH voltage level; L = LOW voltage level; X = Don't care; Z = high-impedance OFF-state.*

Input	Switch
SEL	
L	R0 to R1; G0 to G1; B0 to B1
H	R0 to R2; G0 to G2; B0 to B2

### 7.2 H-Sync/V-Sync level translator

The horizontal and vertical synchronization buffers have inputs (H0, V0) referenced to  $V_{CC(A)}$  and outputs (H1, V1 and H2, V2) that are referenced to  $V_{CC(B)}$ . This allows level translation of synchronization signals from as low as 2.0 V up to 5.5 V and supports low-voltage CMOS or TTL-compatible graphics controllers meeting the VESA specification for output drive of  $\pm 8$  mA.

**Table 4.** Function table HV

*H = HIGH voltage level; L = LOW voltage level; X = Don't care; Z = high-impedance OFF-state.*

Input	Switch
SEL	
L	H1 = H0; V1 = V0; H2, V2 = Z
H	H2 = H0; V2 = V0; H1, V1 = Z

### 7.3 Display-Data Channel Multiplexer

The NX5DV713E provides two identical SPDT active-level translating switches to route DDC signals (See [Table 5](#)). The switch outputs are limited to a diode drop less than the voltage applied on  $V_{CC(A)}$ . To provide VESA I<sup>2</sup>C-compatible signals 3.3 V should be applied to  $V_{CC(A)}$ . If voltage translation is not required  $V_{CC(A)}$  should be connected to  $V_{CC(B)}$ .

**Table 5. Function table DDC**

*H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.*

Input SEL	Switch
L	SDA0 to SDA1, SCL0 to SCL1
H	SDA0 to SDA2, SCL0 to SCL2

## 8. Limiting values

**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+6	V
$V_{CC(B)}$	supply voltage B		-0.5	+6	V
$V_I$	input voltage		[1] -0.5	+6	V
$V_{SW}$	switch voltage		[1] -0.5	+6	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V	-50	-	mA
$I_{SK}$	switch clamping current	$V_I < -0.5$ V	-50	-	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$I_O$	output current	$V_O = 0$ V to $V_{CC(B)}$	-	±50	mA
$I_{CC}$	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
$I_{GND}$	ground current		-100	-	mA
$I_{SW}$	switch current	$V_{SW} > -0.5$ V or $V_{SW} < 6$ V; source or sink current	-	±30	mA
		$V_{SW} > -0.5$ V or $V_{SW} < 6$ V; pulsed at 1 ms duration, < 10 % duty cycle; peak current	-	±90	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +85 °C	[2] -	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] For HWQFN32 package: above 137 °C the value of  $P_{tot}$  derates linearly with 20.5 mW/K.

## 9. Recommended operating conditions

**Table 7. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(A)}$	supply voltage A		2	3.3	5.5	V
$V_{CC(B)}$	supply voltage B		4.5	5.0	5.5	V
$T_{amb}$	ambient temperature	operating in free-air	-40	+25	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC(A)} = 2.3\text{ V to }2.7\text{ V}$	[1] -	20	-	ns/V
		$V_{CC(A)} = 3\text{ V to }3.6\text{ V}$	[1] -	10	-	ns/V
		$V_{CC(A)} = 4.5\text{ V to }5.5\text{ V}$	[1] -	5	-	ns/V

[1] Applies to control signal levels.

## 10. Static characteristics

**Table 8. Static characteristics**

$V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{CC(A)} = 2\text{ V to }5.5\text{ V}$ , unless otherwise specified; Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$			Unit
			Min	Typ [1]	Max	
<b>General</b>						
$I_{CC(A)}$	supply current A	$V_{CC(A)} = 3.3\text{ V}$ ; for H1, H2, V1, V2: $I_O = 0\text{ A}$	-	-	2.0	$\mu\text{A}$
$I_{CC(B)}$	supply current B	$V_{CC(B)} = 5.0\text{ V}$ ; for H1, H2, V1, V2: $I_O = 0\text{ A}$	-	-	2.0	$\mu\text{A}$
<b>HV buffer</b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC(A)} = 3\text{ V to }3.6\text{ V}$	2	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC(A)} = 3\text{ V to }3.6\text{ V}$	-	-	0.8	V
$V_H$	hysteresis voltage		-	50	-	mV
$I_I$	input leakage current	$V_{CC(B)} = V_{CC(A)} = 5.5\text{ V}$ ; $V_I = \text{GND to }V_{CC(A)}$	-	-	$\pm 1$	$\mu\text{A}$
$V_{OH}$	HIGH-level output voltage	$I_O = -8\text{ mA}$	$V_{CC(B)} - 0.5$	-	-	V
$V_{OL}$	LOW-level output voltage	$I_O = 8\text{ mA}$	-	-	0.5	V
$I_{OFF}$	power-off leakage current	$V_I$ or $V_O = 0\text{ V to }5.5\text{ V}$ ; $V_{CC(B)} = 0\text{ V}$ ; $V_{CC(A)} = 0\text{ V to }5.5\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
<b>RGB switches</b>						
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC(B)} = 5.5\text{ V}$ ; $V_I = 0.3\text{ V or }5.5\text{ V}$ ; $V_O = 0\text{ V to }V_{CC(B)}$ ; See <a href="#">Figure 3</a>	-	-	$\pm 1$	$\mu\text{A}$
$I_{S(ON)}$	ON-state leakage current	$V_{CC(B)} = 5.5\text{ V}$ ; $V_I = 0.3\text{ V or }5.5\text{ V}$ ; $V_O = 0\text{ V to }V_{CC(B)}$ ; See <a href="#">Figure 4</a>	-	-	$\pm 1$	$\mu\text{A}$
$R_{ON}$	ON resistance	$V_I = 0.7\text{ V}$ ; $I_{SW} = -10\text{ mA}$ ; See <a href="#">Figure 5</a> and <a href="#">Figure 6</a>	[4] -	4	-	$\Omega$
$\Delta R_{ON}$	ON resistance mismatch between channels	$V_I = \text{GND to }0.7\text{ V}$ ; $I_{SW} = -10\text{ mA}$	[2] -	0.5	-	$\Omega$
$R_{ON(Flat)}$	ON resistance (flatness)	$V_I = \text{GND to }0.7\text{ V}$ ; $I_{SW} = -10\text{ mA}$	[3] -	0.5	-	$\Omega$
$C_{S(OFF)}$	OFF-state capacitance		-	4.5	-	pF
$C_{S(ON)}$	ON-state capacitance		-	12	-	pF

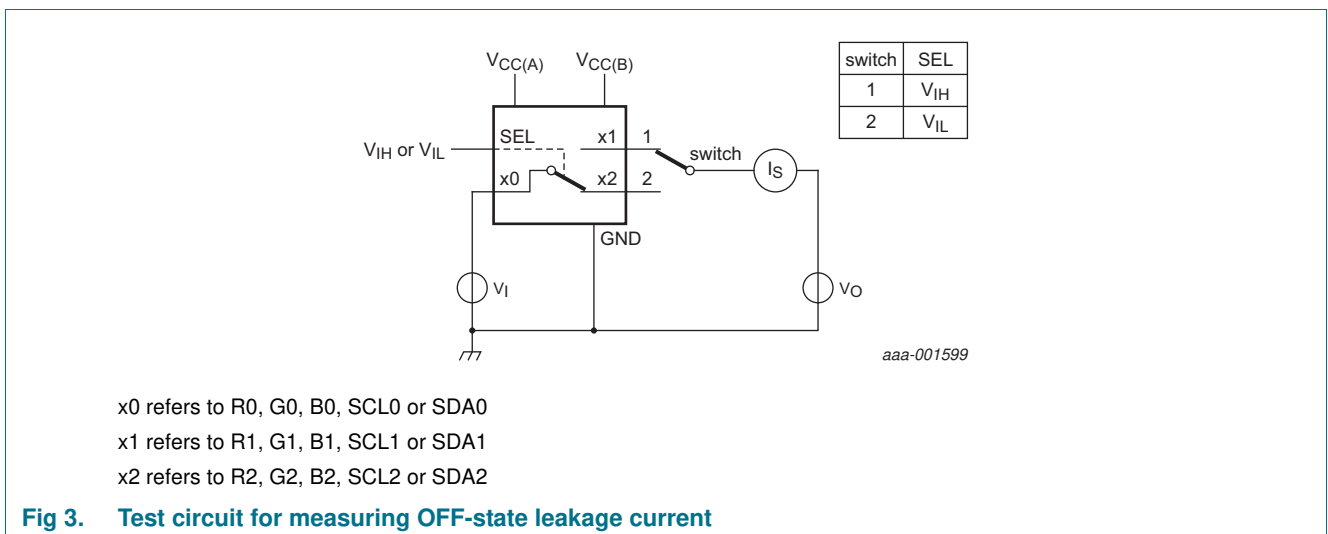
**Table 8. Static characteristics ...continued**

$V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{CC(A)} = 2\text{ V to }5.5\text{ V}$ , unless otherwise specified; Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$			Unit	
			Min	Typ <sup>[1]</sup>	Max		
<b>SDAn, SCLn</b>							
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC(B)} = 5.5\text{ V}$ ; $V_{CC(A)} = 3.6\text{ V}$ ; SCL0, SDA0, SCL1, SCL2, SDA1, SDA2 = $V_{CC(A)}$ or GND; $V_O = 0\text{ V to }V_{CC(B)}$ ; See <a href="#">Figure 3</a>	[5]	-	-	$\pm 1$	$\mu\text{A}$
$R_{ON}$	ON resistance	$V_{CC(A)} = 2\text{ V}$ ; $V_I = 0.4\text{ V}$ ; $I_{SW} = \pm 2\text{ mA}$ ; See <a href="#">Figure 5</a> and <a href="#">Figure 7</a>	-	9	-	-	$\Omega$
$C_{S(ON)}$	ON-state capacitance		-	15	-	-	pF
<b>Control Logic (SEL)</b>							
$V_{IH}$	HIGH-level input voltage	$V_{CC(A)} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	-	V
		$V_{CC(A)} = 3.0\text{ V to }3.6\text{ V}$	2.0	-	-	-	V
		$V_{CC(A)} = 4.5\text{ V to }5.5\text{ V}$	$0.7V_{CC(A)}$	-	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC(A)} = 2.3\text{ V to }2.7\text{ V}$	-	-	-	0.7	V
		$V_{CC(A)} = 3.0\text{ V to }3.6\text{ V}$	-	-	-	0.8	V
		$V_{CC(A)} = 4.5\text{ V to }5.5\text{ V}$	-	-	-	$0.3V_{CC(A)}$	V
$V_H$	hysteresis voltage		-	50	-	-	mV
$I_I$	input leakage current	$V_{CC(A)} = 5.5\text{ V}$ ; $V_I = \text{GND to }V_{CC(A)}$	-	-	-	$\pm 1$	$\mu\text{A}$

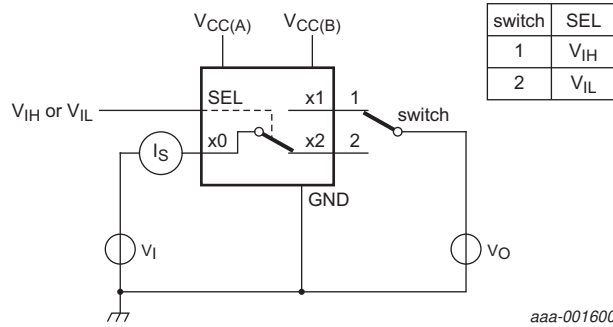
- [1] All typical values are measured at  $V_{CC(B)} = 5\text{ V}$ ,  $V_{CC(A)} = 3.3\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.
- [2] Measured at identical  $V_{CC}$ , temperature and input voltage.
- [3] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical  $V_{CC}$  and temperature.
- [4] Guarantees the LOW level.
- [5] Guarantees the HIGH level.

### 10.1 Test circuits and waveforms



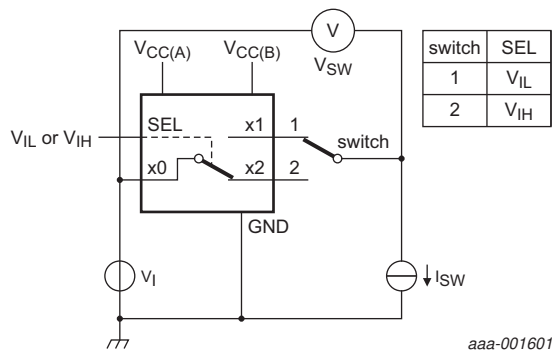
**Fig 3. Test circuit for measuring OFF-state leakage current**





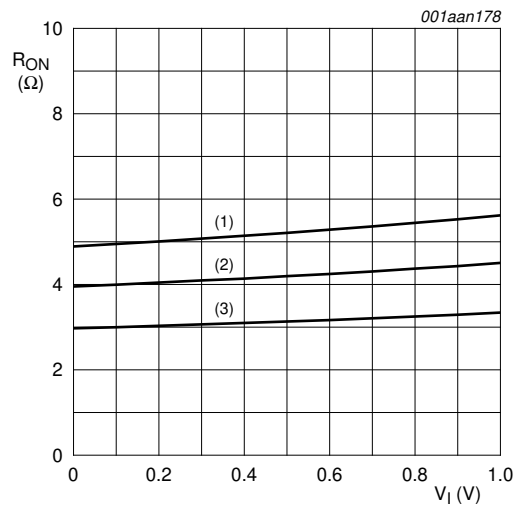
x0 refers to R0, G0, B0, SCL0 or SDA0  
 x1 refers to R1, G1, B1, SCL1 or SDA1  
 x2 refers to R2, G2, B2, SCL2 or SDA2

**Fig 4. Test circuit for measuring ON-state leakage current**



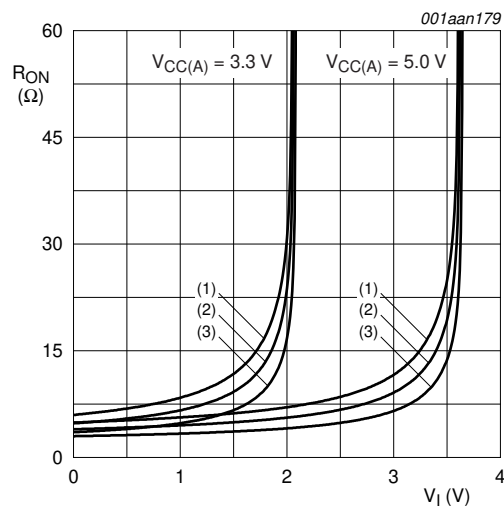
x0 refers to R0, G0, B0, SCL0 or SDA0  
 x1 refers to R1, G1, B1, SCL1 or SDA1  
 x2 refers to R2, G2, B2, SCL2 or SDA2  
 $R_{ON} = V_{SW} / I_{SW}$ .

**Fig 5. Test circuit for measuring ON resistance**



- (1)  $T_{amb} = 85\text{ °C}$
- (2)  $T_{amb} = 25\text{ °C}$
- (3)  $T_{amb} = -40\text{ °C}$

Fig 6. ON resistance as a function of input voltage (RGB switches)



- (1)  $T_{amb} = 85\text{ °C}$
- (2)  $T_{amb} = 25\text{ °C}$
- (3)  $T_{amb} = -40\text{ °C}$

Fig 7. ON resistance as a function of input voltage (DDC switches)

## 11. Dynamic characteristics

**Table 9. Dynamic characteristics**

At recommended operating conditions; Voltages are referenced to GND (ground = 0 V;  $V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{CC(A)} = 2\text{ V to }5.5\text{ V}$ ).

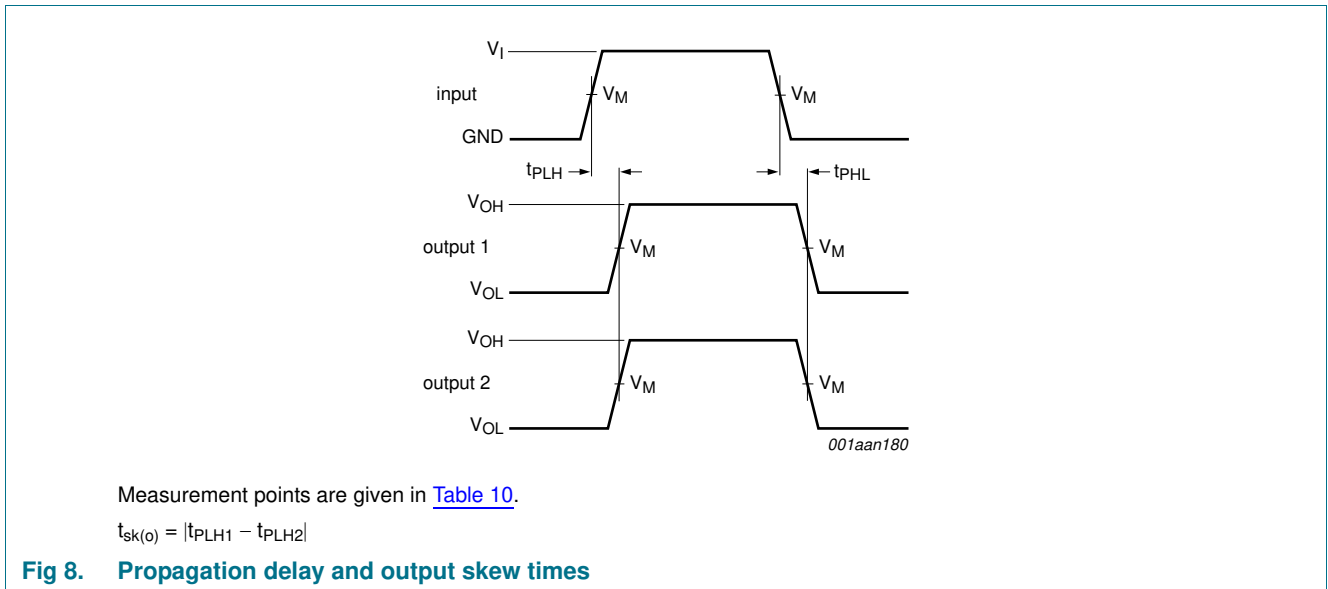
Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$			Unit
			Min	Typ <sup>[1]</sup>	Max	
$t_{pd}$	propagation delay	H0 to H1, H2 and V0 to V1, V2; See <a href="#">Figure 8</a> and <a href="#">Figure 9</a>	-	3	-	ns
$t_{en}$	enable time	SEL to all outputs; See <a href="#">Figure 9</a> , <a href="#">Figure 10</a> and <a href="#">Figure 11</a>	-	15	-	ns
$t_{dis}$	disable time	SEL to all outputs; See <a href="#">Figure 9</a> , <a href="#">Figure 10</a> and <a href="#">Figure 11</a>	-	5	-	ns
$t_{b-m}$	break-before-make time	See <a href="#">Figure 9</a> , <a href="#">Figure 10</a> and <a href="#">Figure 12</a>	-	10	-	ns
$t_{sk(o)}$	output skew time	Skew between any Rn, Gn and Bn ports; see <a href="#">Figure 8</a>	-	50	-	ps

[1] All typical values are measured at  $V_{CC(B)} = 5\text{ V}$ ;  $V_{CC(A)} = 3.3\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ .

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

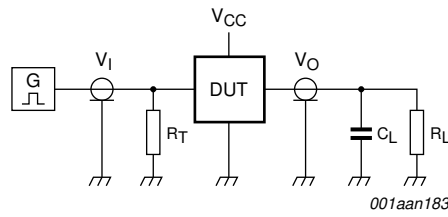
[3] Guaranteed by design.

### 11.1 Test circuits and waveforms



**Table 10. Measurement points**

Input		Output	
$V_M$	$V_I$	$V_X$	$V_M$
$0.5V_{CC(A)}$	GND to $V_{CC(A)}$	$0.9V_{OH}$	$0.5V_{CC(B)}$



Test data is given in [Table 11](#).

Definitions:

DUT = Device Under Test.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

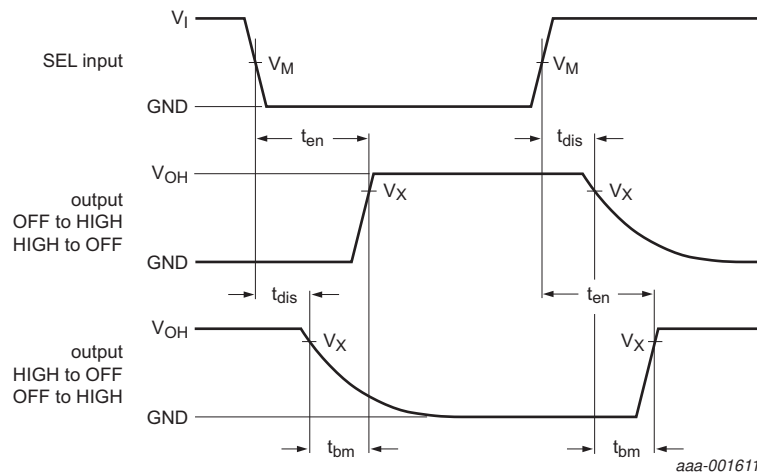
$C_L$  = Load capacitance including test jig and probe.

$R_L$  = Load resistance.

**Fig 9. Test circuit for measuring propagation delay times, enable and disable times (SEL to H1, H2, V1, V2), break-before-make times (H1 to H2, V1 to V2)**

**Table 11. Test data**

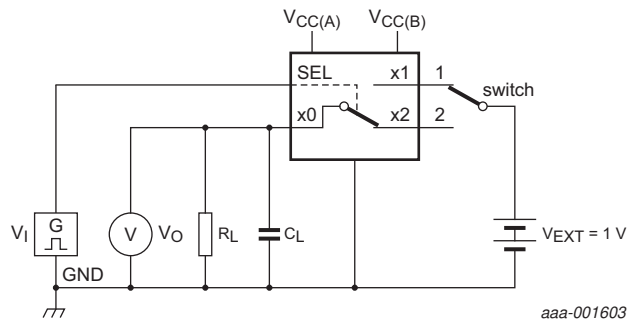
Input	Load	
$t_r, t_f$	$C_L$	$R_L$
$\leq 2.5$ ns	10 pF	1 k $\Omega$



Measurement points are given in [Table 10](#).

Logic level:  $V_{OH}$  is typical output voltage level that occurs with the output load.

**Fig 10. Enable and disable times (all outputs) and break-before-make times**



Test data is given in [Table 12](#).

x0 refers to R0, G0, B0, SCL0, SDA0

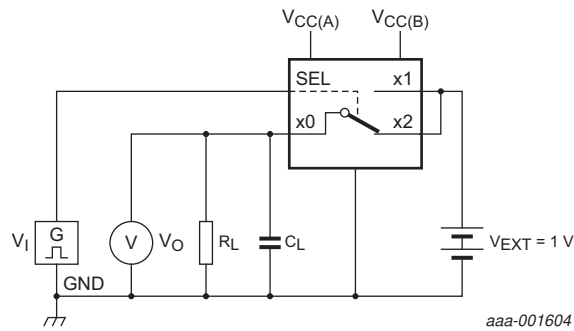
x1 refers to R1, G1, B1, SCL1, SDA1

x2 refers to R2, G2, B2, SCL2, SDA2

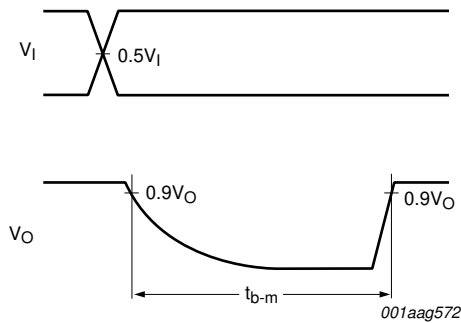
**Fig 11. Test circuit for measuring enable and disable times (SEL to Rn, Gn, Bn, SDAn, SCLn)**

**Table 12. Test data**

Input		Load	
$t_r, t_f$	$V_I$	$C_L$	$R_L$
$\leq 2.5$ ns	GND to $V_{CC(A)}$	10 pF	100 $\Omega$



a. Test circuit



b. Input and output measurement points

Test data is given in [Table 12](#).

x0 refers to R0, G0, B0, SCL0, SDA0

x1 refers to R1, G1, B1, SCL1, SDA1

x2 refers to R2, G2, B2, SCL2, SDA2

**Fig 12. Test circuit for measuring break-before-make time (R1 to R2, G1 to G2, B1 to B2, SCL1 to SCL2, SDA1 to SDA2)**

## 12. Additional dynamic characteristics

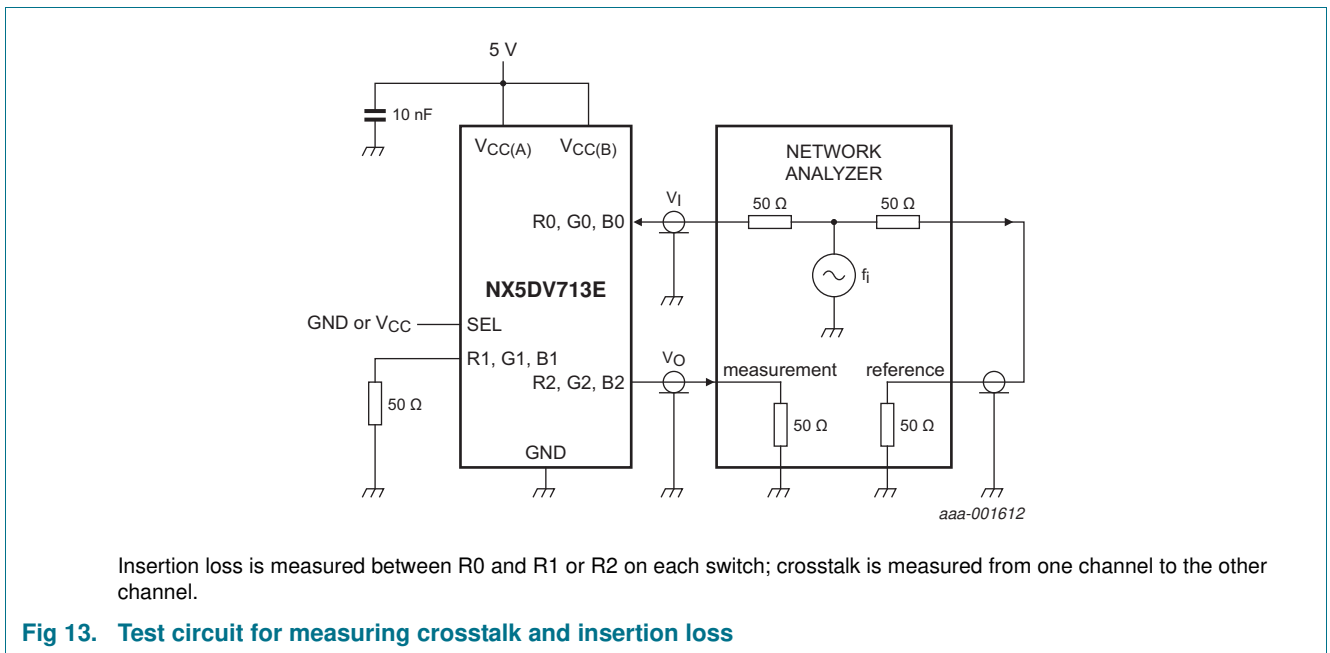
**Table 13. Additional dynamic characteristics**

$V_{CC(B)} = 5.0\text{ V} \pm 10\%$ ,  $V_{CC(A)} = 2\text{ V to } 5.5\text{ V}$ , unless otherwise specified; Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	$T_{\text{amb}} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$			Unit	
			Min	Typ	Max		
$f_{(-3\text{dB})}$	-3 dB frequency response	$R_L = 50\ \Omega$ ; see <a href="#">Figure 13</a>	[1]	-	600	-	MHz
$\alpha_{\text{ins}}$	Insertion loss	$f_i = 1\text{ MHz}$ ; $R_L = R_S = 50\ \Omega$ ; see <a href="#">Figure 13</a>	-	-	0.6	-	dB
Xtalk	crosstalk	between switches; $f_i = 50\text{ MHz}$ ; $R_L = 50\ \Omega$ ; see <a href="#">Figure 13</a>	[1]	-	-50	-	dB

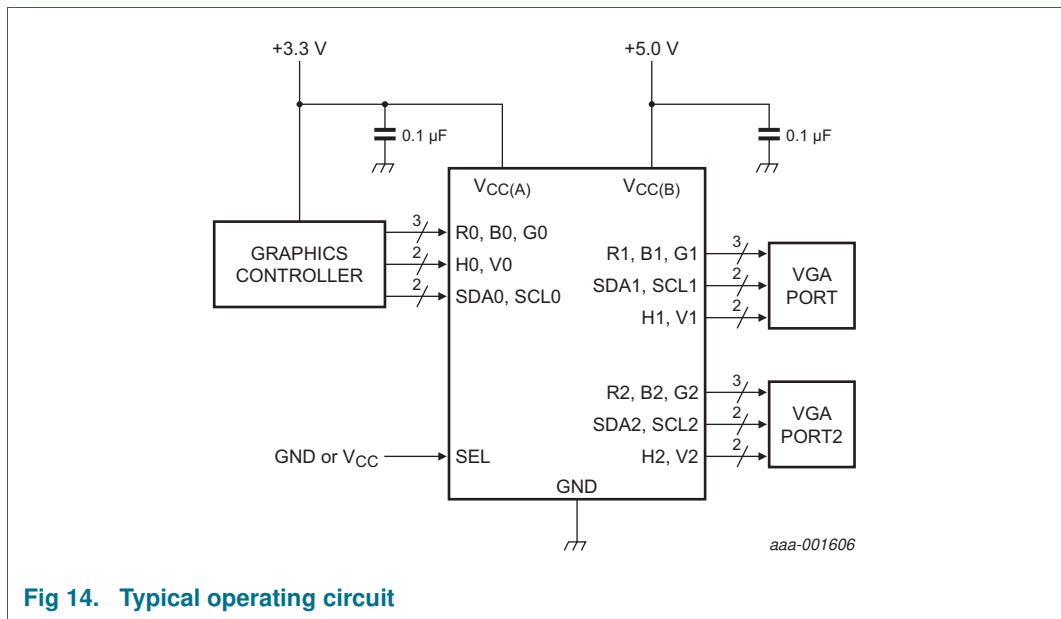
[1]  $f_i$  is biased at  $0.5V_{CC}$ .

### 12.1 Test circuits



**13. Application information**

The NX5DV713E provides the level shifting necessary to drive two standard VGA ports from a graphic controller as low as 2.2 V. Internal buffers drive the HSYNC and VSYNC signals to VGA standard TTL levels. The DDC multiplexer provides level shifting by clamping signals to a diode drop less than  $V_{CC(A)}$  (See [Figure 14](#)). Connect  $V_{CC(A)}$  to 3.3 V for normal operation, or to  $V_{CC(B)}$  to disable voltage clamping for DDC signals



**Fig 14. Typical operating circuit**



14. Package outline

HWQFN32: plastic thermal enhanced very very thin quad flat package; no leads;  
32 terminals; 3 x 6 x 0.75 mm

SOT1180-1

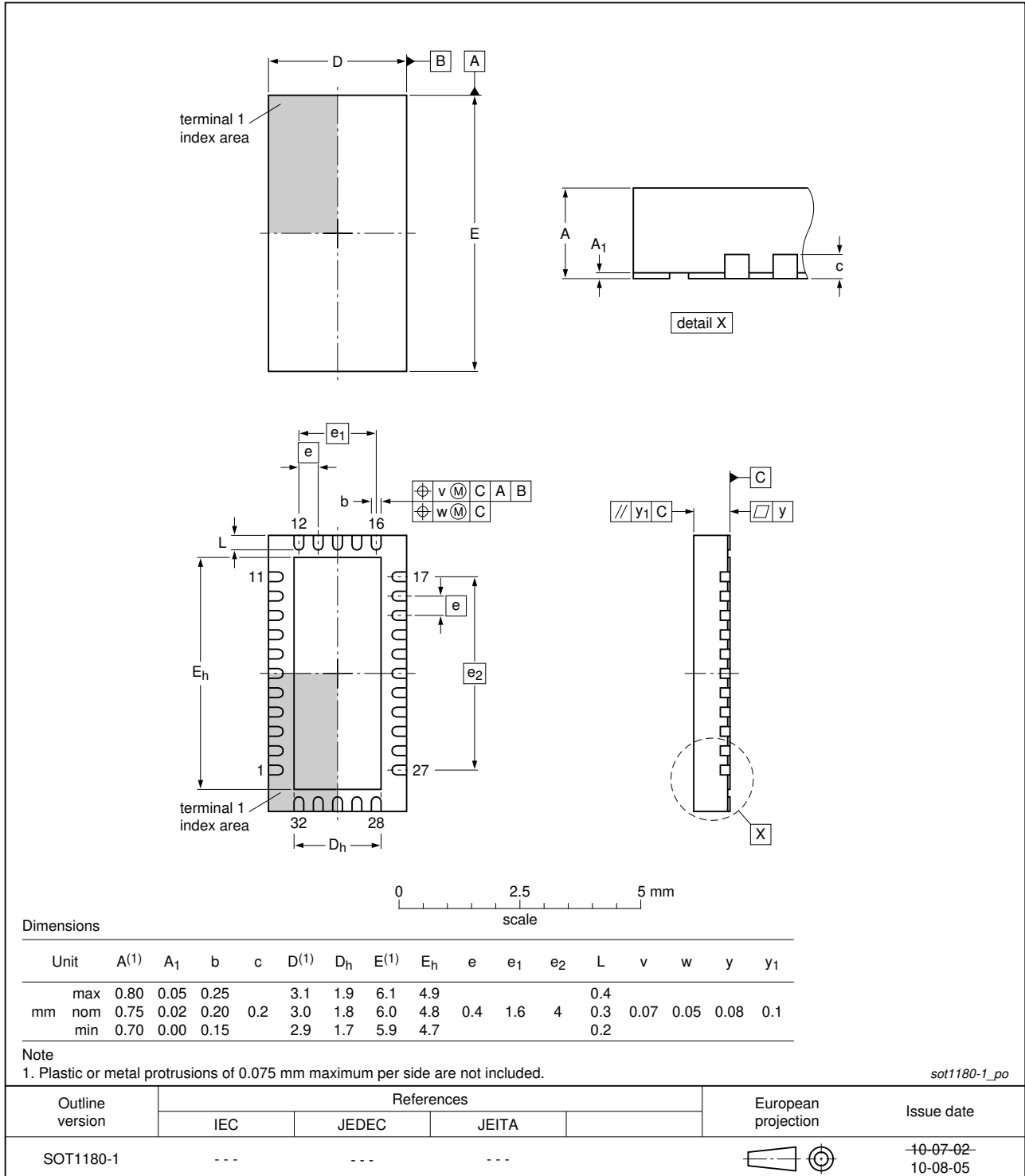


Fig 15. Package outline SOT1180-1 (HWQFN32)

## 15. Abbreviations

Table 14. Abbreviations

Acronym	Description
CDM	Charged Device Model
DDC	Display Data Channel
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
RGB	Red Green Blue
SPDT	Single-Pole Double-Throw
TTL	Transistor-Transistor Logic
VESA	Video Electronics Standards Association

## 16. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX5DV713E v.1	20111124	Product data sheet	-	-

## 17. Legal information

### 17.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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