Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

NX5P3201

3 A USB power switch and 6 A high-side load switch

Rev. 1 — 11 December 2015 Product data sheet

1. General description

The NX5P3201 is an advanced dual power switch consisting of two independent switches. They are, an advanced 3 A bidirectional power switch (SWP) for USB OTG and charger port applications, and a high-side 6 A load switch (SW5).

SWP includes an open-drain status indicator. It also consists of OverTemperature Protection (OTP), UnderVoltage LockOut (UVLO) and OverVoltage LockOut (OVLO) protection circuits. The OVLO circuit isolates the pin VBUS when more than 6.55 V is applied to pin VBUS via the USB connector. To prevent unnecessary switching due to ringing on pins VBUS or PMU, the UVLO circuits include a 15 ms turn-on delay. This deglitch function allows the applied voltage to stabilize above V_{UVLO} before closing SWP.

SW5 consists of OTP, Reverse Current Protection (RCP), and UVLO protection circuits. The UVLO isolates VBAT from VIN until V_I exceeds V_{UVLO}. If the voltage at VBAT exceeds V_I by 30 mV, the RCP circuit isolates VBAT from VIN. It prevents damage to devices on the input side of the switch.

Both switches include slew rate controlled inrush current reduction to prevent damage when switching high capacitive loads.

2. Features and benefits

- 28 V tolerant VBUS supply pin
- Wide supply voltage range from 3.4 V to 6.55 V for SWP and 2.7 V to 5.5 V for SW5
- Automatic SWP operation
- I_{SW} continuous current: 3 A for SWP and 6 A for SW5
- Low ON resistance: 32 mΩ (typical) for SWP and 8 mΩ (typical) for SW5
- Soft-start, slew rate controlled turn-on time
- Status indicator output
- Protection circuitry
  - Reverse current protection
  - Overtemperature protection
  - Overvoltage lockout
  - Undervoltage lockout
- ESD protection:
  - IEC61000-4-2 contact discharge exceeds 8 kV for pin VBUS
  - HBM JS-001-2012 class 3 A exceeds 4 kV
- IEC61000-4-5 surge test exceeds 100 V for pin VBUS
- Specified from −40 °C to +85 °C ambient temperature

3. Applications

- Smartphone and feature phones
- Tablets and e-books

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
NX5P3201CUK	WLCSP30	wafer level chip-scale package; 30 bumps; 2.26 × 2.56 × 0.51 mm (backside coating included)	SOT1443-2

5. Marking

Table 2. Marking codes

Type number	Marking code
NX5P3201CUK	5P32C

6. Functional diagram

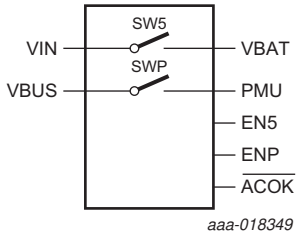


Fig 1. Logic symbol

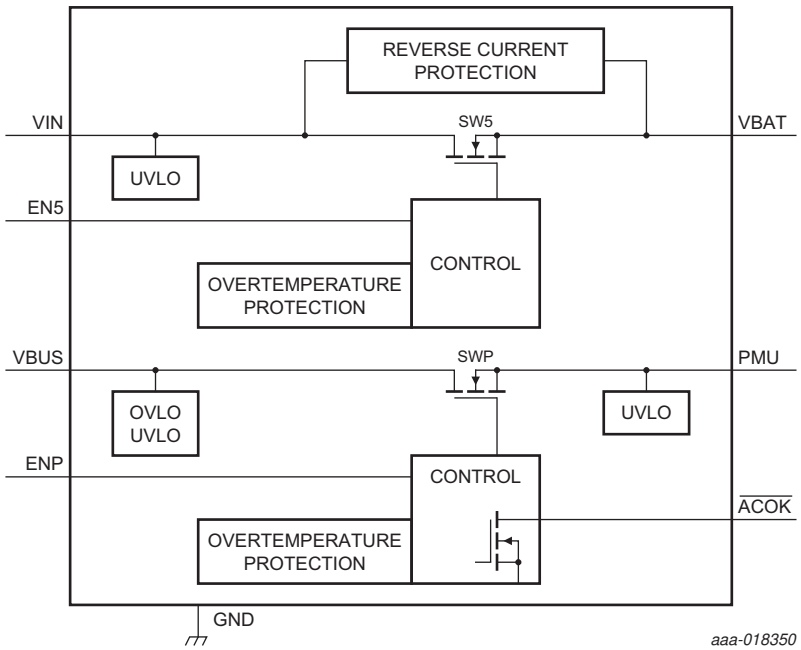


Fig 2. Block diagram (simplified schematic)

7. Pinning information

7.1 Pinning

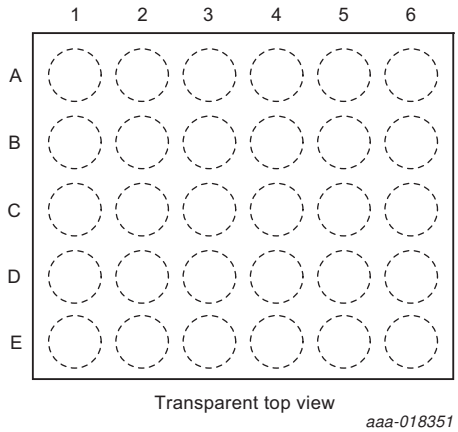


Fig 3. Pin configuration WLCSP30 package

	1	2	3	4	5	6
A	VIN	VBAT	VBAT	VBAT	VBAT	n.c.
B	VIN	VIN	VIN	VIN	VBAT	$\overline{\text{ACOK}}$
C	EN5	GND	VBUS	VBUS	PMU	PMU
D	GND	GND	VBUS	VBUS	PMU	PMU
E	ENP	GND	VBUS	VBUS	VBUS	PMU

Transparent top view

aaa-018352

Fig 4. Ball mapping for WLCSP30

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VBUS	C3, C4, D3, D4, E3, E4, E5	power switch (SWP) input/output
PMU	C5, C6, D5, D6, E6	power switch (SWP) input/output
VIN	A1, B1, B2, B3, B4	load switch (SW5) input
VBAT	A2, A3, A4, A5, B5	load switch (SW5) output
$\overline{ACOK}$	B6	status indicator (open drain; active LOW)
GND	C2, D1, D2, E2	ground (0 V)
EN5	C1	load switch (SW5) enable input (active HIGH)
n.c.	A6	not connected[1]
ENP	E1	power switch (SWP) enable input (active HIGH)

[1] Internally pulled down to GND.

8. Functional description

Table 4. Function table for power switch (SWP)[1]

ENP	VBUS	PMU	$\overline{ACOK}$	Operation mode
H	$V_{UVLO} < V_{BUS} < V_{OVLO}$	$< V_{UVLO}$	L	enable; power switch (SWP) closed; USB charging mode
H	$< V_{UVLO}$	$> V_{UVLO}$	L	enable; power switch (SWP) closed; USB OTG mode
H	$< V_{UVLO}$	$< V_{UVLO}$	Z	undervoltage lockout; power switch (SWP) open
H	X	X	Z	overtemperature protection; power switch (SWP) open
H	$> V_{OVLO}$	X	Z	overvoltage lockout; power switch (SWP) open
L	X	X	Z	disable; power switch (SWP) open

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state; X = don't care.

Table 5. Function table for load switch (SW5)[1]

EN5	VIN	VBAT	Operation mode
H	$< V_{UVLO}$	X	undervoltage lockout; load switch (SW5) open
H	$> V_{UVLO}$	V_I	enable; load switch (SW5) closed; high current mode
H	X	X	overtemperature protection; load switch (SW5) open
H	$V_I < V_{BAT} - 35$ mV	X	reverse bias current or backdrive current; load switch (SW5) open
L	X	X	disable; load switch (SW5) open

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

8.1 Enable inputs

If protection circuits corresponding to load switch (SW5) are inactive, the EN5 enable input controls the load switch (SW5). Similarly, if protection circuits corresponding to power switch (SWP) are inactive, the ENP enable input controls the power switch (SWP).

8.2 UnderVoltage LockOut (UVLO)

The UVLO circuit disables SWP when V_{BUS} and $V_{sup} < V_{UVLO}$. Once either V_{BUS} or V_{sup} exceeds V_{UVLO} for 15 ms, and no other protection circuits are active, the ENP controls SWP.

An UVLO circuit disables SW5 when $V_I < V_{UVLO}$. Once $V_I > V_{UVLO}$ and no other protection circuits are active, EN5 controls the state of SW5.

8.3 OverVoltage LockOut (OVLO)

When $V_{BUS} > 6.55$ V, the OVLO circuit disables SWP and sets the $\overline{ACOK}$ output to high-impedance state. Once $V_{BUS} < 6.45$ V and no other protection circuits are active, $\overline{ACOK}$ is set to LOW and ENP controls SWP.

8.4 OverTemperature Protection (OTP)

If SWP exceeds 130 °C, its OTP circuit disables it and sets the $\overline{ACOK}$ output to high-impedance state. Once the temperature decreases below 110 °C and no other protection circuits are active, if ENP is HIGH, then $\overline{ACOK}$ is set to LOW.

The OTP circuit of SW5 protects SW5. However, it does not control the $\overline{ACOK}$ output. When the OTP circuit is deactivated, EN5 determines the state of SW5.

8.5 $\overline{ACOK}$ output

The $\overline{ACOK}$ output is an open-drain output that requires an external pull-up resistor. If SWP is closed, the $\overline{ACOK}$ output is set to LOW. If the OVLO, UVLO or OTP circuits of SWP are activated, or ENP is LOW, $\overline{ACOK}$ is set to a high-impedance state. An external pull-up resistor of value between 10 kΩ to 200 kΩ is connected to $\overline{ACOK}$.

8.6 Reverse Current Protection (RCP)

When EN5 is HIGH, if $V_I < (V_{BAT} - 35$ mV) for longer than 4 ms, the RCP circuit disables SW5. Once $V_I > V_{BAT}$ for longer than 4 ms and no other protection circuits are active, EN5 determines the state of SW5.

9. Application design-in information

The NX5P3201 typically connects a USB port in a portable battery operated device. The $\overline{ACOK}$ signal requires an additional external pull-up resistor which should be connected to a voltage source matching the logic level of the controller.

Slew rate controlled inrush current reduction circuits function during switching. Once a switch is enabled, any large current generated through a change in load is not recognized as inrush current.

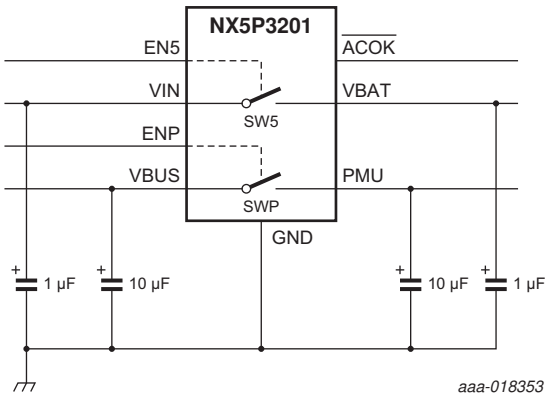


Fig 5. Test setup for ESD conformance to electrostatic discharge immunity test

10. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage	on pin VBUS	[1]	−0.5	+29	V
		on pin PMU	[1]	−0.5	+6.75	V
		on pin VIN	[1]	−2.0	+6.0	V
		on pins EN5 and ENP	[1]	−0.5	+6.0	V
V_O	output voltage	on pins VBAT and $\overline{ACOK}$	[2][3]	−0.5	+6.0	V
I_{IK}	input clamping current	on pins EN5 and ENP		−50	-	mA
I_{SK}	switch clamping current	on pins VIN, VBUS, PMU, and VBAT; $V_I < -0.5$ V		−50	-	mA
I_{SW}	switch current	T_{amb} = 85 °C; power switch (SWP)		-	3	A
		T_{amb} = 85 °C; load switch (SW5)		-	6	A
I_{SWM}	peak switch current	t_p = 1 ms; f_{sw} = 217 Hz (GSM calibration)		-	9	A
		t_p = 100 µs; f_{sw} = 217 Hz (with rising time 100 µs)		-	11	A
T_j	junction temperature			−40	+125	°C
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation		[4]	-	400	mW

[1] If the switch clamping current rating is observed, the minimum and maximum switch voltage ratings may be exceeded.

[2] If the input current rating is observed, the minimum input voltage rating may be exceeded.

[3] EN5 can be connected to VIN. In this condition, the minimum input voltage value is −2.0 V for EN5.

[4] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed at lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 85 °C and the use of a two-layer PCB.

11. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	on pin VBUS	3.4	28	V
		on pin VIN	2.7	5.5	V
		on pin PMU	3.4	5.5	V
		on pins EN5 and ENP	0	5.5	V
V_O	output voltage	on pins $\overline{ACOK}$ and VBAT	0	5.5	V
T_{amb}	ambient temperature		−40	+85	°C

12. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	99	K/W

[1] $R_{th(j-a)}$ is dependent upon board layout. To minimize $R_{th(j-a)}$, all pins should have a solid connection to larger copper layer areas. In multi-layer PCBs, the second layer should be used to create a large heat spreader area below the device. Avoid using solder-stop varnish under the device.

13. Static characteristics

Table 9. Static characteristics for power switch (SWP)

V_{BUS} or V_{sup} = 4.0 V to 5.5 V unless otherwise specified; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	on pin ENP	1.2	-	-	1.2	-	V
V_{IL}	LOW-level input voltage	on pin ENP	-	-	0.4	-	0.4	V
V_{OL}	LOW-level output voltage	on pin $\overline{ACOK}$; I_O = 4 mA	-	-	0.35	-	0.4	V
I_q	quiescent current	on pin VBUS						
		SWP closed; I_O = 0 A; see Figure 6	-	220	-	-	350	µA
		SWP open; ENP = LOW; V_{BUS} = 0 V to 5.5 V	-	8	-	-	16	µA
		on pin PMU						
		SWP closed; I_O = 0 A; see Figure 7	-	220	-	-	260	µA
		SWP open; ENP = LOW; V_{sup} = 0 V to 5.5 V	-	8	-	-	16	µA
$I_{S(OFF)}$	OFF-state leakage current	VBUS output; ENP = LOW; V_{sup} = 5.5 V; V_{BUS} = 0 V to 28 V	-	26	-	-	35	µA
		PMU output; ENP = LOW; V_{BUS} = 28 V; V_{sup} = 0 V to 5.5 V	-	5	-	-	10	µA

Table 9. Static characteristics for power switch (SWP) *…continued*

V_{BUS} or V_{sup} = 4.0 V to 5.5 V unless otherwise specified; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{UVLO}	undervoltage lockout voltage	on pins VBUS and PMU	-	3.2	-	3.0	3.4	V
$V_{hys(UVLO)}$	undervoltage lockout hysteresis voltage	on pins VBUS and PMU	-	100	-	90	110	mV
V_{OVLO}	overvoltage lockout voltage	on pin VBUS	-	6.55	-	6.2	6.9	V
$V_{hys(OVLO)}$	overvoltage lockout hysteresis voltage	on pin VBUS	-	100	-	90	110	mV
$C_{S(ON)}$	ON-state capacitance	on pins VBUS and PMU	-	-	1.0	-	1.0	nF

[1] All typical values are measured at V_{BUS} or V_{sup} = 5.0 V unless otherwise specified.

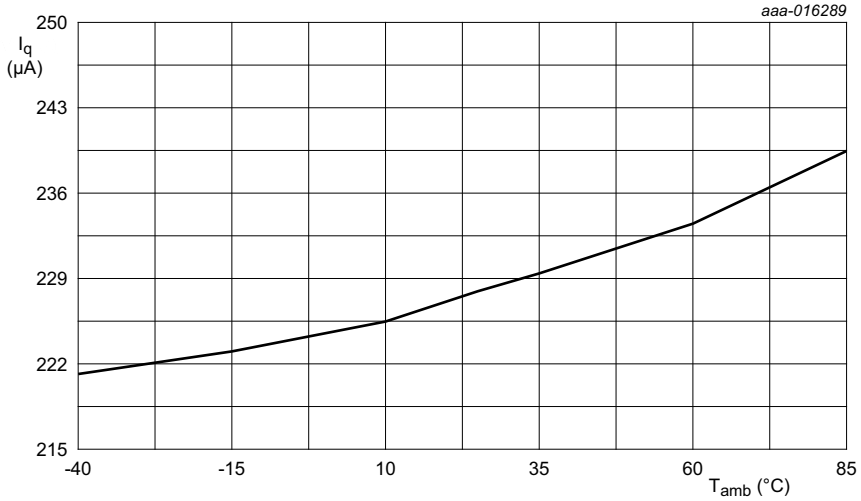
Table 10. Static characteristics for load switch (SW5)

V_I = 2.7 V to 5.5 V unless otherwise specified; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	EN5 input	-	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	EN5 input	-	-	-	-	0.6	V
I_I	input leakage current	EN5 input; $V_{en(lsw)}$ = 0 V to 5.5 V	-	-	-	-	0.1	µA
$V_{th(RCP)}$	RCP threshold voltage	$V_{th(RCP)} = V_{BAT} - V_I$	-	30	-	10	55	mV
$V_{th(RCP)hys}$	RCP threshold voltage hysteresis		-	35	-	10	60	mV
V_{UVLO}	undervoltage lockout voltage	on pin VIN; EN5 = HIGH	-	2.5	-	2.35	2.7	V
I_q	quiescent current	on pin VIN; I_O = 0 A						
		EN5 = HIGH; see Figure 8	-	90	-	-	150	µA
		EN5 = LOW; see Figure 8	-	10	-	-	15	µA
I_{OFF}	power-off leakage current	V_{BAT} = 0 V to 5.5 V; V_I = 0 V; see Figure 11	-	-	-	-	5.0	µA
$I_{S(OFF)}$	OFF-state leakage current	VBAT output; EN5 = LOW; V_I = 5.5 V; V_{BAT} = 0 V to 5.5 V; see Figure 12	-	-	-	–4.5	+2.0	µA
$C_{S(ON)}$	ON-state capacitance	on pins VIN and VBAT	-	-	0.5	-	0.5	nF

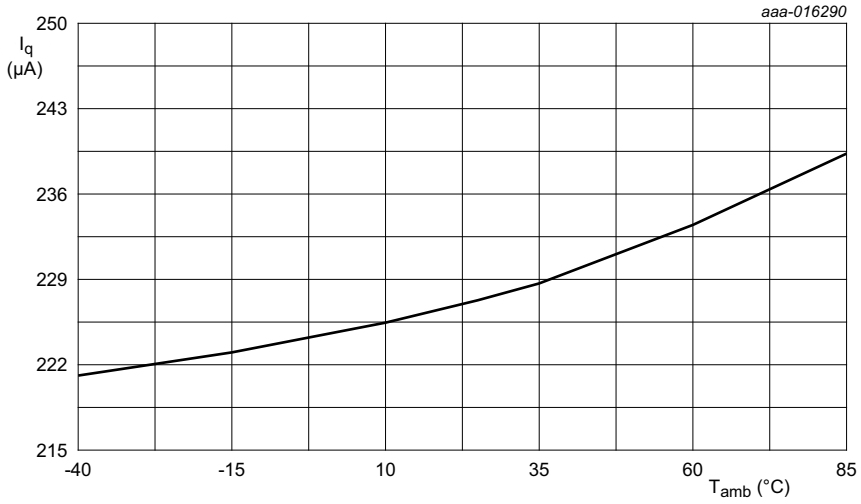
[1] All typical values are measured at V_I = 3.0 V unless otherwise specified.

13.1 Graphs



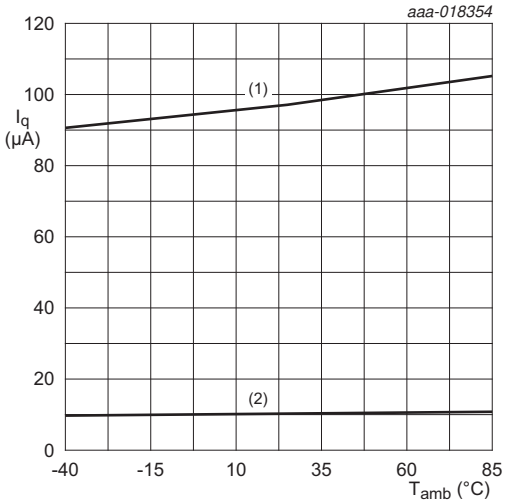
V_{BUS} = 5.5 V; I_O = 0 A; ENP = HIGH.

Fig 6. I_q versus temperature



V_{sup} = 5.5 V; I_O = 0 A; ENP = HIGH.

Fig 7. I_q versus temperature

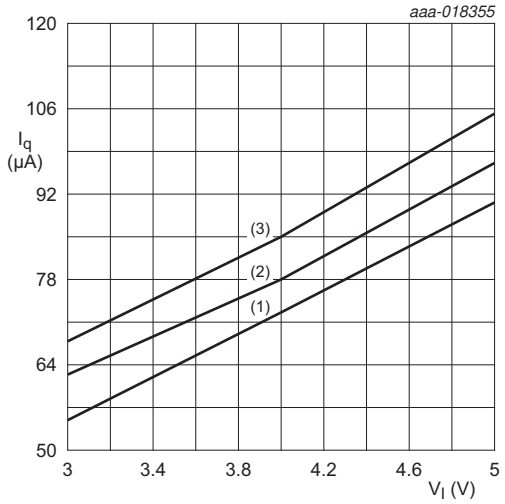


V_I = 5.0 V; I_O = 0 A.

(1) EN5 = HIGH

(2) EN5 = LOW

Fig 8. I_q versus temperature



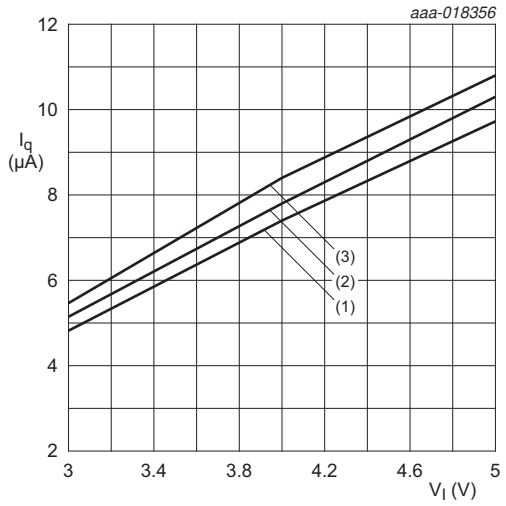
I_O = 0 A.

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 85 °C

Fig 9. I_q versus V_I (EN5 = HIGH)



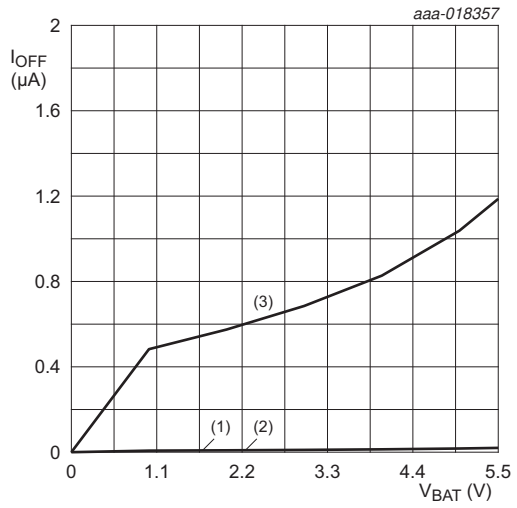
I_O = 0 A.

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 85 °C

Fig 10. I_q versus V_I (EN5 = LOW)



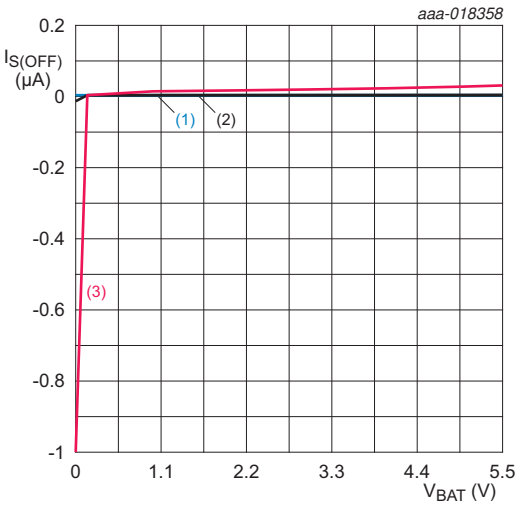
V_I = 0 V.

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 85 °C

Fig 11. I_{OFF} versus V_{BAT}



V_I = 5.5 V.

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 85 °C

Fig 12. $I_{S(OFF)}$ versus V_{BAT}

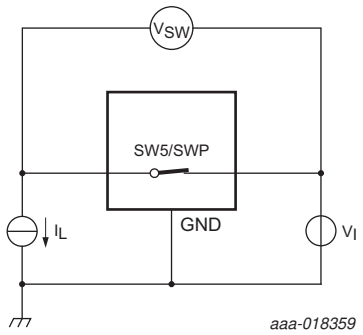
13.2 ON resistance

Table 11. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

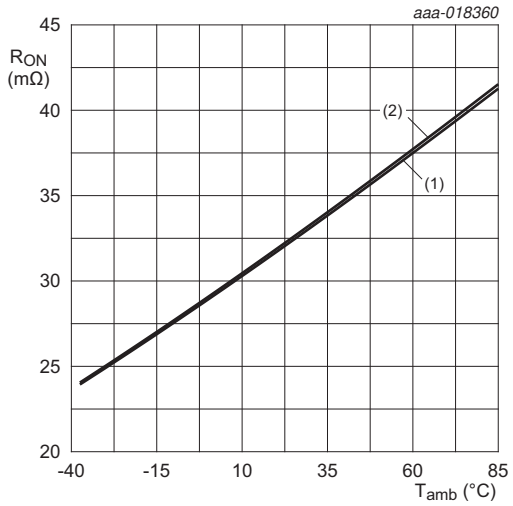
Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
R_{ON}	ON resistance	SWP; V_I = V_{BUS} or V_{sup} = 4.0 V to 5.5 V; see Figure 13, Figure 14, and Figure 16						
		I_L = 200 mA	-	32	-	-	50	mΩ
		I_L = 1.5 A	-	32	-	-	50	mΩ
		SW5; V_I = 3.0 V to 5.5 V; see Figure 13, Figure 15, and Figure 17						
		I_L = 200 mA	-	8	-	-	13	mΩ
		I_L = 1.5 A	-	8	-	-	13	mΩ

13.3 ON resistance test circuit and waveforms



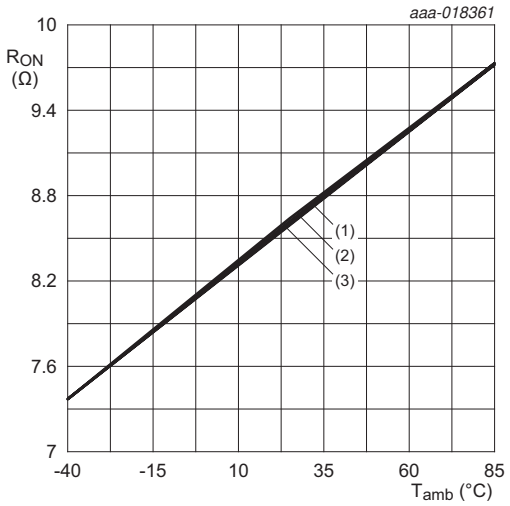
$R_{ON} = V_{SW} / I_L$.

Fig 13. Test circuit for measuring ON resistance



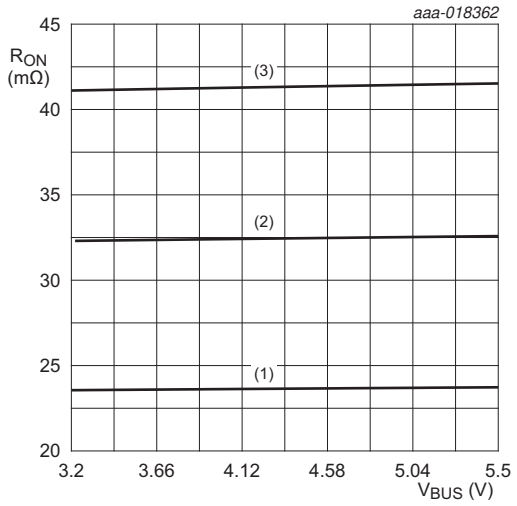
(1) V_I = 4.0 V
(2) V_I = 5.0 V

Fig 14. ON resistance versus temperature (SWP)



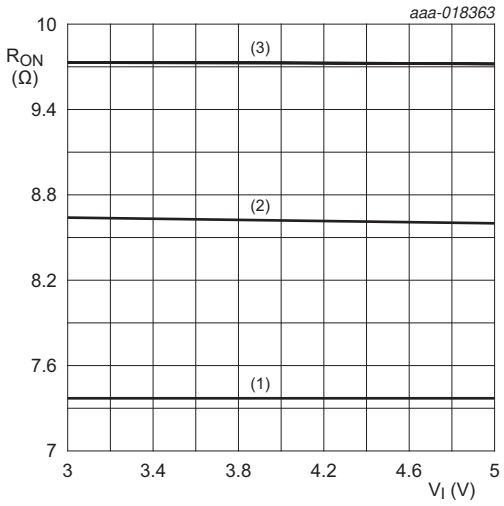
(1) V_I = 3.0 V
(2) V_I = 4.0 V
(3) V_I = 5.0 V

Fig 15. ON resistance versus temperature (SW5)



(1) T_{amb} = −40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 85 °C

Fig 16. ON resistance versus bus supply voltage (SWP)



(1) T_{amb} = −40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 85 °C

Fig 17. ON resistance versus input voltage (SW5)

14. Dynamic characteristics

Table 12. Dynamic characteristics for power switch (SWP)

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); R_L = 100 Ω; C_L = 0.1 μF; unless otherwise specified; for test circuit, see Figure 18 and Figure 20.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t_{deb}	debounce time	V_{BUS} to V_{sup}; 4.0 V < V_{BUS} < 5.5 V	-	14	-	9	19	ms
		V_{sup} to V_{BUS}; 4.0 V < V_{sup} < 5.5 V	-	14	-	9	19	ms
t_{TLH}	LOW to HIGH output transition time	on pins PMU and VBUS; C_L = 100 μF						
		V_{BUS} = 5.0 V	-	2	-	1.5	3.0	ms
		V_{sup} = 5.0 V	-	6	-	1.65	7	ms
t_{dis}	disable time	on pins PMU and VBUS						
		V_{BUS} = 3.0 V	-	3.5	-	2.2	6.0	μs
		V_{sup} = 3.0 V	-	5	-	4	5.5	μs
$t_{start(soft)}$	soft-start time	on pins PMU and VBUS; V_I = V_{BUS} or V_{sup} = 5.0 V	-	26.5	-	-	-	ms

Table 13. Dynamic characteristics for load switch (SW5)

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); R_L = 100 Ω; C_L = 0.1 μF; unless otherwise specified; for test circuit, see Figure 19 and Figure 20.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{en}	enable time	pin EN5 to pin VBAT	-	2.4	-	0.9	3.0	ms
t_{dis}	disable time	pin EN5 to pin VBAT	-	50	-	40	55	μs
t_{TLH}	LOW to HIGH output transition time	on pin VBAT; R_L = 125 Ω; C_L = 1 μF	-	4	-	1.8	4.5	ms
t_{THL}	HIGH to LOW output transition time	on pin VBAT; R_L = 40 Ω; C_L = 100 μF	-	8.0	-	-	8.5	ms

[1] All typical values are measured at V_I = 5.0 V.

14.1 Waveforms and test circuits

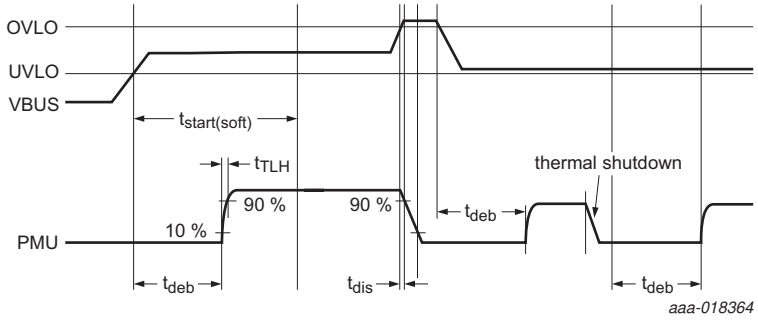
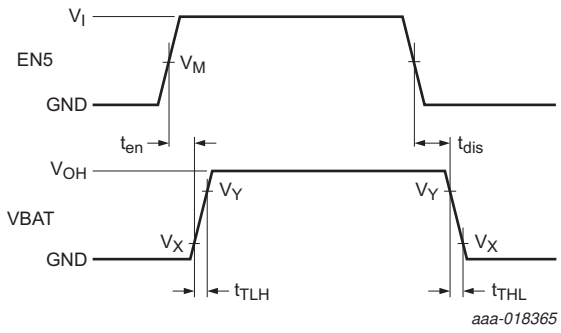


Fig 18. SWP switching time



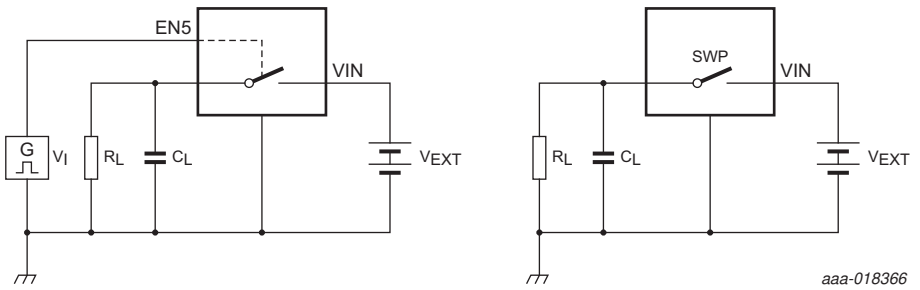
Measurement points are given in Table 14.

Logic level: V_{OH} is the typical output voltage that occurs with the output load.

Fig 19. SW5 switching time

Table 14. Measurement points

Input		Output	
V_I	V_M	V_X	V_Y
5.0 V	0.5 × V_I	0.1 × V_{OH}	0.9 × V_{OH}



Test data is given in Table 15.

Definitions for test circuit:

R_L = Load resistance.

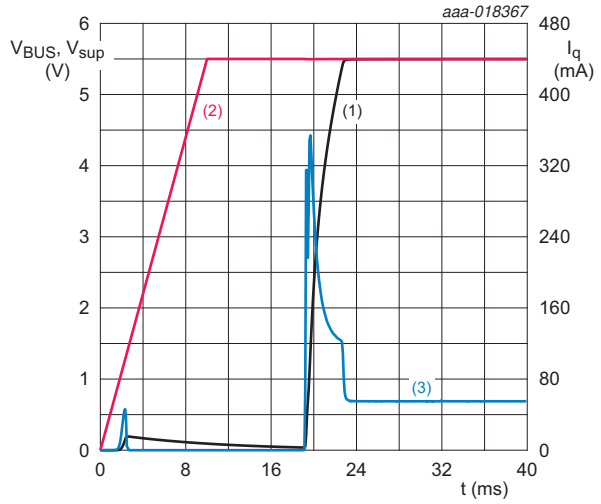
C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Fig 20. Test circuits for measuring switching times

Table 15. Test data

Supply voltage	Input	Load	
V_{EXT}	V_I	C_L	R_L
3.0 V to 5.5 V	2.0 V	0.1 μF	100 Ω



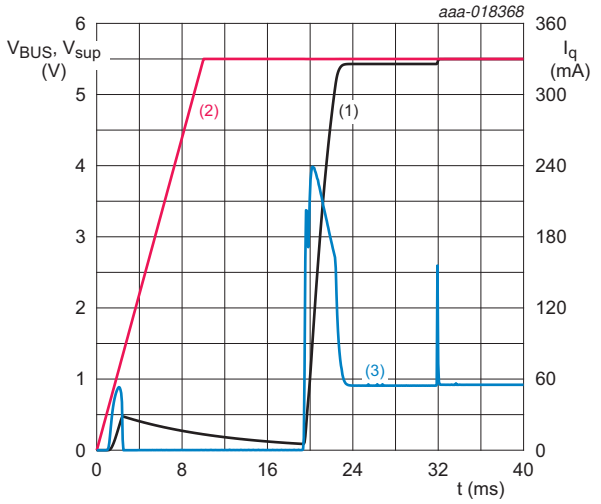
R_L = 100 Ω; C_L = 100 µF; T_{amb} = 25 °C.

(1) V_{sup}

(2) V_{BUS}

(3) I_q on pin VBUS

Fig 21. Waveform showing the enable time versus inrush current (SWP)



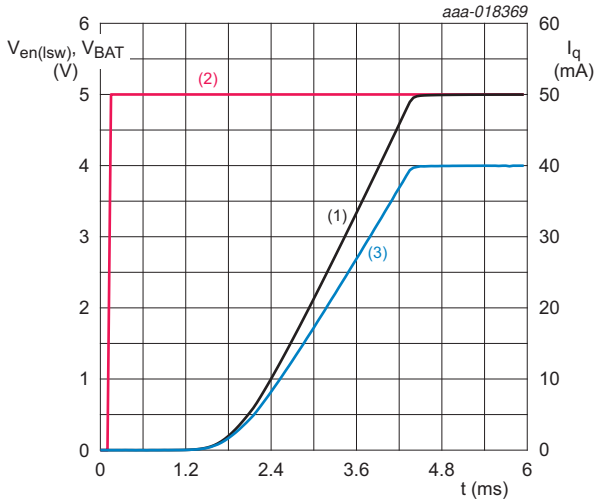
R_L = 100 Ω; C_L = 100 µF; T_{amb} = 25 °C.

(1) V_{BUS}

(2) V_{sup}

(3) I_q on pin PMU

Fig 22. Waveform showing the enable time versus inrush current (SWP)



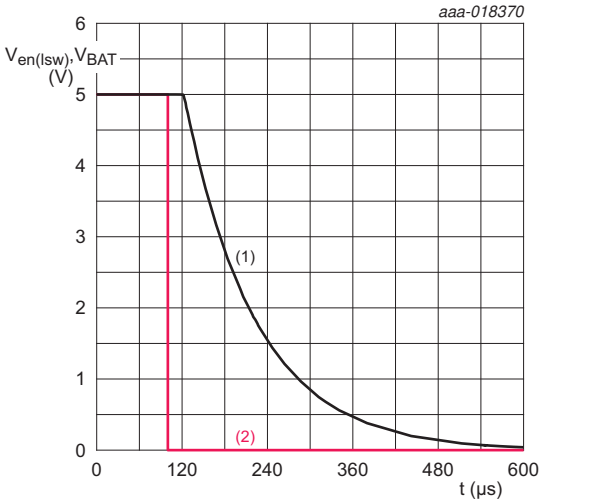
R_L = 100 Ω; C_L = 0.1 µF; T_{amb} = 25 °C.

(1) V_{BAT}

(2) $V_{en(lsw)}$

(3) I_q on pin VIN

Fig 23. Waveform showing the enable time versus inrush current (SW5)



R_L = 100 Ω; C_L = 0.1 µF; T_{amb} = 25 °C.

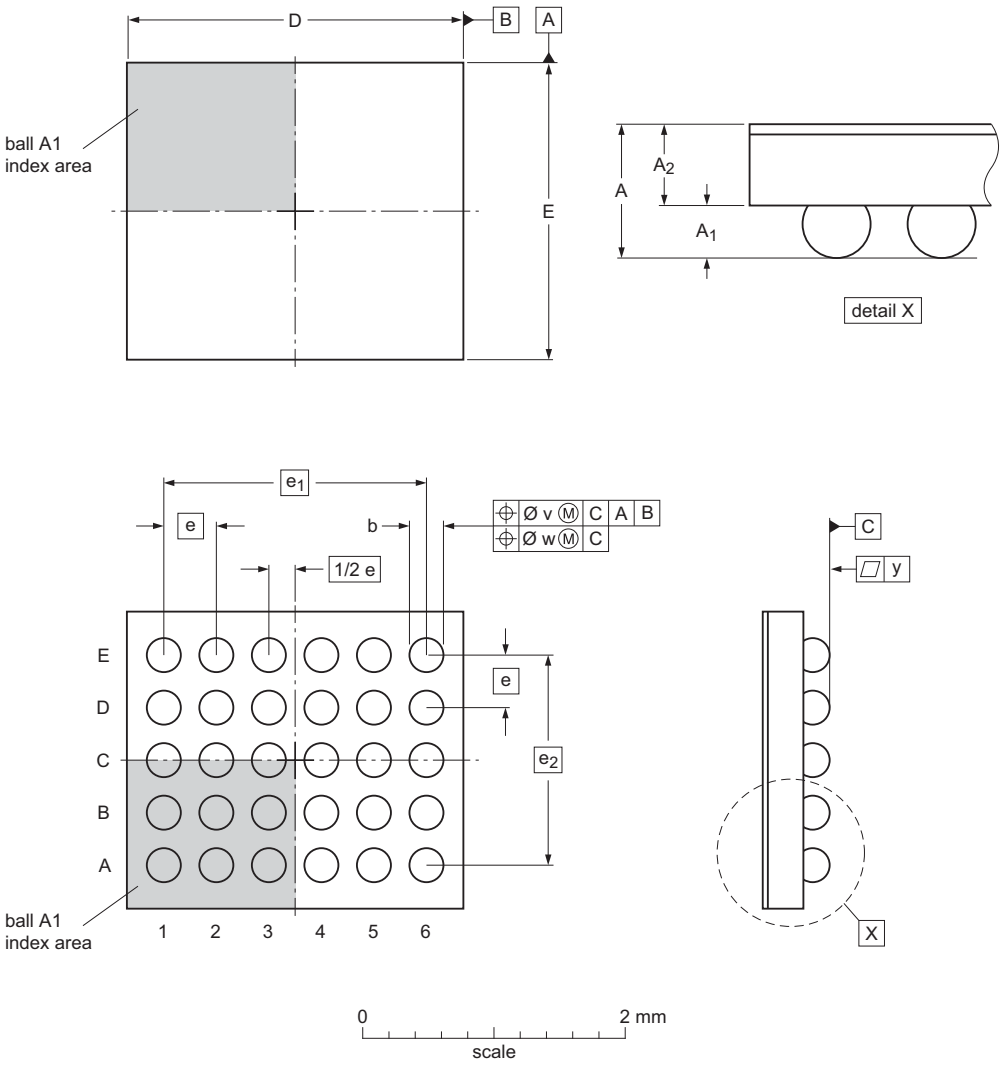
(1) V_{BAT}

(2) $V_{en(lsw)}$

Fig 24. Waveform showing the disable time (SW5)

15. Package outline

WLCSP30: wafer level chip-scale package; 30 bumps; 2.26 x 2.56 x 0.51 mm (backside coating included) **SOT1443-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	max	0.55	0.23	0.34	0.29	2.59	2.29						
	nom	0.51	0.20	0.31	0.26	2.56	2.26	0.4	2.0	1.6	0.05	0.015	0.03
	min	0.47	0.17	0.29	0.23	2.53	2.23						

Note: Backside coating 40 µm

sot1443-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1443-2		- - -				~~15-06-10~~ 15-06-11

Fig 25. Package outline SOT1443-2 (WLCSP30)

16. Soldering of WLCSP packages

16.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

16.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

16.3 Reflow soldering

Key characteristics in reflow soldering are:

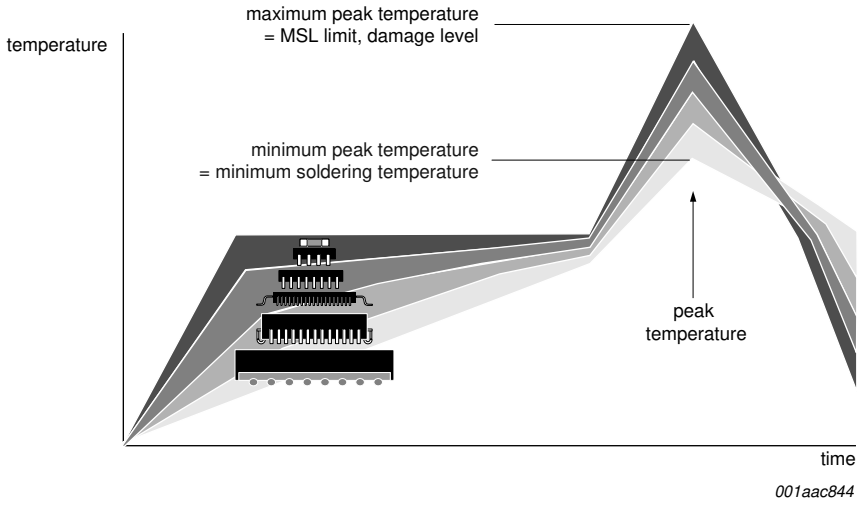
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 26) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 16.

Table 16. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 26.



MSL: Moisture Sensitivity Level

Fig 26. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

16.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

16.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

16.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

16.3.4 Cleaning

Cleaning can be done after reflow soldering.

17. Abbreviations

Table 17. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
HBM	Human Body Model
OTP	OverTemperature Protection
OVLO	OverVoltage LockOut
PCB	Printed-Circuit Board
RCP	Reverse Current Protection
USB OTG	Universal Serial Bus On-The-Go
UVLO	UnderVoltage LockOut
WLCSP	Wafer Level Chip Scale Package

18. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX5P3201 v.1	20151211	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

19.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

19.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

19.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

20. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

21. Tables

22. Figures

23. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 11 December 2015
Document identifier: NX5P3201