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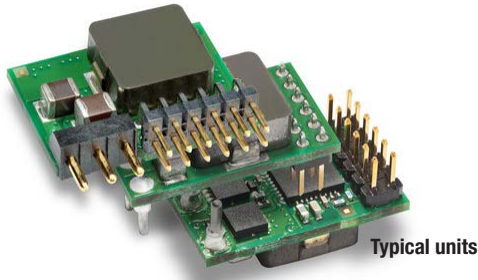
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Discontinued

PRODUCT OVERVIEW

The OKDx-T/12-W12 is a high efficiency, digital Point-of-Load (PoL) DC-DC power converter capable of delivering 12A/60W. Designed for a minimal footprint, the high power-density module measures just 20.8 x 7.6 x 15.6 mm (0.82 x 0.3 x 0.612 in) (SIP version).

PMBus™ compatibility allows monitoring and configuration of critical system level performance

requirements. Apart from standard PoL performance and safety features like OVP, OCP, OTP, and UVLO, these digital converters have advanced features: Adaptive compensation of PWM control loop, fast loop transient response, synchronization, and phase spreading. These converters are ideal for use in telecommunications, networking, and distributed power applications

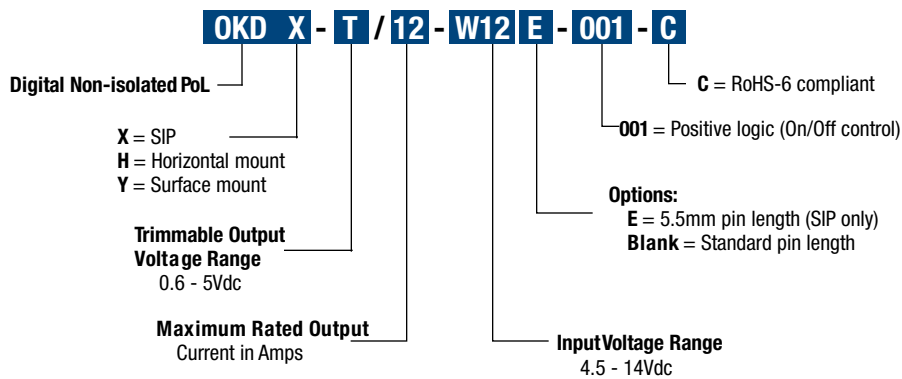
FEATURES

- SIP, Horizontal mount, or SMT package
- 4.5 to 14Vdc Input voltage range
- 0.6 to 5.0Vdc Output voltage range, up to 12A
- High efficiency, typ. 97.1% at 5Vin, 3.3Vout ½ load
- Configuration and Monitoring via PMBus™
- Synchronization & Phase Spreading
- Voltage Tracking & Voltage margining
- MTBF 21.2 Mh

ORDERING GUIDE

Model Number	Package Type	Input	Output
OKDX-T/12-W12-001-C	SIP	4.5-14V	0.6-5.0V, 12A / 60W
OKDX-T/12-W12E-001-C	SIP		
OKDH-T/12-W12-001-C	Horizontal Mount TH		
OKDY-T/12-W12-001-C	Surface Mount		

PART NUMBER STRUCTURE



Absolute Maximum Ratings

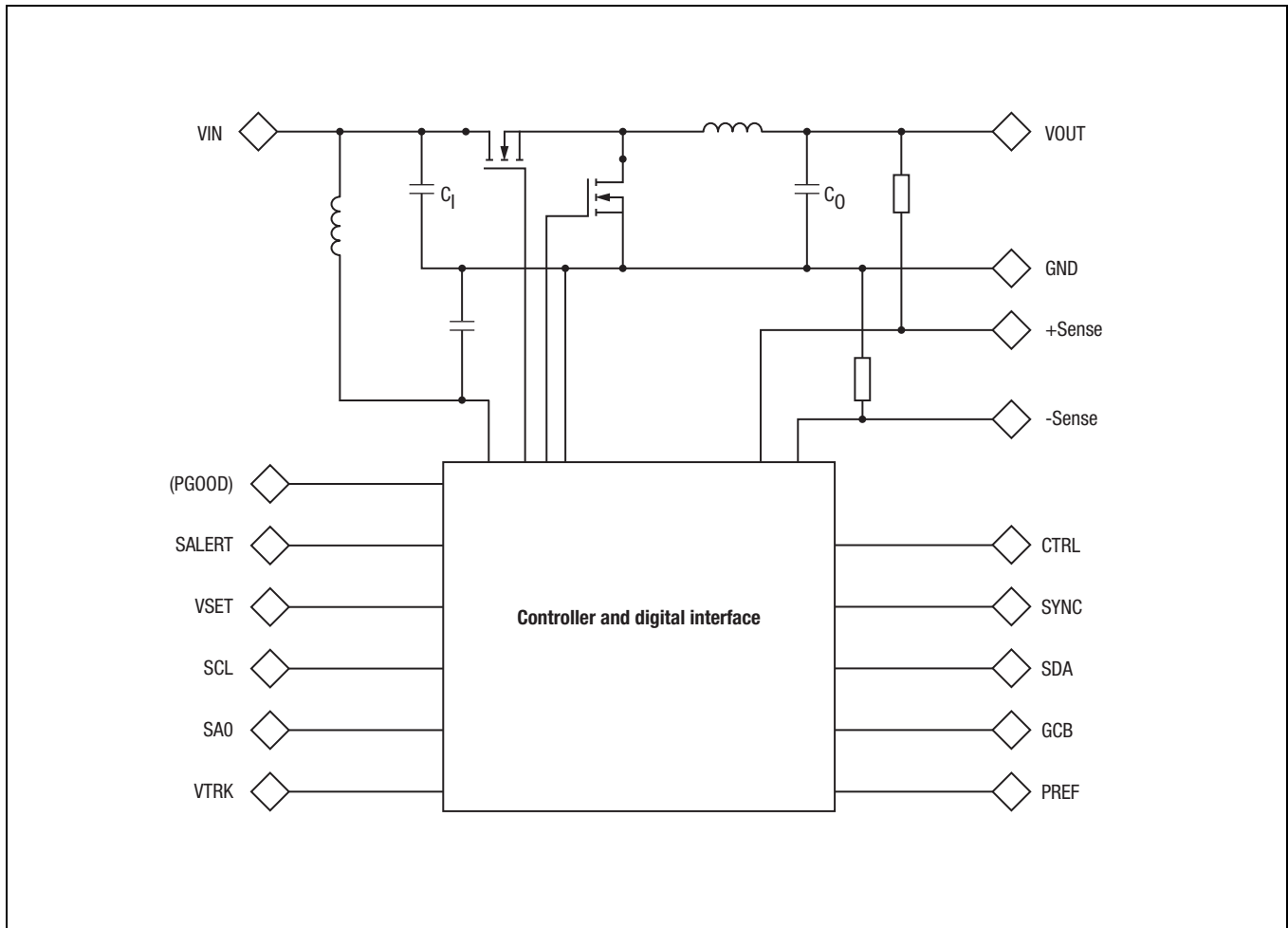
Characteristics		Min	Typ	Max	Unit
T _{P1}	Operating temperature (see Thermal Consideration section)	-40		120	°C
T _S	Storage temperature	-40		125	°C
V _I	Input voltage (See Operating Information Section for input and output voltage relations)	-0.3		16	V
Logic I/O voltage	CTRL, SA0, SA1, SALERT, SCL, SDA, VSET, SYNC, GCB, PG	-0.3		6.5	V
Ground voltage differential	-S, PREF, GND	-0.3		0.3	V
Analog pin voltage	V _O , +S, VTRK	-0.3		6.5	V

Stress in excess of Absolute Maximum Ratings may cause permanent damage. Absolute Maximum Ratings, sometimes referred to as no destruction limits, are normally tested with one parameter at a time exceeding the limits in the Electrical Specification. If exposed to stress above these limits, function and performance may degrade in an unspecified manner.

Configuration File

This product is designed with a digital control circuit. The control circuit uses a configuration file which determines the functionality and performance of the product. The Electrical Specification table shows parameter values of functionality and performance with the default configuration file, unless otherwise specified. The default configuration file is designed to fit most application need with focus on high efficiency. If different characteristics are required it is possible to change the configuration file to optimize certain performance characteristics. In this Technical specification examples are included to show the possibilities with digital control. See Operating Information section for information about trade offs when optimizing certain key performance characteristics.

Fundamental Circuit Diagram



C_i=22 μF C_o =100 μF

Electrical Specification

$T_{P1} = -30$ to $+95^{\circ}\text{C}$, $V_I = 4.5$ to 14 V , $V_I > V_O + 1.0\text{ V}$

Typical values given at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12.0\text{ V}$, max I_O , unless otherwise specified under Conditions.

Default configuration file, 190 10-CDA 102 0207/001.

External $C_{IN} = 470\text{ }\mu\text{F}/10\text{ m}\Omega$, $C_{OUT} = 470\text{ }\mu\text{F}/10\text{ m}\Omega$. See Operating Information section for selection of capacitor types.

Sense pins are connected to the output pins.

Characteristics	Conditions	Min	Typ	Max	Unit
V_I	Input voltage rise time			2.4	V/ms

V_O	Output voltage without pin strap			1.2	V	
	Output voltage adjustment range		0.60		5.0	
	Output voltage adjustment including margining		0.54		5.5	
	Output voltage set-point resolution			± 0.025	% V_O	
	Output voltage accuracy	Including line, load, temp. See Note 15	-1		1	%
	Internal resistance +S/-S to VOUT/GND			4.7		Ω
	Line regulation	$V_O = 0.6\text{ V}$		2		mV
		$V_O = 1.0\text{ V}$		2		
		$V_O = 3.3\text{ V}$		2		
		$V_O = 5.0\text{ V}$		3		
Load regulation; $I_O = 0 - 100\%$	$V_O = 0.6\text{ V}$		3		mV	
	$V_O = 1.0\text{ V}$		2			
	$V_O = 3.3\text{ V}$		2			
	$V_O = 5.0\text{ V}$		2			
V_{Oac}	Output ripple & noise $C_O = 470\text{ }\mu\text{F}$ (minimum external capacitance). See Note 12	$V_O = 0.6\text{ V}$		20	mVp-p	
		$V_O = 1.0\text{ V}$		30		
		$V_O = 3.3\text{ V}$		60		
		$V_O = 5.0\text{ V}$		100		

I_O	Output current	See Note 17	0.001		12	A
I_S	Static input current at max I_O	$V_O = 0.6\text{ V}$		0.76		A
		$V_O = 1.0\text{ V}$		1.17		
		$V_O = 3.3\text{ V}$		3.53		
		$V_O = 5.0\text{ V}$		4.1		
I_{lim}	Current limit threshold		14		20	A
I_{sc}	Short circuit current	RMS, hiccup mode, See Note 3	$V_O = 0.6\text{ V}$		8	A
			$V_O = 1.0\text{ V}$		6	
			$V_O = 3.3\text{ V}$		5	
			$V_O = 5.0\text{ V}$		4	

η	Efficiency	50% of max I_O	$V_O = 0.6\text{ V}$		82.6	%
			$V_O = 1.0\text{ V}$		88.5	
			$V_O = 3.3\text{ V}$		94.7	
			$V_O = 5.0\text{ V}$		95.7	
		max I_O	$V_O = 0.6\text{ V}$		78.5	%
			$V_O = 1.0\text{ V}$		85.4	
			$V_O = 3.3\text{ V}$		93.6	
			$V_O = 5.0\text{ V}$		94.9	
P_d	Power dissipation at max I_O	$V_O = 0.6\text{ V}$		2.05	W	
		$V_O = 1.0\text{ V}$		2.11		
		$V_O = 3.3\text{ V}$		2.66		
		$V_O = 5.0\text{ V}$		3.15		
P_{ii}	Input idling power (no load)	Default configuration: Continues Conduction Mode, CCM	$V_O = 0.6\text{ V}$		0.33	W
			$V_O = 1.0\text{ V}$		0.35	
			$V_O = 3.3\text{ V}$		0.56	
			$V_O = 5.0\text{ V}$		0.99	

Characteristics			Conditions	Min	Typ	Max	Unit
P_{CTRL}	Input standby power	Turned off with CTRL-pin	Default configuration: Monitoring enabled, Precise timing enabled		180		mW
C_i	Internal input capacitance				22		μ F
C_o	Internal output capacitance				100		μ F
C_{OUT}	Total external output capacitance		See Note 10	300		7 500	μ F
	ESR range of capacitors (per single capacitor)		See Note 10	5		30	m Ω
V_{tr1}	Load transient peak voltage deviation Load step 25-75-25% of max I_o	Default configuration $di/dt = 2 A/\mu s$ $C_o=470 \mu F$ (minimum external capacitance) see Note 13	$V_o = 0.6 V$		55		mV
			$V_o = 1.0 V$		65		
			$V_o = 3.3 V$		110		
			$V_o = 5.0 V$		190		
t_{tr1}	Load transient recovery time, Note 5 Load step 25-75-25% of max I_o	Default configuration $di/dt = 2 A/\mu s$ $C_o=470 \mu F$ (minimum external capacitance) see Note 13	$V_o = 0.6 V$		230		μs
			$V_o = 1.0 V$		210		
			$V_o = 3.3 V$		200		
			$V_o = 5.0 V$		200		
f_s	Switching frequency				320		kHz
	Switching frequency range		PMBus configurable		200-640		kHz
	Switching frequency set-point accuracy				± 5		%
	Control Circuit PWM Duty Cycle			5		95	%
	Minimum Sync Pulse Width			150			ns
	Synchronization Frequency Tolerance		External clock source	-13		13	%
Input Under Voltage Lockout, UVLO	UVLO threshold				3.85		V
	UVLO threshold range		PMBus configurable		3.85-14		V
	Set point accuracy			-150		150	mV
	UVLO hysteresis				0.35		V
	UVLO hysteresis range		PMBus configurable		0-10.15		V
	Delay					2.5	μs
Fault response			See Note 3	Automatic restart, 70 ms			
Input Over Voltage Protection, IOVP	IOVP threshold				16		V
	IOVP threshold range		PMBus configurable		4.2-16		V
	Set point accuracy			-150		150	mV
	IOVP hysteresis				1		V
	IOVP hysteresis range		PMBus configurable		0-11.8		V
	Delay					2.5	μs
Fault response			See Note 3	Automatic restart, 70 ms			
Power Good, PG, See Note 2	PG threshold				90		% V_o
	PG hysteresis				5		% V_o
	PG delay				10		ms
	PG delay range		PMBus configurable		0-500		s
Output voltage Over/Under Voltage Protection, OVP/UVP	UVP threshold				85		% V_o
	UVP threshold range		PMBus configurable		0-100		% V_o
	UVP hysteresis				5		% V_o
	OVP threshold				115		% V_o
	OVP threshold range		PMBus configurable		100-115		% V_o
	UVP/OVP response time				25		μs
	UVP/OVP response time range		PMBus configurable		5-60		μs
Fault response			See Note 3	Automatic restart, 70 ms			

Characteristics		Conditions	Min	Typ	Max	Unit
Over Current Protection, OCP	OCP threshold			18		A
	OCP threshold range	PMBus configurable		0-18		A
	Protection delay,	See Note 4		5		T_{sw}
	Protection delay range	PMBus configurable		1-32		T_{sw}
	Fault response	See Note 3	Automatic restart, 70 ms			
Over Temperature Protection, OTP at P1 See Note 9	OTP threshold			120		°C
	OTP threshold range	PMBus configurable		-40...+120		°C
	OTP hysteresis			15		°C
	OTP hysteresis range	PMBus configurable		0-160		°C
	Fault response	See Note 3	Automatic restart, 240 ms			

V_{IL}	Logic input low threshold	SYNC, SA0, SA1, SCL, SDA, GCB, CTRL, VSET			0.8	V
V_{IH}	Logic input high threshold		2			V
I_{IL}	Logic input low sink current	CTRL			0.6	mA
V_{OL}	Logic output low				0.4	V
V_{OH}	Logic output high	SYNC, SCL, SDA, SALERT, GCB, PG	2.25			V
I_{OL}	Logic output low sink current				4	mA
I_{OH}	Logic output high source current				2	mA
t_{set}	Setup time, SMBus	See Note 1	300			ns
t_{hold}	Hold time, SMBus	See Note 1	250			ns
t_{free}	Bus free time, SMBus	See Note 1	2			ms
C_p	Internal capacitance on logic pins				10	pF

Boot-up time		See Note 11		35		ms	
Output Voltage Delay Time See Note 6	Delay duration			10		ms	
	Delay duration range	PMBus configurable		2-500000			
	Delay accuracy turn-on	Default configuration: CTRL controlled Precise timing enabled			±0.25		ms
			PMBus controlled Precise timing disabled			-0.25/+4	
Delay accuracy turn-off				-0.25/+4		ms	
Output Voltage Ramp Time See Note 14	Ramp duration			10		ms	
	Ramp duration range	PMBus configurable		0-200			
	Ramp time accuracy				100		µs

VTRK Input Bias Current	$V_{VTRK} = 5.5$ V			110	200	µA
VTRK Tracking Ramp Accuracy ($V_O - V_{VTRK}$)	100% Tracking, see Note 8		-100		100	mV
VTRK Regulation Accuracy ($V_O - V_{VTRK}$)	100% Tracking		-1		1	%

Monitoring accuracy	READ_VIN vs V_I			3		%	
	READ_VOUT vs V_O			1		%	
	READ_IOUT vs I_O	$I_O = 0-12$ A, $T_{P1} = 0$ to $+95^\circ$ C $V_I = 12$ V			±1.6		A
	READ_IOUT vs I_O	$I_O = 0-12$ A, $T_{P1} = 0$ to $+95^\circ$ C $V_I = 4.5-14$ V			±2.7		A

Note 1: See section I2C/SMBus Setup and Hold Times – Definitions.

Note 2: Monitorable over PMBus Interface.

Note 3: Automatic restart ~70 or 240 ms after fault if the fault is no longer present. Continuous restart attempts if the fault reappear after restart. See Operating Information for other fault response options.

Note 4: T_{sw} is the switching period.

Note 5: Within +/-3% of V_O

Note 6: See section Soft-start Power Up.

Note 8: Tracking functionality is designed to follow a VTRK signal with slewrate < 2.4V/ms. For faster VTRK signals accuracy will depend on the regulator bandwidth.

Note 9: See section Over Temperature Protection (OTP).

Note 10: See section External Capacitors.

Note 11: See section Start-Up Procedure.

Note 12: See graph Output Ripple vs External Capacitance and Operating information section Output Ripple and Noise.

Note 13: See graph Load Transient vs. External Capacitance and Operating information section External Capacitors.

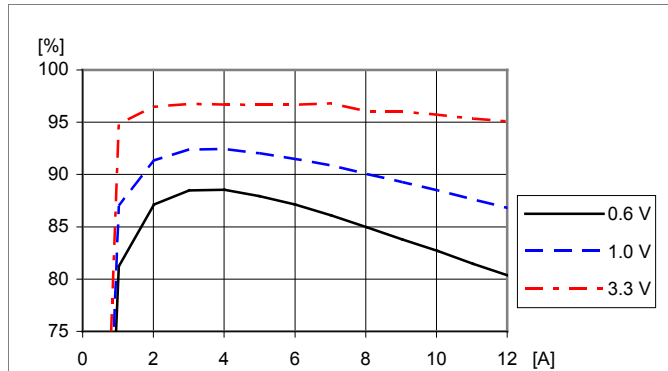
Note 14: Time for reaching 100% of nominal V_{out} .

Note 15: For $V_{out} < 1.0$ V accuracy is +/-10 mV. For further deviations see section Output Voltage Adjust using PMBus.

Note 17: Without minimum load the monitoring function will cause an output voltage of ~0.6 V when the output is disabled. This does not apply if Low Power mode is used.

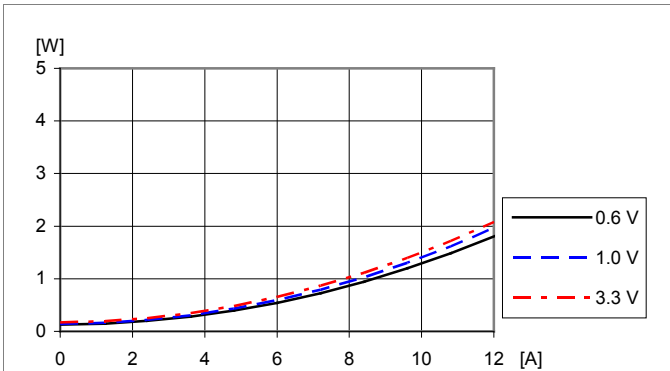
Typical Characteristics
Efficiency and Power Dissipation

Efficiency vs. Output Current, $V_I=5\text{ V}$



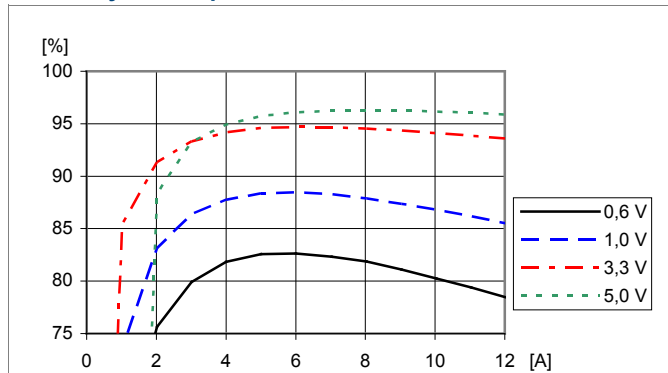
Efficiency vs. load current and output voltage:
 $T_{P1} = +25^\circ\text{C}$, $V_I=5\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Power Dissipation vs. Output Current, $V_I=5\text{ V}$



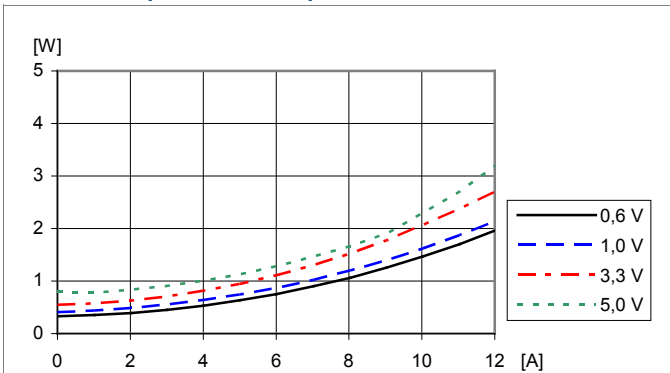
Dissipated power vs. load current and output voltage:
 $T_{P1} = +25^\circ\text{C}$, $V_I=5\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Efficiency vs. Output Current, $V_I=12\text{ V}$



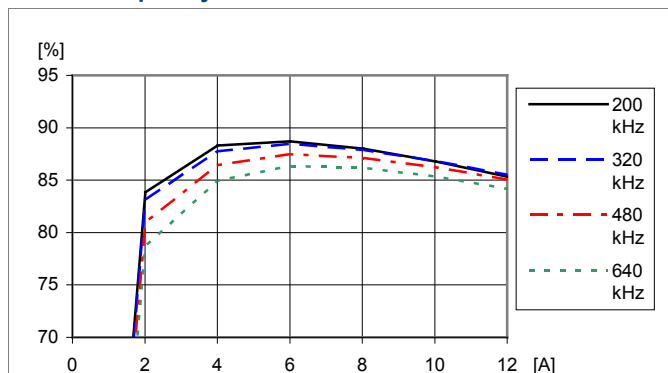
Efficiency vs. load current and output voltage at
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Power Dissipation vs. Output Current, $V_I=12\text{ V}$



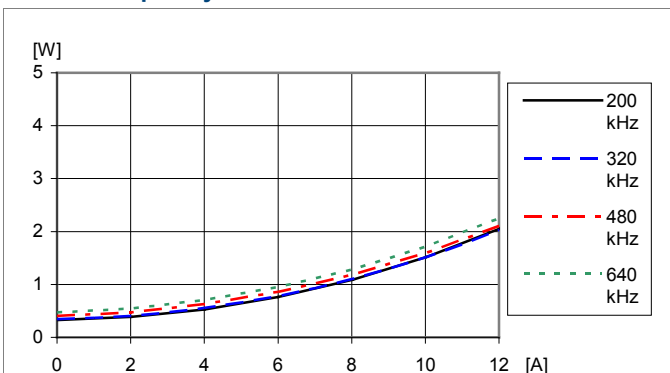
Dissipated power vs. load current and output voltage:
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Efficiency vs. Output Current and Switch Frequency



Efficiency vs. load current and switch frequency at
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $V_O=1.0\text{ V}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$
Default configuration except changed frequency.

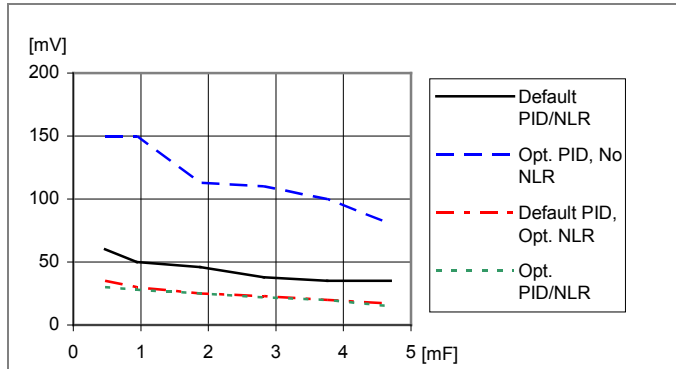
Power Dissipation vs. Output Current and Switch Frequency



Dissipated power vs. load current and switch frequency at
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $V_O=1.0\text{ V}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$
Default configuration except changed frequency.

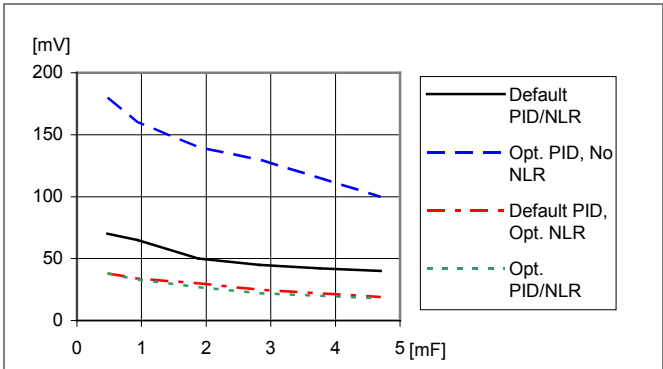
Typical Characteristics
Load Transient

Load Transient vs. External Capacitance, $V_O=1.0\text{ V}$



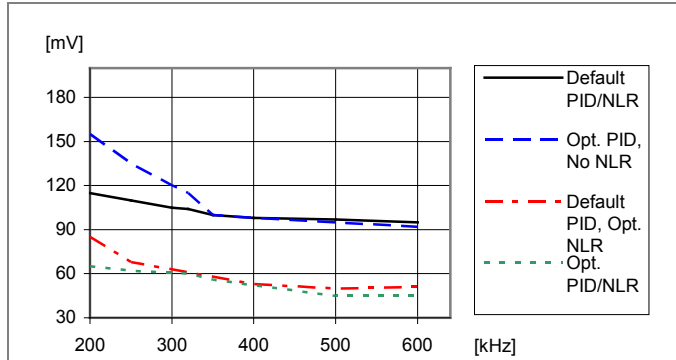
Load transient peak voltage deviation vs. external capacitance.
Step-change (3-9-3 A). Parallel coupling of capacitors with 470 $\mu\text{F}/10\text{ m}\Omega$,
 $T_{P1} = +25^\circ\text{C}$. $V_I=12\text{ V}$, $V_O=1.0\text{ V}$, $f_{sw}=320\text{ kHz}$, $di/dt=2\text{ A}/\mu\text{s}$

Load Transient vs. External Capacitance, $V_O=3.3\text{ V}$



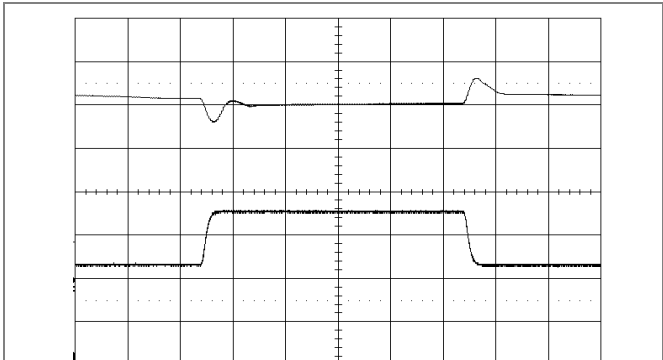
Load transient peak voltage deviation vs. external capacitance.
Step-change (3-9-3 A). Parallel coupling of capacitors with 470 $\mu\text{F}/10\text{ m}\Omega$,
 $T_{P1} = +25^\circ\text{C}$. $V_I=12\text{ V}$, $V_O=3.3\text{ V}$, $f_{sw}=320\text{ kHz}$, $di/dt=2\text{ A}/\mu\text{s}$

Load transient vs. Switch Frequency



Load transient peak voltage deviation vs. frequency.
Step-change (3-9-3 A).
 $T_{P1} = +25^\circ\text{C}$. $V_I=12\text{ V}$, $V_O=3.3\text{ V}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$

Output Load Transient Response, Default PID/NLR

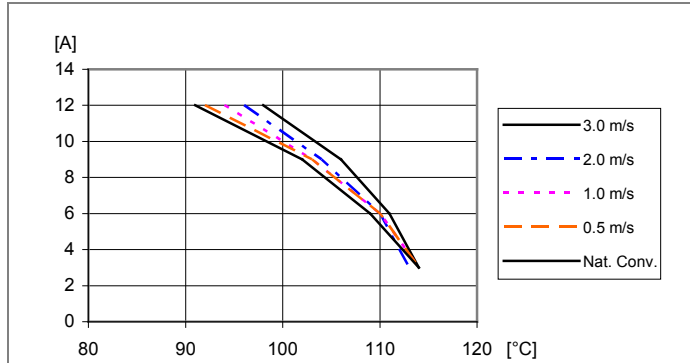


Output voltage response to load current step-change (3-9-3 A) at:
 $T_{P1} = +25^\circ\text{C}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$
 $di/dt=2\text{ A}/\mu\text{s}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$

Top trace: output voltage (200 mV/div.).
Bottom trace: load current (5 A/div.).
Time scale: (0.1 ms/div.).

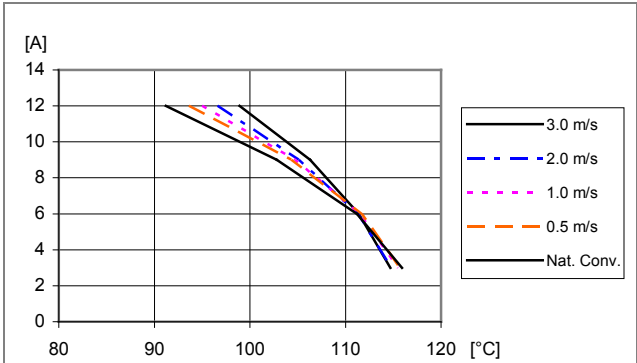
Typical Characteristics
Output Current Characteristic

Output Current Derating, $V_O=0.6\text{ V}$



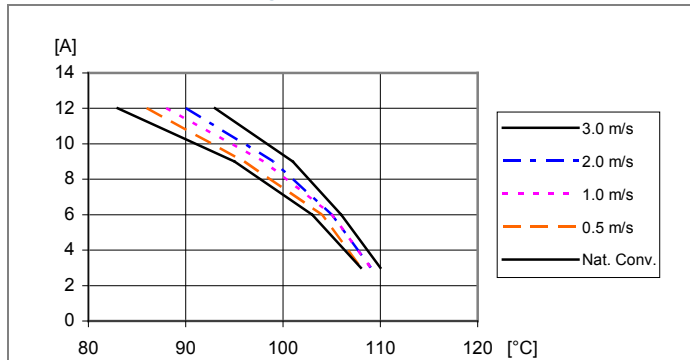
Available load current vs. ambient air temperature and airflow at $V_O=0.6\text{ V}$, $V_I=12\text{ V}$. See Thermal Consideration section.

Output Current Derating, $V_O=1.0\text{ V}$



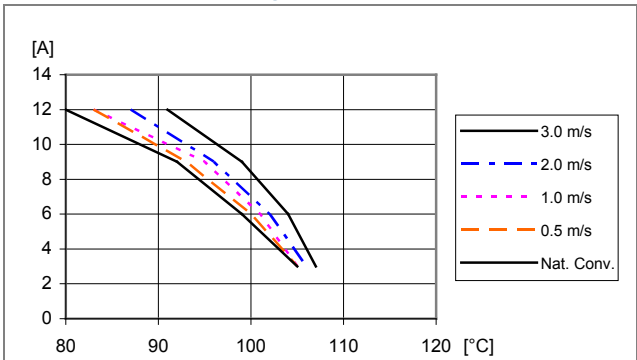
Available load current vs. ambient air temperature and airflow at $V_O=1.0\text{ V}$, $V_I=12\text{ V}$. See Thermal Consideration section.

Output Current Derating, $V_O=3.3\text{ V}$



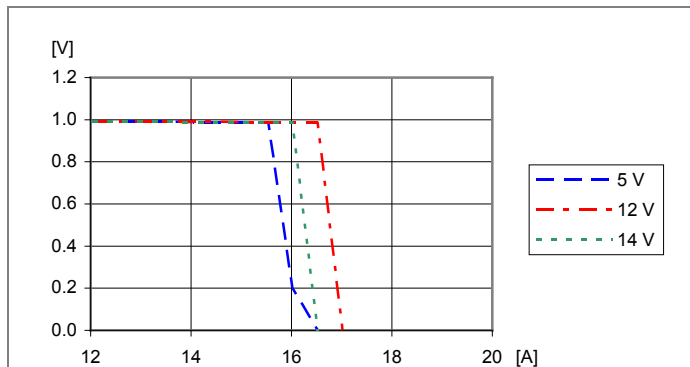
Available load current vs. ambient air temperature and airflow at $V_O=3.3\text{ V}$, $V_I=12\text{ V}$. See Thermal Consideration section.

Output Current Derating, $V_O=5.0\text{ V}$



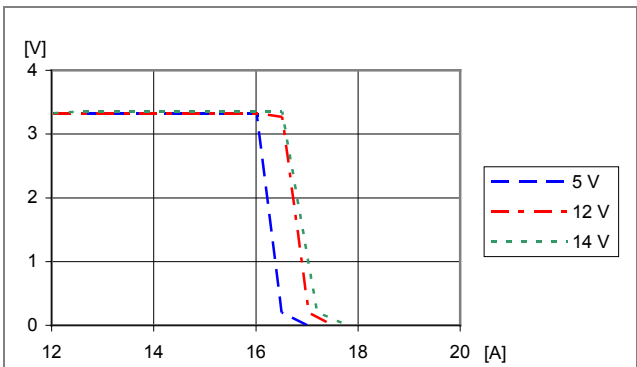
Available load current vs. ambient air temperature and airflow at $V_O=5.0\text{ V}$, $V_I=12\text{ V}$. See Thermal Consideration section.

Current Limit Characteristics, $V_O=1.0\text{ V}$



Output voltage vs. load current at $T_{P1} = +25^\circ\text{C}$. $V_O=1.0\text{ V}$.

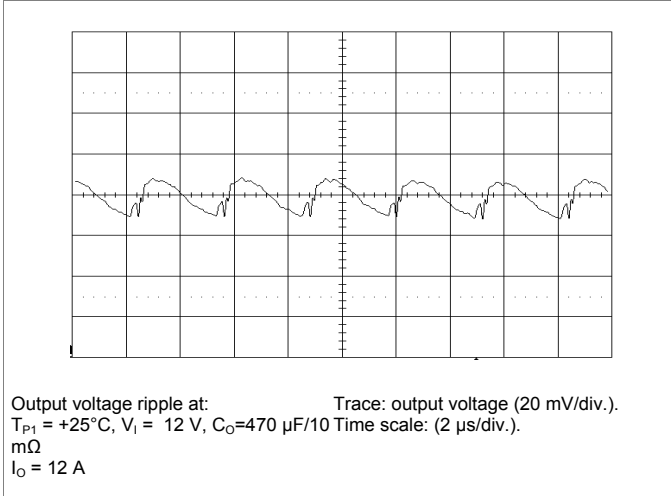
Current Limit Characteristics, $V_O=3.3\text{ V}$



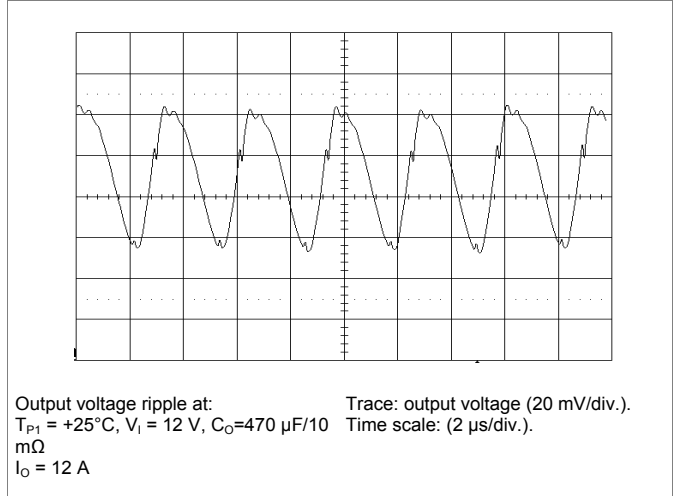
Output voltage vs. load current at $T_{P1} = +25^\circ\text{C}$. $V_O=3.3\text{ V}$.

Typical Characteristics
Output Voltage

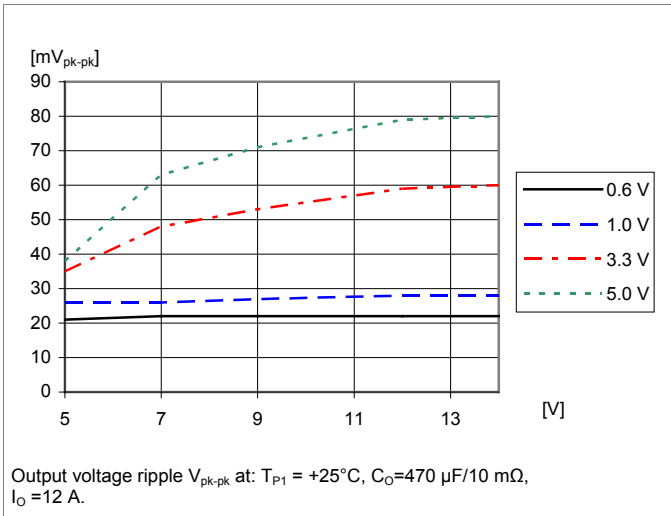
Output Ripple & Noise, $V_O=1.0\text{ V}$



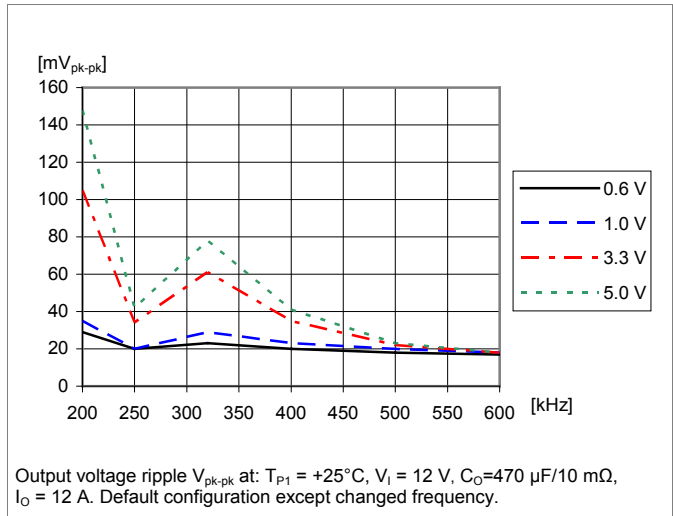
Output Ripple & Noise, $V_O=3.3\text{ V}$



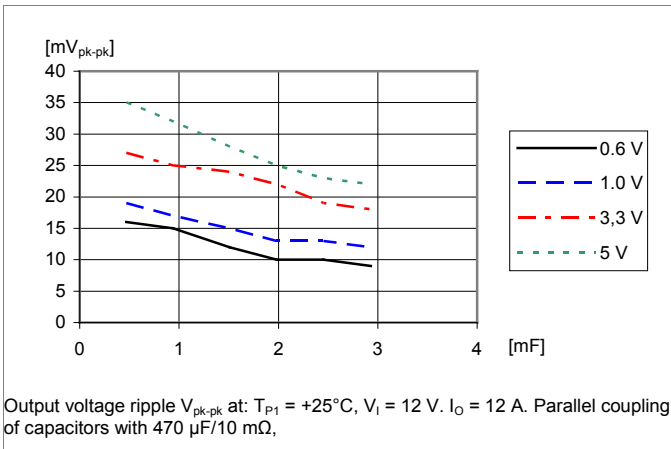
Output Ripple vs. Input Voltage



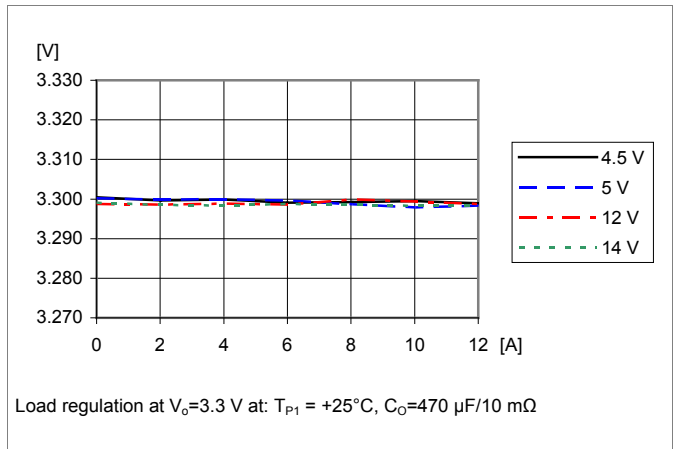
Output Ripple vs. Frequency



Output Ripple vs. External Capacitance

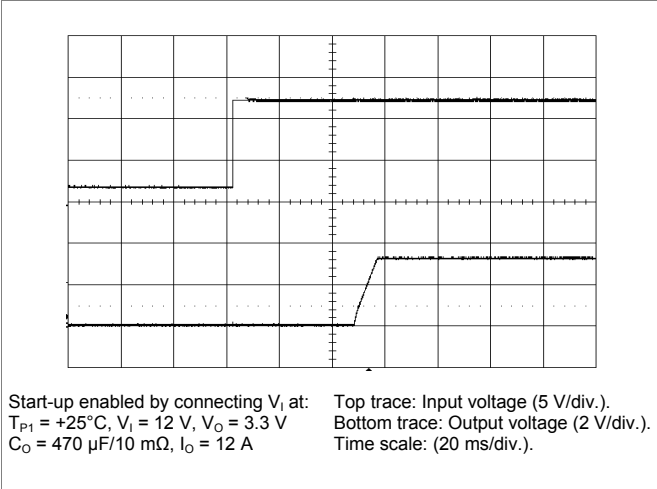


Load regulation, $V_O=3.3\text{ V}$

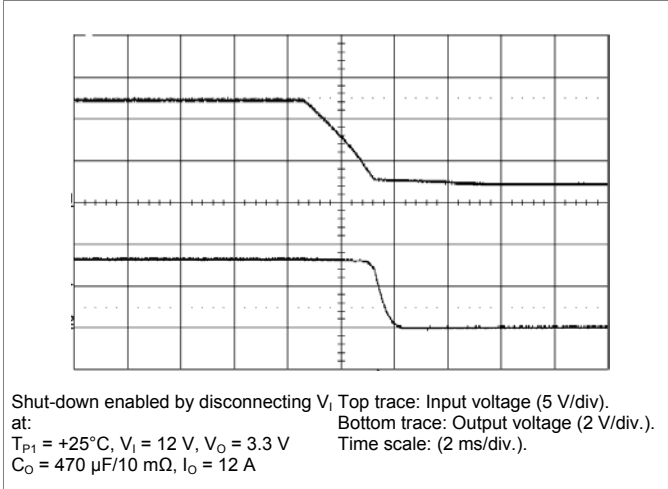


Typical Characteristics
Start-up and shut-down

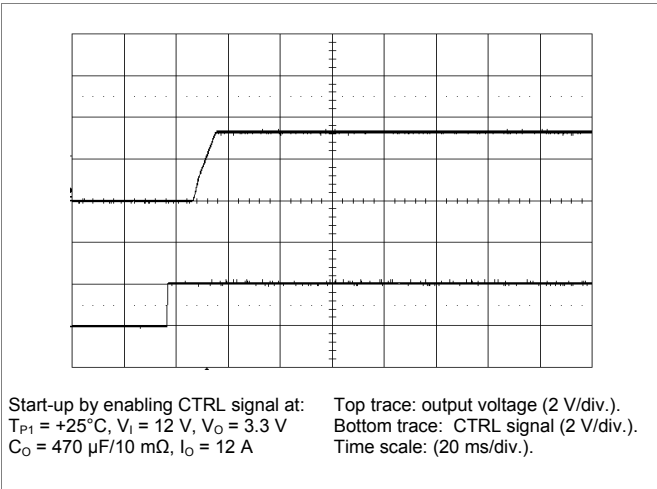
Start-up by input source



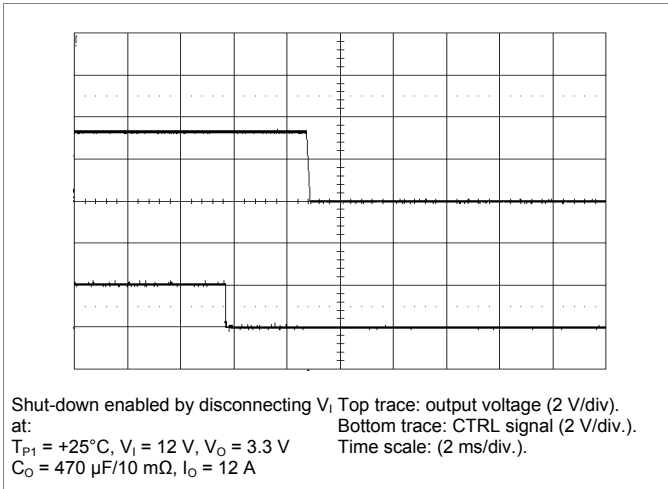
Shut-down by input source



Start-up by CTRL signal



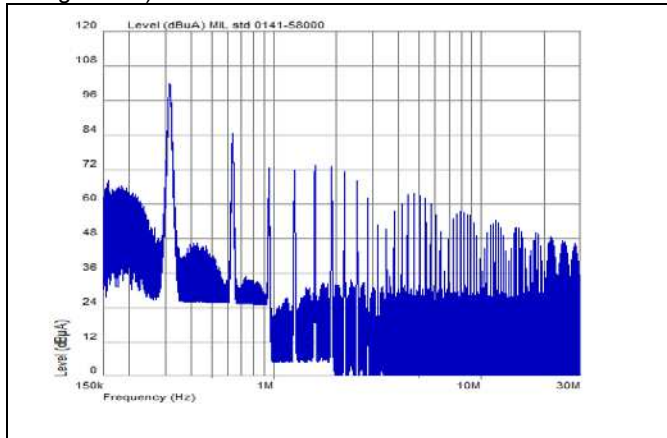
Shut-down by CTRL signal



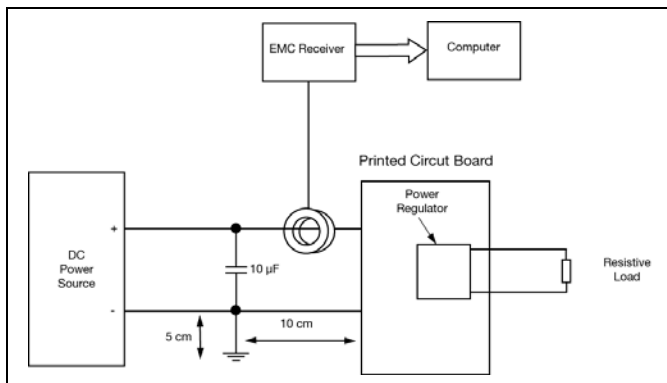
EMC Specification

Conducted EMI measured according to test set-up and standard MIL std 0141 - 58000. The fundamental switching frequency is 320 kHz at $V_i = 12.0$ V, max I_o .

Conducted EMI Input terminal value (typical for default configuration)



EMI without filter



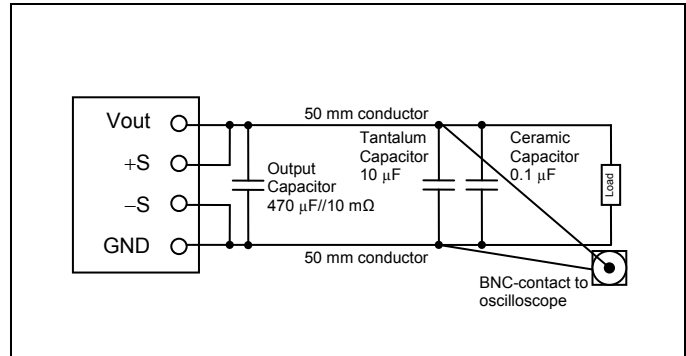
Test set-up

Layout Recommendations

The radiated EMI performance of the product will depend on the PWB layout and ground layer design. It is also important to consider the stand-off of the product. If a ground layer is used, it should be connected to the output of the product and the equipment ground or chassis. A ground layer will increase the stray capacitance in the PWB and improve the high frequency EMC performance.

Output Ripple and Noise

Output ripple and noise is measured according to figure below. A 50 mm conductor works as a small inductor forming together with the two capacitances a damped filter.



Output ripple and noise test set-up.

Operating information

Power Management Overview

This product is equipped with a PMBus interface. The product incorporates a wide range of readable and configurable power management features that are simple to implement with a minimum of external components. Additionally, the product includes protection features that continuously safeguard the load from damage due to unexpected system faults. A fault is also shown as an alert on the SALERT pin. The following product parameters can continuously be monitored by a host: Input voltage, output voltage/current, and internal temperature. If the monitoring is not needed it can be disabled and the product enters a low power mode reducing the power consumption. The protection features are not affected.

The product is delivered with a default configuration suitable for a wide range operation in terms of input voltage, output voltage, and load. The configuration is stored in an internal Non-Volatile Memory (NVM). All power management functions can be reconfigured using the PMBus interface. Please contact your local Murata Power Solutions representative for design support of custom configurations or appropriate SW tools for design and down-load of your own configurations.

Input Voltage

The input voltage range, 4.5 - 14 V, makes the product easy to use in intermediate bus applications when powered by a non-regulated bus converter or a regulated bus converter. See Ordering Information for input voltage range.

Input Under Voltage Lockout, UVLO

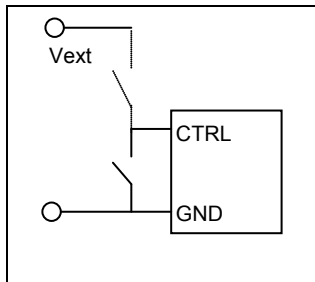
The product monitors the input voltage and will turn-on and turn-off at configured levels. The default turn-on input voltage level setting is 4.20 V, whereas the corresponding turn-off input voltage level is 3.85 V. Hence, the default hysteresis between turn-on and turn-off input voltage is 0.35 V. Once an input turn-

off condition occurs, the device can respond in a number of ways as follows:

1. Continue operating without interruption. The unit will continue to operate as long as the input voltage can be supported. If the input voltage continues to fall, there will come a point where the unit will cease to operate.
2. Continue operating for a given delay period, followed by shutdown if the fault still exists. The device will remain in shutdown until instructed to restart.
3. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.

The default response from a turn-off is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition. If the fault condition is no longer present, the product will be re-enabled. The turn-on and turn-off levels and response can be reconfigured using the PMBus interface.

Remote Control



The product is equipped with a remote control function, i.e., the CTRL pin. The remote control can be connected to either the primary negative input connection (GND) or an external voltage (Vext), which is a 3 - 5 V positive supply voltage in accordance to the SMBus Specification version 2.0.

The CTRL function allows the product to be turned on/off by an external device like a semiconductor or mechanical switch. By default the product will turn on when the CTRL pin is left open and turn off when the CTRL pin is applied to GND. The CTRL pin has an internal pull-up resistor. When the CTRL pin is left open, the voltage generated on the CTRL pin is max 5.5 V. If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to asserting the CTRL pin.

The product can also be configured using the PMBus interface to be “Always on”, or turn on/off can be performed with PMBus commands.

Input and Output Impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. The performance in some applications can be enhanced by addition of external capacitance as described under External Decoupling Capacitors. If the input voltage source contains significant inductance, the addition a capacitor with low ESR at the input of the product will ensure stable operation.

External Capacitors

Input capacitors:

The input ripple RMS current in a buck converter is equal to

$$\text{Eq. 1. } I_{inputRMS} = I_{load} \sqrt{D(1-D)},$$

where I_{load} is the output load current and D is the duty cycle.

The maximum load ripple current becomes $I_{load} / 2$. The ripple current is divided into three parts, i.e., currents in the input source, external input capacitor, and internal input capacitor. How the current is divided depends on the impedance of the input source, ESR and capacitance values in the capacitors. A minimum capacitance of 300 μF with low ESR is recommended. The ripple current rating of the capacitors must follow Eq. 1. For high-performance/transient applications or wherever the input source performance is degraded, additional low ESR ceramic type capacitors at the input is recommended. The additional input low ESR capacitance above the minimum level insures an optimized performance.

Output capacitors:

When powering loads with significant dynamic current requirements, the voltage regulation at the point of load can be improved by addition of decoupling capacitors at the load. The most effective technique is to locate low ESR ceramic and electrolytic capacitors as close to the load as possible, using several capacitors in parallel to lower the effective ESR. The ceramic capacitors will handle high-frequency dynamic load changes while the electrolytic capacitors are used to handle low frequency dynamic load changes. Ceramic capacitors will also reduce high frequency noise at the load. It is equally important to use low resistance and low inductance PWB layouts and cabling.

External decoupling capacitors are a part of the control loop of the product and may affect the stability margins. Stable operation is guaranteed for the following total capacitance C_O in the output decoupling capacitor bank where

$$\text{Eq. 2. } C_O = [C_{min}, C_{max}] = [300, 7500] \mu\text{F}.$$

The decoupling capacitor bank should consist of capacitors which have a capacitance value larger than $C \geq C_{min}$ and has an ESR range of

$$\text{Eq. 3. } ESR = [ESR_{min}, ESR_{max}] = [5, 30] \text{ m}\Omega$$

The control loop stability margins are limited by the minimum time constant τ_{min} of the capacitors. Hence, the time constant of the capacitors should follow Eq. 4.

$$\text{Eq. 4. } \tau \geq \tau_{min} = C_{min} ESR_{min} = 1.5 \mu\text{s}$$

This relation can be used if your preferred capacitors have parameters outside the above stated ranges in Eq. 2 and Eq.3.

- If the capacitors capacitance value is $C < C_{min}$ one must use at least N capacitors where
$$N \geq \left\lceil \frac{C_{min}}{C} \right\rceil \text{ and } ESR \geq ESR_{min} \frac{C_{min}}{C}.$$
- If the ESR value is $ESR > ESR_{max}$ one must use at least N capacitors of that type where

$$N \geq \left\lceil \frac{ESR}{ESR_{max}} \right\rceil \text{ and } C \geq \frac{C_{min}}{N}$$

- If the *ESR* value is $ESR < ESR_{min}$ the capacitance value should be

$$C \geq C_{min} \frac{ESR_{min}}{ESR}$$

For a total capacitance outside the above stated range or capacitors that do not follow the stated above requirements above a re-design of the control loop parameters will be necessary for robust dynamic operation and stability.

Control Loop Compensation

The product is configured with a robust control loop compensation which allows for a wide range operation of input and output voltages and capacitive loads as defined in the section External Decoupling Capacitors. For an application with a specific input voltage, output voltage, and capacitive load, the control loop can be optimized for a robust and stable operation and with an improved load transient response. This optimization will minimize the amount of required output decoupling capacitors for a given load transient requirement yielding an optimized cost and minimized board space. The control loop parameters can be reconfigured using the PMBus interface.

Load Transient Response Optimization

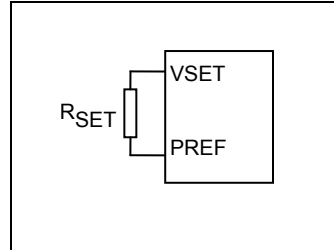
The product incorporates a Non-Linear transient Response, NLR, loop that decreases the response time and the output voltage deviation during a load transient. The NLR results in a higher equivalent loop bandwidth than is possible using a traditional linear control loop. The product is pre-configured with appropriate NLR settings for robust and stable operation for a wide range of input voltage and a capacitive load range as defined in the section External Decoupling Capacitors. For an application with a specific input voltage, output voltage, and capacitive load, the NLR configuration can be optimized for a robust and stable operation and with an improved load transient response. This will also reduce the amount of output decoupling capacitors and yield a reduced cost. However, the NLR slightly reduces the efficiency. In order to obtain maximal energy efficiency the load transient requirement has to be met by the standard control loop compensation and the decoupling capacitors. The NLR settings can be reconfigured using the PMBus interface.

Remote Sense

The product has remote sense that can be used to compensate for voltage drops between the output and the point of load. The sense traces should be located close to the PWB ground layer to reduce noise susceptibility. Due to derating of internal output capacitance the voltage drop should be kept below $V_{DROPMAX} = (5.5 - V_{OUT}) / 2$. A large voltage drop will impact the electrical performance of the regulator. If

the remote sense is not needed +S should be connected to VOUT and -S should be connected to GND.

Output Voltage Adjust using Pin-strap Resistor



Using an external Pin-strap resistor, R_{SET} , the output voltage can be set in the range 0.6 V to 3.3 V at 28 different levels shown in the table below. The resistor should be applied between the VSET pin and the PREF pin.

R_{SET} also sets the maximum output voltage, see section “Output Voltage Range Limitation”. The resistor is sensed only during product start-up. Changing the resistor value during normal operation will not change the output voltage. The input voltage must be at least 1 V larger than the output voltage in order to deliver the correct output voltage. See Ordering Information for output voltage range.

The following table shows recommended resistor values for R_{SET} . Maximum 1% tolerance resistors are required.

V_{OUT} [V]	R_{SET} [kΩ]	V_{OUT} [V]	R_{SET} [kΩ]
0.60	10	1.50	46.4
0.65	11	1.60	51.1
0.70	12.1	1.70	56.2
0.75	13.3	1.80	61.9
0.80	14.7	1.90	68.1
0.85	16.2	2.00	75
0.90	17.8	2.10	82.5
0.95	19.6	2.20	90.9
1.00	21.5	2.30	100
1.05	23.7	2.50	110
1.10	26.1	3.00	121
1.15	28.7	3.30	133
1.20	31.6	4.00	147
1.25	34.8	5.00	162
1.30	38.3	5.50	178
1.40	42.2		

The output voltage and the maximum output voltage can be pin strapped to three fixed values by connecting the VSET pin according to the table below.

V_{OUT} [V]	VSET
0.60	Shorted to PREF
1.2	Open “high impedance”
2.5	Logic High, GND as reference

Output Voltage Adjust using PMBus

The output voltage set by pin-strap can be overridden by configuration file or by using a PMBus command. See Electrical Specification for adjustment range.

When setting the output voltage by configuration file or by a PMBus command, the specified output voltage accuracy is valid only when the set output voltage level falls within the same bin range as the voltage level defined by the pin-strap resistor R_{SET} . The applicable bin ranges are defined in the table below. Valid accuracy for voltage levels outside the applicable bin range is two times the specified.

Example:

Nominal V_{out} is set to 1.10V by $R_{set}=26.1\text{kohm}$. 1.10V falls within the bin range 0.988-1.383V, thus specified accuracy is valid when adjusting V_{out} within 0.988-1.383V.

V_{OUT} bin ranges [V]
0 – 0.988
0.988 – 1.383
1.383 – 1.975
1.975 – 2.398
2.398 – 2.963
2.963 – 3.753
3.753 – 4.938
4.938 –

Output Voltage Range Limitation

The output voltage range that is possible to set by configuration or by the PMBus interface is limited by the pin-strap resistor R_{SET} . The maximum output voltage is set to 110% of the nominal output value defined by R_{SET} .

$V_{OUT_MAX} = 1.1 \times V_{OUT_RSET}$. This protects the load from an over voltage due to an accidental wrong PMBus command.

Over Voltage Protection (OVP)

The product includes over voltage limiting circuitry for protection of the load. The default OVP limit is 15% above the nominal output voltage. If the output voltage exceeds the OVP limit, the product can respond in different ways:

1. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.
2. Turn off the high-side MOSFET and turn on the low-side MOSFET. The low-side MOSFET remains ON until the device attempts a restart, i.e. the output voltage is pulled to ground level (crowbar function).

The default response from an overvoltage fault is to immediately shut down as in 2. The device will continuously check for the presence of the fault condition, and when the fault condition no longer exists the device will be re-enabled. For continuous OVP when operating from an external clock for

synchronization, the only allowed response is an immediate shutdown. The OVP limit and fault response can be reconfigured using the PMBus interface.

Under Voltage Protection (UVP)

The product includes output under voltage limiting circuitry for protection of the load. The default UVP limit is 15% below the nominal output voltage. The UVP limit can be reconfigured using the PMBus interface.

Power Good

The product provides a Power Good (PG) flag in the Status Word register that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. If specified in section Connections, the product also provides a PG signal output. The PG pin is active high and by default open-drain but may also be configured as push-pull via the PMBus interface.

By default, the PG signal will be asserted when the output reaches above 90% of the nominal voltage, and de-asserted when the output falls below 85% of the nominal voltage. These limits may be changed via the PMBus interface. A PG delay period is defined as the time from when all conditions within the product for asserting PG are met to when the PG signal is actually asserted. The default PG delay is set to 10 ms. This value can be reconfigured using the PMBus interface

Switching Frequency

The fundamental switching frequency is 320 kHz, which yields optimal power efficiency. The switching frequency can be set to any value between 200 kHz and 640 kHz using the PMBus interface. The switching frequency will change the efficiency/power dissipation, load transient response and output ripple. For optimal control loop performance the control loop must be re-designed when changing the switching frequency.

Synchronization

Synchronization is a feature that allows multiple products to be synchronized to a common frequency. Synchronized products powered from the same bus eliminate beat frequencies reflected back to the input supply, and also reduces EMI filtering requirements. Eliminating the slow beat frequencies (usually <10 kHz) allows the EMI filter to be designed to attenuate only the synchronization frequency. Synchronization can also be utilized for phase spreading, described in section Phase Spreading.

The products can be synchronized with an external oscillator or one product can be configured with the SYNC pin as a SYNC Output working as a master driving the synchronization. All others on the same synchronization bus should be configured with SYNC Input or SYNC Auto Detect (Default configuration) for correct operation. When the SYNC pin is configured in auto detect mode the product will automatically check for a clock signal on the SYNC pin.

Phase Spreading

When multiple products share a common DC input supply, spreading of the switching clock phase between the products can be utilized. This dramatically reduces input capacitance requirements and efficiency losses, since the peak current drawn from the input supply is effectively spread out over the whole switch period. This requires that the products are synchronized. Up to 16 different phases can be used. The phase spreading of the product can be configured using the PMBus interface.

Adaptive Diode Emulation

Most power converters use synchronous rectification to optimize efficiency over a wide range of input and output conditions. However, at light loads the synchronous MOSFET will typically sink current and introduce additional energy losses associated with higher peak inductor currents, resulting in reduced efficiency. Adaptive diode emulation mode turns off the low-side FET gate drive at low load currents to prevent the inductor current from going negative, reducing the energy losses and increasing overall efficiency. Diode emulation is not available for current sharing groups. Note: the overall bandwidth of the product may be reduced when in diode emulation mode. It is recommended that diode emulation is disabled prior to applying significant load steps. The diode emulation mode can be configured using the PMBus interface.

Adaptive Frequency and Pulse Skip Control

Since switching losses contribute to the efficiency of the power converter, reducing the switching frequency will reduce the switching losses and increase efficiency. The product includes an Adaptive Frequency Control mode, which effectively reduces the observed switching frequency as the load decreases. Adaptive frequency mode is only available while the device is operating within Adaptive Diode Emulation Mode. As the load current is decreased, diode emulation mode decreases the Synch-FET on-time to prevent negative inductor current from flowing. As the load is decreased further, the Switch-FET pulse width will begin to decrease while maintaining the programmed frequency, f_{PROG} (set by the `FREQ_SWITCH` command). Once the Switch-FET pulse width (D) reaches 50% of the nominal duty cycle, D_{NOM} (determined by V_I and V_O), the switching frequency will start to decrease according to the following equation:

$$\text{Eq. 5. } f_{sw} = D \left(\frac{2(f_{PROG} - f_{MIN})}{D_{NOM}} \right) + f_{MIN}$$

Disabling a minimum Synch-FET makes the product also pulse skip which reduces the power loss further. It should be noted that adaptive frequency mode is not available for current sharing groups and is not allowed when the device is placed in auto-detect mode and a clock source is present on the SYNC pin, or if the device is outputting a clock signal on its SYNC pin. The adaptive frequency and pulse skip modes can be configured using the PMBus interface.

Efficiency Optimized Dead Time Control

The product utilizes a closed loop algorithm to optimize the dead-time applied between the gate drive signals for the switch and synch FETs. The algorithm constantly adjusts the deadtime non-overlap to minimize the duty cycle, thus maximizing efficiency. This algorithm will null out deadtime differences due to component variation, temperature and loading effects. The algorithm can be configured via the PMBus interface.

Over Current Protection (OCP)

The product includes current limiting circuitry for protection at continuous overload. The following OCP response options are available:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the product).
5. Initiate an immediate shutdown.

The default response from an over current fault is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition, and if the fault condition no longer exists the device will be re-enabled. The load distribution should be designed for the maximum output short circuit current specified. The OCP limit and response of the product can be reconfigured using the PMBus interface.

Start-up Procedure

The product follows a specific internal start-up procedure after power is applied to the VIN pin:

1. Status of the address and output voltage pin-strap pins are checked and values associated with the pin settings are loaded.
2. Values stored in the Murata default non-volatile memory are loaded. This overwrites any previously loaded values.
3. Values stored in the user non-volatile memory are loaded. This overwrites any previously loaded values.

Once this process is completed and the start-up time has passed (see Electrical Specification), the product is ready to be enabled using the CTRL pin. The product is also ready to accept commands via the PMBus interface, which will overwrite any values loaded during the start-up procedure.

Soft-start Power Up

The soft-start control introduces a time-delay before allowing the output voltage to rise. Once the boot-up time has passed and the output has been enabled, the device requires approximately 2 ms before its output voltage may be allowed to start its ramp-up process. If a soft-start delay period less than 2 ms has been configured the device will default to a 2 ms delay period. If a delay period greater than 2 ms is configured, the device will wait for the configured delay period prior to starting to ramp its output. After the delay period has expired, the output will begin to ramp towards its target voltage according to the configured soft-start ramp time.

The default settings for the soft-start delay period and the soft-start ramp time is 10 ms. Hence, power-up is completed within 20 ms in default configuration using remote control. Precise timing reduces the delay time variations and is by default activated. The soft-start power up of the product can be reconfigured using the PMBus interface.

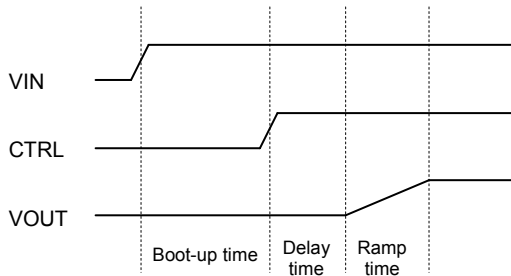


Illustration of Power Up Procedure.

Output Voltage Sequencing

A group of products may be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs, and ASICs that require one supply to reach its operating voltage prior to another. Multi-product sequencing can be achieved by configuring the start delay and rise time of each device through the PMBus interface and by using the CTRL start signal.

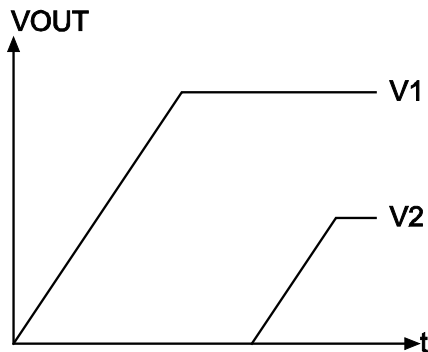


Illustration of Output Voltage Sequencing.

Voltage Tracking

The product integrates a lossless tracking scheme that allows its output to track a voltage that is applied to the VTRK pin with no external components required. During ramp-up, the output voltage follows the VTRK voltage until the preset output voltage level is met. The product offers two modes of tracking as follows:

1. Coincident. This mode configures the product to ramp its output voltage at the same rate as the voltage applied to the VTRK pin.

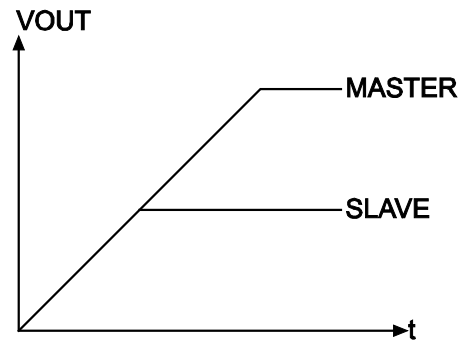


Illustration of Coincident Voltage Tracking.

2. Ratiometric. This mode configures the product to ramp its output voltage at a rate that is a percentage of the voltage applied to the VTRK pin. The default setting is 50%, but a different tracking ratio may be set by an external resistive voltage divider or through the PMBus interface.

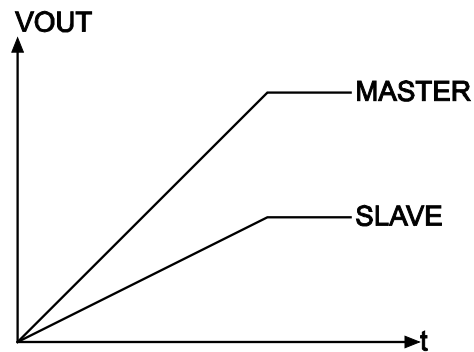


Illustration of Ratiometric Voltage Tracking

The master device in a tracking group is defined as the device that has the highest target output voltage within the group. This master device will control the ramp rate of all tracking devices and is not configured for tracking mode. All of the CTRL pins in the tracking group must be connected and driven by a single logic source. It should be noted that current sharing groups that are also configured to track another voltage do not offer pre-bias protection; a minimum load should therefore be enforced to avoid the output voltage from being held up by an outside force.

Voltage Margining Up/Down

The product can adjust its output higher or lower than its nominal voltage setting in order to determine whether the load device is capable of operating over its specified supply voltage range. This provides a convenient method for dynamically testing the operation of the load circuit over its supply margin or range. It can also be used to verify the function of supply voltage supervisors. Margin limits of the nominal output voltage $\pm 5\%$ are default, but the margin limits can be reconfigured using the PMBus interface.

Pre-Bias Startup Capability

Pre-bias startup often occurs in complex digital systems when current from another power source is fed back through a dual-supply logic component, such as FPGAs or ASICs. The product incorporates synchronous rectifiers, but will not sink current during startup, or turn off, or whenever a fault shuts down the product in a pre-bias condition. Pre-bias protection is not offered for current sharing groups that also have voltage tracking enabled.

Group Communication Bus

The Group Communication Bus, GCB, is used to communicate between products. This dedicated bus provides the communication channel between devices for features such as sequencing, fault spreading and current sharing. The GCB bus solves the PMBus data rate limitation. The GCB pin of all products in an application should be connected together. A pull-up resistor is required on the common GCB in order to guarantee the rise time as follows:

$$\text{Eq. 6 } \tau = R_{GCB} C_{GCB} \leq 1\mu s,$$

where R_{GCB} is the pull up resistor value and C_{GCB} is the bus loading. The pull-up resistor should be tied to an external supply voltage in range from 3.3 to 5 V, which should be present prior to or during power-up. If exploring untested compensation or deadtime configurations, it is recommended that 27 Ω series resistors are placed between the GCB pin of each product and the common GCB connection. This will avoid propagation of faults between products potentially caused by hazardous configuration settings. When the configurations of the products are settled the series resistors can be removed.

Fault spreading

The product can be configured to broadcast a fault event over the GCB bus to the other devices in the group. When a non-destructive fault occurs and the device is configured to shut down on a fault, the device will shut down and broadcast the fault event over the GCB bus. The other devices on the GCB bus will shut down together if configured to do so, and will attempt to re-start in their prescribed order if configured to do so.

Over Temperature Protection (OTP)

The products are protected from thermal overload by an internal over temperature shutdown circuit. When T_{P1} as defined in thermal consideration section exceeds 120°C the product will shut down. The product will make continuous attempts to start up and resume normal operation automatically when the temperature has dropped $>15^\circ\text{C}$ below the over temperature threshold. The specified OTP level and hysteresis are valid for worst case operation regarding cooling conditions, input voltage and output voltage. This means the OTP level and hysteresis in many cases will be lower. The OTP level, hysteresis, and fault response of the product can be reconfigured using the PMBus interface. The fault response can be configured as follows:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts (default configuration).
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

Optimization examples

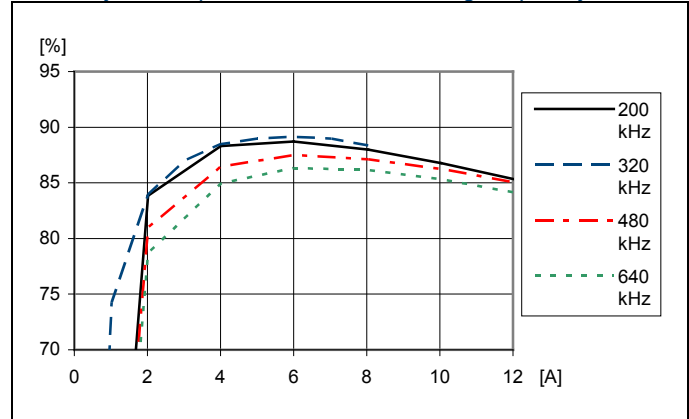
This product is designed with a digital control circuit. The control circuit uses a configuration file which determines the functionality and performance of the product. It is possible to change the configuration file to optimize certain performance characteristics. In the table below is a schematic view on how to change different configuration parameters in order to achieve an optimization towards a wanted performance.

↑	Increase
→	No change
↓	Decrease

Config. parameters	Switching frequency	Control loop bandwidth	NLR threshold	Diode emulation (DCM)	Min. pulse
Optimized performance					
Maximize efficiency	↓	→	↑	Enable	Disable
Minimize ripple ampl.	↑	→	↑	Enable or disable	Enable or disable
Improve load transient response	↑	↑	↓	Disable	Disable
Minimize idle power loss	↓	↑	→	Enable	Enable

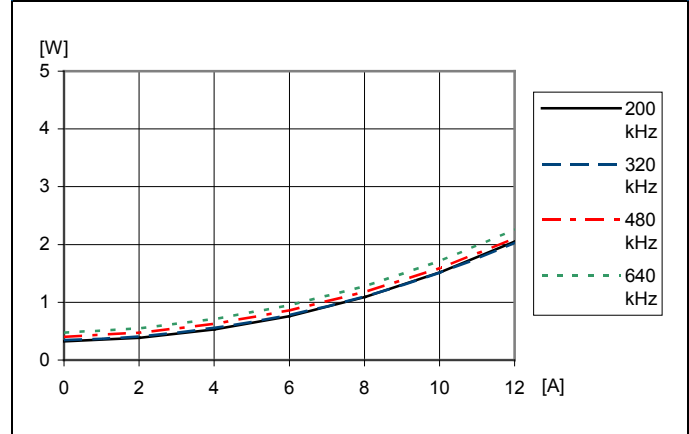
P _{ii}	Input idling power (no load)	Default configuration: Continues Conduction Mode, CCM	V _O = 0.6 V	0.36	W
			V _O = 1.0 V	0.35	
			V _O = 3.3 V	0.54	
			V _O = 5.0 V	0.97	
		DCM, Discontinues Conduction Mode (diode emulation)	V _O = 0.6 V	0.30	W
			V _O = 1.0 V	0.37	
			V _O = 3.3 V	0.41	
			V _O = 5.0 V	0.45	
P _{ii}	Input idling power (no load)	DCM with Adaptive Frequency and Minimum Pulse Enabled	V _O = 0.6 V	0.29	W
			V _O = 1.0 V	0.35	
			V _O = 3.3 V	0.37	
			V _O = 5.0 V	0.42	
		DCM with Adaptive Frequency and Minimum Pulse Disabled	V _O = 0.6 V	0.25	W
			V _O = 1.0 V	0.20	
			V _O = 3.3 V	0.20	
			V _O = 5.0 V	0.20	
P _{CTRL}	Input standby power	Turned off with CTRL-pin	Default configuration: Monitoring enabled, Precise timing enabled	180	mW
			Monitoring enabled, Precise timing disabled	120	mW
			Low power mode: Monitoring disabled, Precise timing disabled	85	mW
V _{tr1}	Load transient peak voltage deviation	Default configuration di/dt = 2 A/μs C _O =470 μF	V _O = 0.6 V	55	mV
			V _O = 1.0 V	65	
			V _O = 3.3 V	110	
			V _O = 5.0 V	190	
	Load step 25-75-25% of max I _O	Optimized PID and NLR configuration di/dt = 2 A/μs C _O =470 μF	V _O = 0.6 V	40	mV
			V _O = 1.0 V	35	
			V _O = 3.3 V	55	
			V _O = 5.0 V	105	
t _{tr1}	Load transient recovery time	Default configuration di/dt = 2 A/μs C _O =470 μF	V _O = 0.6 V	230	us
			V _O = 1.0 V	210	
			V _O = 3.3 V	200	
			V _O = 5.0 V	200	
	Load step 25-75-25% of max I _O	Optimized PID and NLR configuration di/dt = 2 A/μs C _O =470 μF	V _O = 0.6 V	45	us
			V _O = 1.0 V	40	
			V _O = 3.3 V	40	
			V _O = 5.0 V	35	

Efficiency vs. Output Current and Switching frequency



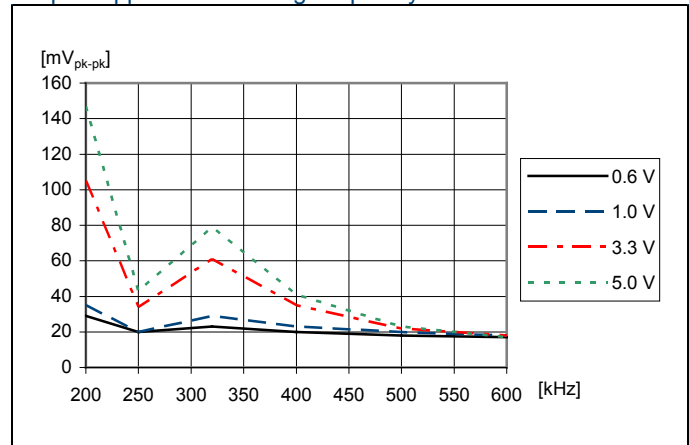
Efficiency vs. load current and switching frequency at T_{P1} = +25°C, V_I=12 V, V_O=3.3V, C_O=470 μF/10 mΩ. Default configuration except changed frequency

Power Dissipation vs. Output Current and Switching frequency



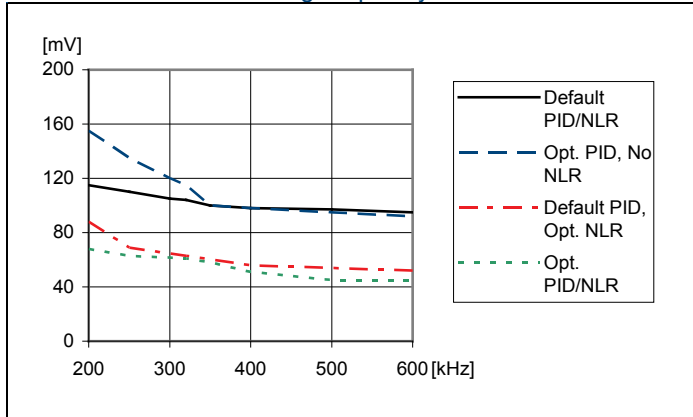
Dissipated power vs. load current and switching frequency at T_{P1} = +25°C, V_I=12 V, V_O=3.3V, C_O=470 μF/10 mΩ. Default configuration except changed frequency

Output Ripple vs. Switching frequency



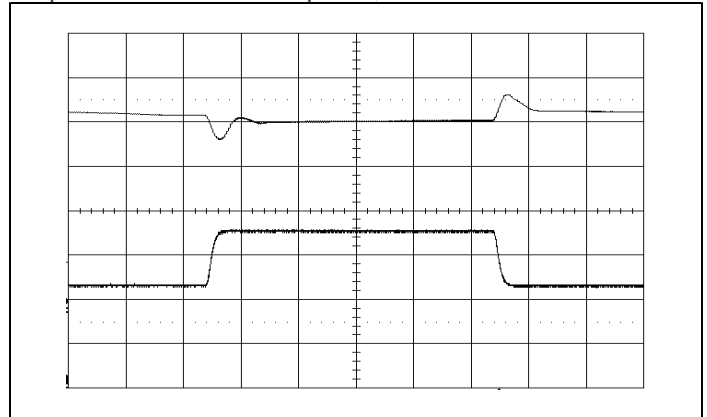
Output voltage ripple V_{pk-pk} at: T_{P1} = +25°C, V_I = 12 V, C_O=470 μF/10 mΩ, I_O = 12 A resistive load. Default configuration except changed frequency.

Load transient vs. Switching frequency



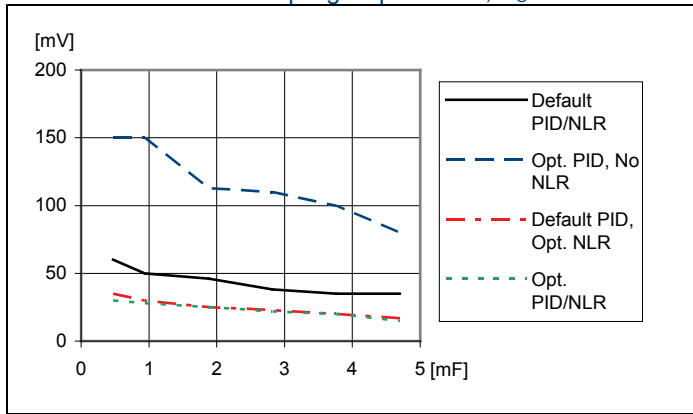
Load transient peak voltage deviation vs. frequency. Step-change (3-9-3 A). $T_{P1} = +25^{\circ}\text{C}$. $V_I=12\text{ V}$, $V_O=3.3\text{ V}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$

Output Load Transient Response, Default PID/NLR



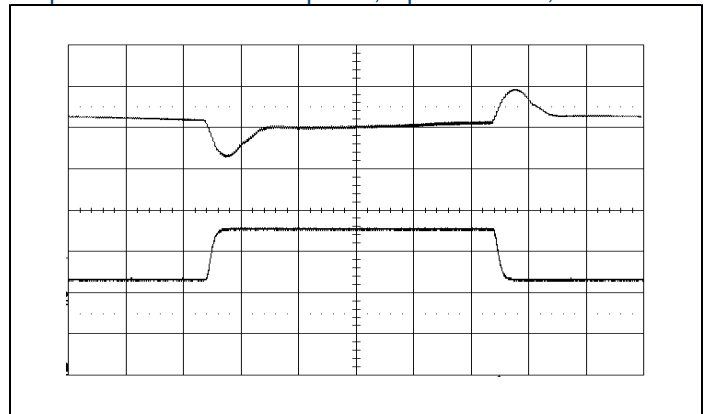
Output voltage response to load current step-change (3-9-3 A) at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$, $di/dt=2\text{ A}/\mu\text{s}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$ Default PID Control Loop and NLR
Top trace: output voltage (200 mV/div.). Bottom trace: load current (5 A/div.). Time scale: (0.1 ms/div.).

Load Transient vs. Decoupling Capacitance, $V_O=1.0\text{ V}$



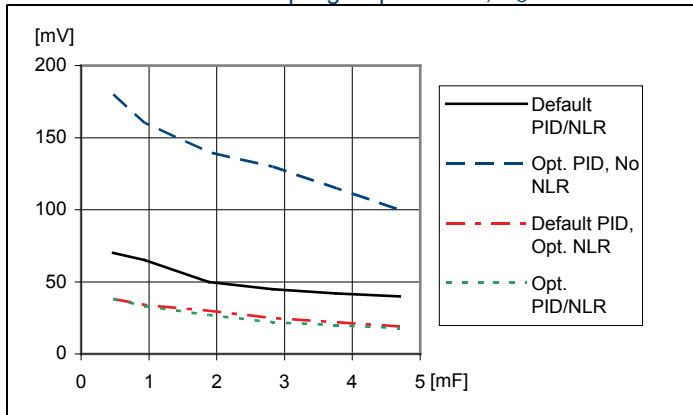
Load transient peak voltage deviation vs. decoupling capacitance. Step-change (3-9-3 A). Parallel coupling of capacitors with $470\text{ }\mu\text{F}/10\text{ m}\Omega$, $T_{P1} = +25^{\circ}\text{C}$. $V_I=12\text{ V}$, $V_O=1.0\text{ V}$, $f_{sw}=320\text{ kHz}$, $di/dt=2\text{ A}/\mu\text{s}$

Output Load Transient Response, Optimized PID, no NLR



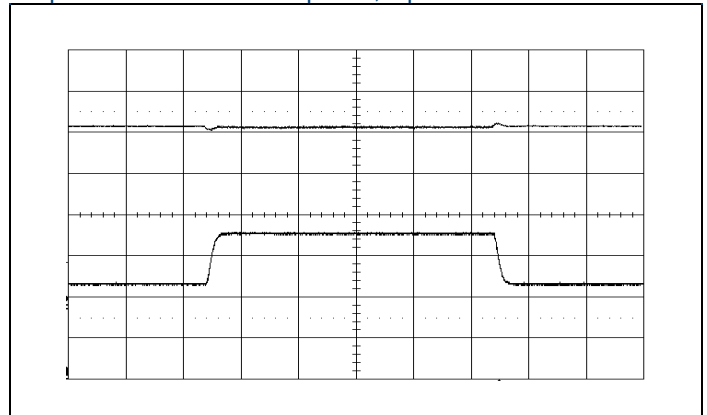
Output voltage response to load current step-change (3-9-3 A) at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$, $di/dt=2\text{ A}/\mu\text{s}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$ Optimized PID Control Loop and no NLR
Top trace: output voltage (200 mV/div.). Bottom trace: load current (5 A/div.). Time scale: (0.1 ms/div.).

Load Transient vs. Decoupling Capacitance, $V_O=3.3\text{ V}$



Load transient peak voltage deviation vs. decoupling capacitance. Step-change (3-9-3 A). Parallel coupling of capacitors with $470\text{ }\mu\text{F}/10\text{ m}\Omega$, $T_{P1} = +25^{\circ}\text{C}$. $V_I=12\text{ V}$, $V_O=3.3\text{ V}$, $f_{sw}=320\text{ kHz}$, $di/dt=2\text{ A}/\mu\text{s}$

Output Load Transient Response, Optimized NLR



Output voltage response to load current step-change (3-9-3 A) at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$, $di/dt=2\text{ A}/\mu\text{s}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$ Default PID Control Loop and optimized NLR
Top trace: output voltage (200 mV/div.). Bottom trace: load current (5 A/div.). Time scale: (0.1 ms/div.).

Thermal Consideration

General

The product is designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation.

Cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependant on the airflow across the product. Increased airflow enhances the cooling of the product.

The Output Current Derating graph found in the Output section for each model provides the available output current vs. ambient air temperature and air velocity at specified V_i .

The product is tested on a 254 x 254 mm, 35 μm (1 oz), test board mounted vertically in a wind tunnel with a cross-section of 608 x 203 mm. The test board has 8 layers.

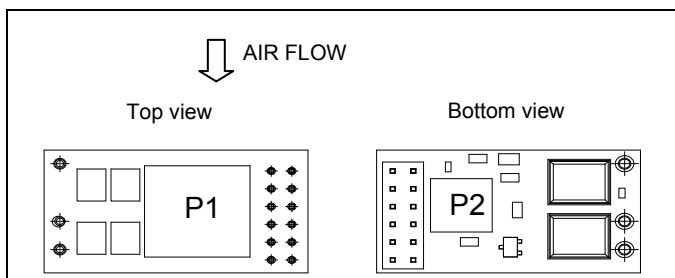
Proper cooling of the product can be verified by measuring the temperature at positions P1 and P2. The temperature at these positions should not exceed the max values provided in the table below.

Note that the max value is the absolute maximum rating (non destruction) and that the electrical Output data is guaranteed up to $T_{P1} + 95^\circ\text{C}$.

Definition of product operating temperature

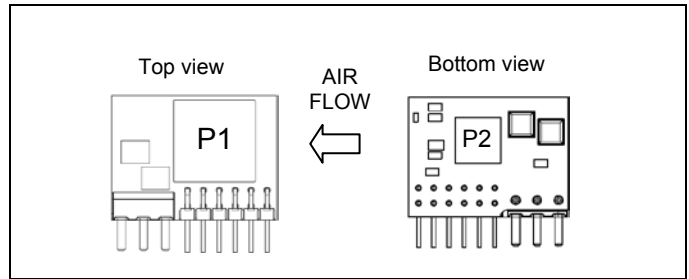
The product operating temperatures are used to monitor the temperature of the product, and proper thermal conditions can be verified by measuring the temperature at positions P1 and P2. The temperature at these positions (T_{P1} , T_{P2}) should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology. Temperatures above maximum T_{P1} , measured at the reference point P1 are not allowed and may cause permanent damage.

Position	Description	Max Temp.
P1	Reference point, L1, inductor	120°C
P2	N1, control circuit	120°C



Temperature positions and air flow direction.

SIP version

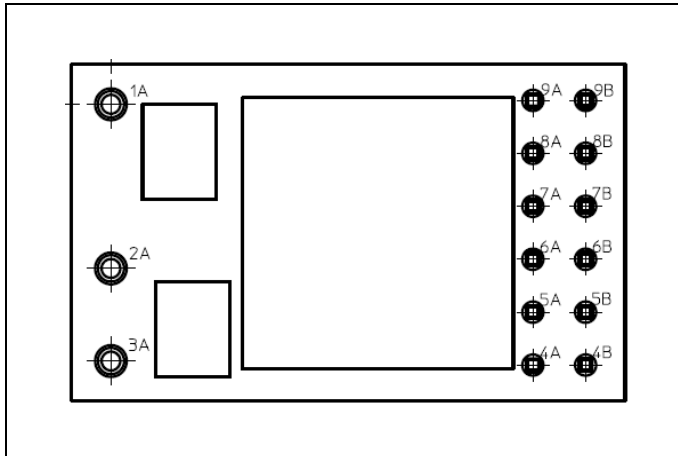


Temperature positions and air flow direction.

Definition of reference temperature T_{P1}

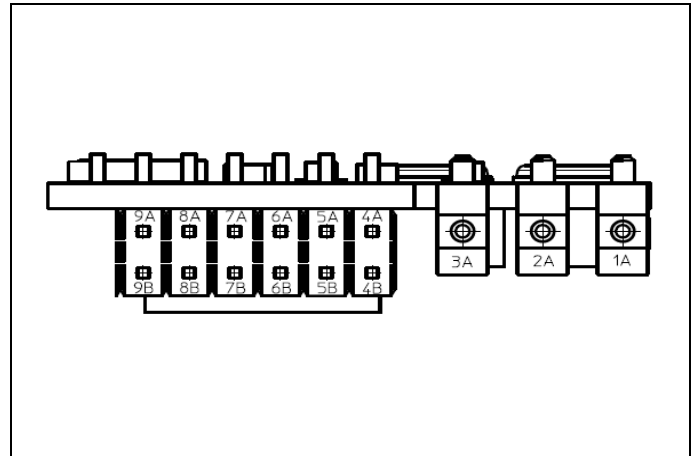
The reference temperature is used to monitor the temperature limits of the product. Temperature above maximum T_{P1} , measured at the reference point P1 is not allowed and may cause degradation or permanent damage to the product. T_{P1} is also used to define the temperature range for normal operating conditions. T_{P1} is defined by the design and used to guarantee safety margins, proper operation and high reliability of the product.

Connections (Horizontal & SMT versions)



Pin layout, top view (component placement for illustration only).

Connections (SIP version)



Pin layout, bottom view (component placement for illustration only).

Pin	Designation	Function
1A	VIN	Input Voltage
2A	GND	Power Ground
3A	VOUT	Output Voltage
4A	VTRK or PG *	Voltage Tracking input or Power Good
4B	PREF	Pin-strap reference
5A	+S	Positive sense
5B	-S	Negative sense
6A	SA0	PMBus address pinstrap
6B	GCB	Group Communication Bus
7A	SCL	PMBus Clock
7B	SDA	PMBus Data
8A	VSET	Output voltage pinstrap
8B	SYNC	Synchronization I/O
9A	SALERT	PMBus Alert
9B	CTRL	Remote Control

Pin	Designation	Function
1A	VIN	Input Voltage
2A	GND	Power Ground
3A	VOUT	Output voltage
4A	+S	Positive sense
4B	-S	Negative sense
5A	VSET	Output voltage pin-strap
5B	VTRK	Voltage tracking input
6A	SALERT	PMBus Alert
6B	SDA	PMBus data
7A	SCL	PMBus Clock
7B	SYNC	Synchronization I/O
8A	SA0	PMBus address pin-strap
8B	CTRL	Remote Control
9A	GCB	Group Communication Bus
9B	PREF	Pin-strap Reference

* For these products the PG pin is internally tied to the VTRK input of the products' controller. Typically the VTRK input bias current will be equivalent to a 50 kohm pull-down resistor. This should be considered when choosing pull-up resistor for the PG signal.

Unused input pins

Unused SDA, SCL and GCB pins should still have pull-up resistors as specified.

Unused VTRK or SYNC pins should be left unconnected or connected to the PREF pin.

Unused CTRL pin can be left open due to internal pull-up. VSET and SA0/SA1 pins must have pinstrap resistors as specified.

PWB layout considerations

The pinstrap resistors, R_{SET} , and R_{SA0}/R_{SA1} should be placed as close to the product as possible to minimize loops that may pick up noise.

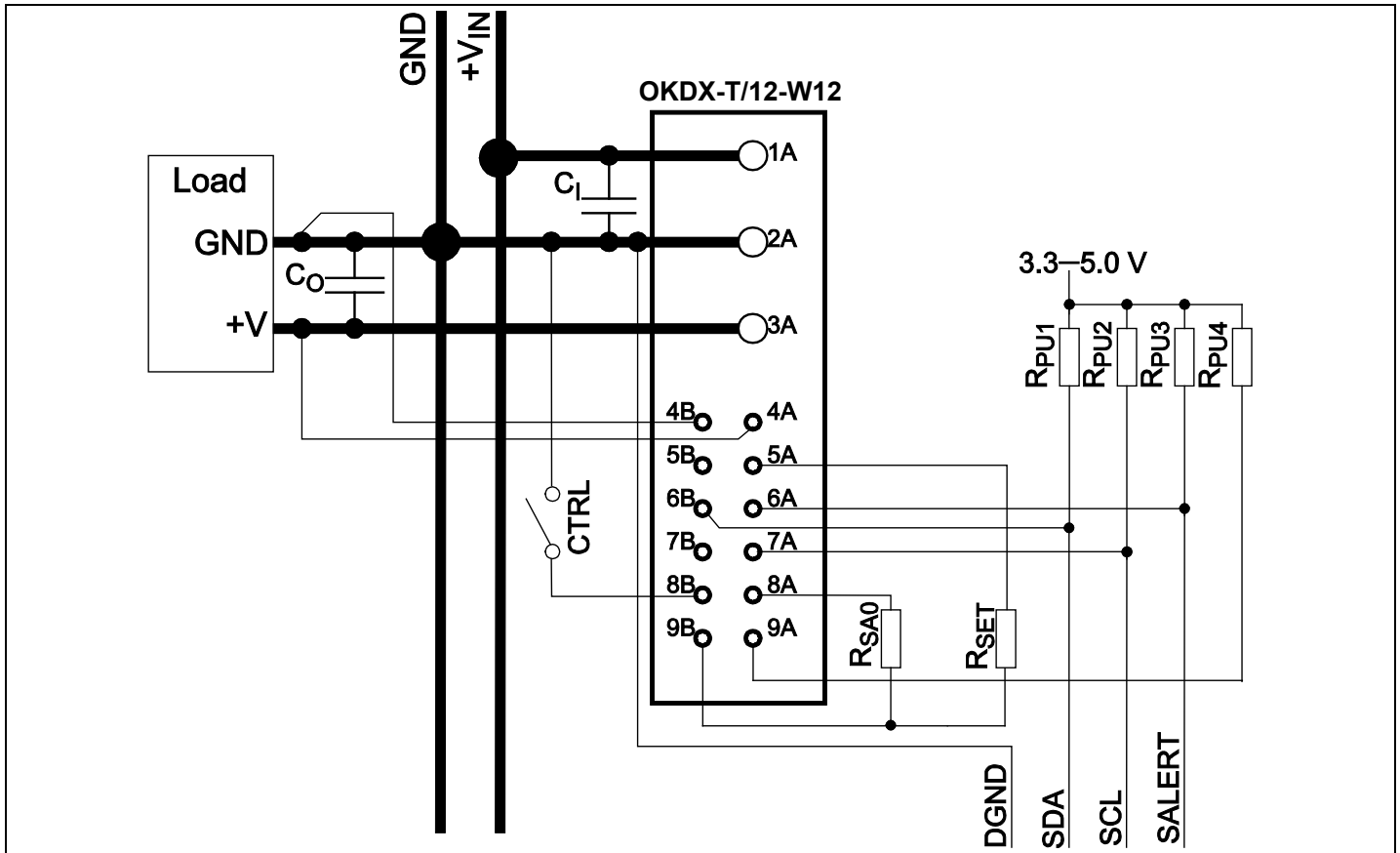
Avoid current carrying planes under the pinstrap resistors and the PMBus signals.

The capacitor C_I (or capacitors implementing it) should be placed as close to the input pins as possible.

Capacitor C_O (or capacitors implementing it) should be placed close to the load.

Care should be taken in the routing of the connections from the sensed output voltage to the S+ and S- terminals. These sensing connections should be routed as a differential pair, preferably between ground planes which are not carrying high currents. The routing should avoid areas of high electric or magnetic fields.

Typical Application Circuit (SIP version)



Standalone operation with PMBus communication. Top view of product footprint.

PMBus interface

This product provides a PMBus digital interface that enables the user to configure many aspects of the device operation as well as to monitor the input and output voltages, output current and device temperature. The product can be used with any standard two-wire I²C or SMBus host device. In addition, the product is compatible with PMBus version 1.1 and includes an SALERT line to help mitigate bandwidth limitations related to continuous fault monitoring. The product supports 100 kHz bus clock frequency only. The PMBus signals, SCL, SDA and SALERT require passive pull-up resistors as stated in the SMBus Specification. Pull-up resistors are required to guarantee the rise time as follows:

$$\text{Eq. 7} \quad \tau = R_p C_p \leq 1 \mu s$$

where R_p is the pull-up resistor value and C_p is the bus loading, the maximum allowed bus load is 400 pF. The pull-up resistor should be tied to an external supply voltage in range from 2.7 to 5.5 V, which should be present prior to or during power-up. If the proper power supply is not available, voltage dividers may be applied. Note that in this case, the resistance in the equation above corresponds to parallel connection of the resistors forming the voltage divider.

Monitoring via PMBus

the PMBus interface. Fault conditions can be monitored using the SALERT pin, which will be asserted when any number of pre-configured fault or warning conditions occur. It is also possible to continuously monitor one or more of the power conversion parameters including but not limited to the following:

- Input voltage
- Output voltage
- Output current
- Internal junction temperature
- Switching frequency
- Duty cycle

In the default configuration monitoring is enabled also when the output voltage is disabled. This can be changed in order to reduce standby power consumption.

Snap shot parameter capture

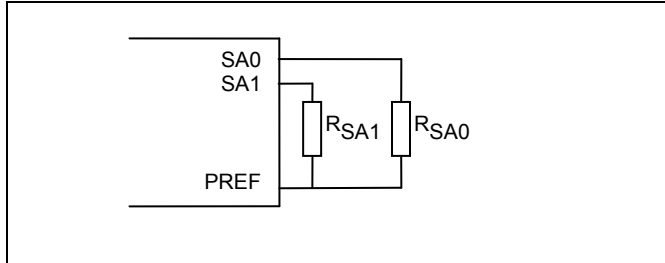
This product offers a special feature that enables the user to capture parametric data during normal operation or following a fault. The following parameters are stored:

- Input voltage
- Output voltage
- Output current
- Internal junction temperature
- Switching frequency
- Duty cycle
- Status registers

The Snapshot feature enables the user to read the parameters via the PMBus interface during normal operation, although it should be noted that reading the 22 bytes will occupy the bus for some time. The Snapshot enables the user to store the snapshot parameters to Flash memory in response to a pending fault as well as to read the stored data from Flash memory after a fault has occurred. Automatic store to Flash memory following a fault is triggered when any fault threshold level is exceeded, provided that the specific fault response is to shut down. Writing to Flash memory is not allowed if the device is configured to restart following the specific fault condition. It should also be noted that the device supply voltage must be maintained during the time the device is writing data to Flash memory; a process that requires between 700-1400 μs depending on whether the data is set up for a block write. Undesirable results may be observed if the input voltage of the product drops below 3.0 V during this process.

PMBus addressing

The PMBus address should be configured with resistors connected between the SA0/SA1 pins and the PREF pin, as shown in the figure below. Recommended resistor values for hard-wiring PMBus addresses are shown in the table. 1% tolerance resistors are required.



Schematic of connection of address resistor.

Index	R _{SA} [kΩ]	Index	R _{SA} [kΩ]
0	10	13	34.8
1	11	14	38.3
2	12.1	15	42.2
3	13.3	16	46.4
4	14.7	17	51.1
5	16.2	18	56.2
6	17.8	19	61.9
7	19.6	20	68.1
8	21.5	21	75
9	23.7	22	82.5
10	26.1	23	90.9
11	28.7	24	100
12	31.6		

The PMBus address follows the equation below:

Eq. 8 PMBus Address (decimal) = 25 x (SA1 index) + (SA0 index)

The user can theoretically configure up to 625 unique PMBus addresses, however the PMBus address range is inherently limited to 128. Therefore, the user should use index values 0 - 4 on the SA1 pin and the full range of index values on the SA0 pin, which will provide 125 device address combinations.

Products with no SA1 pin have an internally defined SA1 index as follows.

Product	SA1 index
All models	4

Optional PMBus Addressing

Alternatively the PMBus address can be defined by connecting the SA0/SA1 pins according to the table below. SA1 = open for products with no SA1 pin.

		SA0		
		low	open	high
SA1	low	20h	21h	22h
	open	23h	24h	25h
	high	26h	27h	Reserved

Low = Shorted to PREF
 Open = High impedance
 High = Logic high, GND as reference,
 Logic High definitions see Electrical Specification

Reserved Addresses

Address 4Bh is allocated for production needs and can not be used.

Addresses listed in the table below are reserved or assigned according to the SMBus specification and may not be usable. Refer to the SMBus specification for further information.

Address (decimal)	Comment
0	General Call Address / START byte
1	CBUS address
2	Address reserved for different bus format
3-7	Reserved for future use
8	SMBus Host
9-11	Assigned for Smart Battery
12	SMBus Alert Response Address
40	Reserved for ACCESS.bus host
44-45	Reserved by previous versions of the SMBus specification
55	Reserved for ACCESS.bus default address
64-68	Reserved by previous versions of the SMBus specification
72-75	Unrestricted addresses
97	SMBus Device Default Address
120-123	10-bit slave addressing
124-127	Reserved for future use