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OL2381

Highly integrated single-chip sub 1 GHz RF transceiver

Rev. 1 — 30 November 2011

Product data sheet

1. General description

A highly integrated single-chip transceiver solution, the OL2381 is ideally suited to telemetry applications operating in the ISM/SRD bands. The small form factor, low power consumption and wide supply voltage range make this device suitable for use in battery powered, handheld devices and their counter parts.

The device utilizes a fully integrated, programmable fractional-N PLL (including loop filter) to control the Local Oscillator (LO), thus supporting multi-channel operation and frequency hopping schemes. This feature also allows programmable frequency steps for crystal (XTAL) drift compensation.

The device can employ ASK, FSK or GFSK type modulation. The ASK modulation characteristics are fully programmable by varying the power amplifier output power in accordance with the TX data. The FSK modulation utilizes the fractional-N PLL capability to precisely modulate the LO frequency with the TX data (in loop modulation). Relaxed narrow band applications can utilize an on-chip GFSK type modulation to improve the spectral occupancy.

The device is based on a low IF direct conversion receiver architecture, with on-chip IF filtering and programmable channel bandwidth. After filtering and amplification the quadrature signals are digitized, demodulated and processed in the digital domain.

Baseband processing of the received signal comprises a demodulator, a data-slicer and clock recovery followed by a Manchester decoder. Automated signal signature recognition units are available to allow simple, fast and reliable data reception.

The device is controlled via a three-wire serial interface (SPI) with data input and output, data clock and interface enable. The interface can be configured to a full SPI interface with separate data and clock pins. Additional pins are available to access internal signals in real-time.

2. Features and benefits

- Highly integrated solution for the 315/434/868/915 MHz band
- Very few external components required
- Complies with ETSI EN300-220/FCC part 15 standards
- Near zero-IF RX architecture
- On-chip channel filtering with automatic calibration supported to provide stable cut-off frequencies and filter roll-off
- Multi-channel TX and RX operation by fully integrated fractional-N PLL with on-chip loop filter



- Automatic VCO sub-band selection and calibration to reduce PLL loop bandwidth variation
- Programmable ASK/FSK modulation with Manchester codec
- Programmable transmitter output power (–20 dBm to +10 dBm), stabilized with onboard PA regulator
- Digital RSSI with a configurable threshold
- Onboard Signal Signature Recognition Unit (SSRU) with Preamble Pattern Recognition (PPR)
- Configurable RX polling timer with 2 % absolute accuracy
- Level Sensitive Data (LSD) slicer with self-adjusting threshold
- Low power consumption (RX 16 mA, TX 13 mA at 6 dBm), with ultra Low 0.5 μ A standby current and configurable polling timer
- Single lithium cell operation (2.1 V). Operation up to 3.6 V fully supported
- 32-Pin HVQFN32 Pb-free package

3. Applications

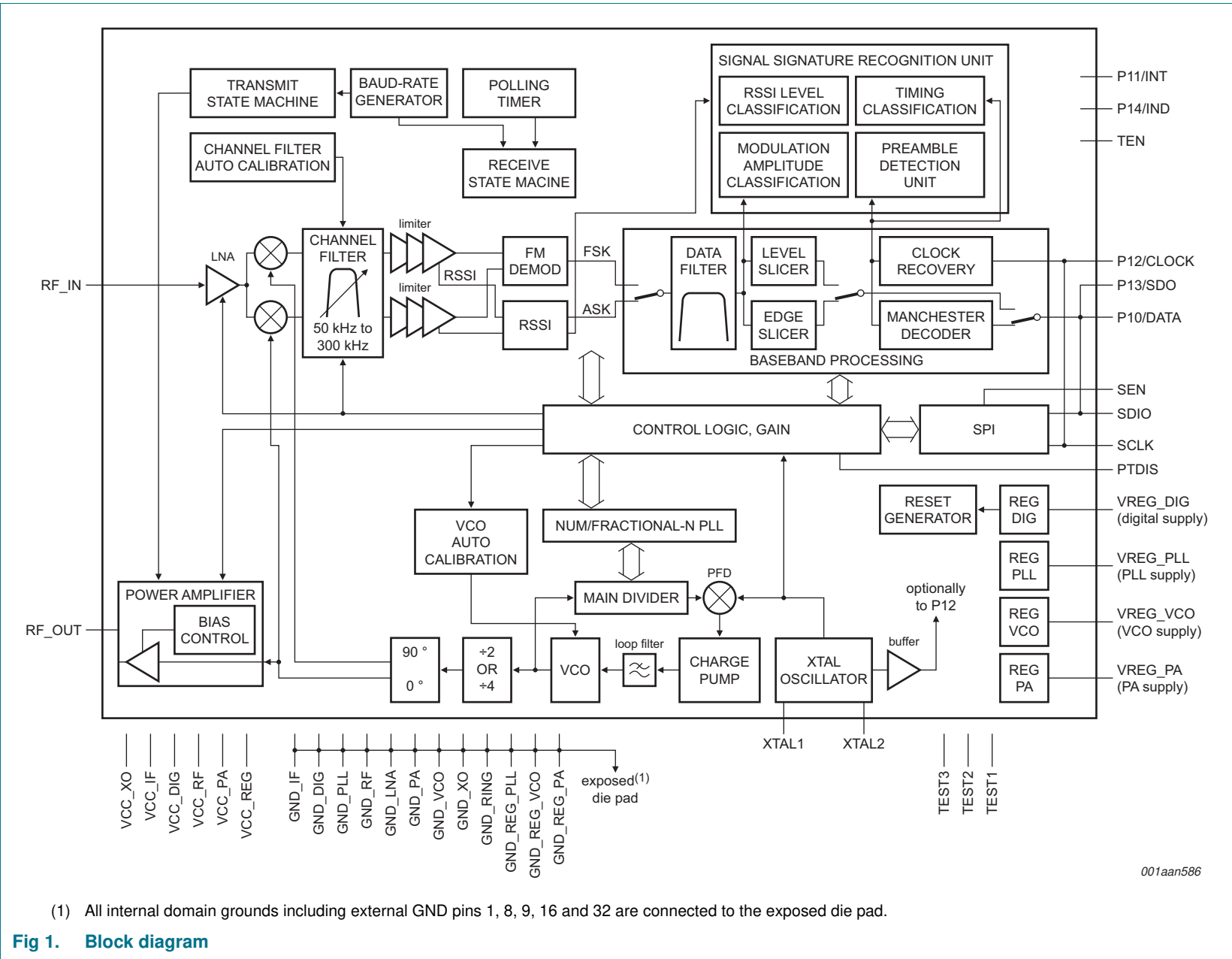
- Smart metering (wireless M-bus)
- Home and building security and automation (KNX-RF)
- Remote control devices
- After-market Remote Keyless Entry (RKE)
- Wireless medical applications
- Wireless sensor network

4. Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
OL2381AHN	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-3

5. Block diagram



(1) All internal domain grounds including external GND pins 1, 8, 9, 16 and 32 are connected to the exposed die pad.

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

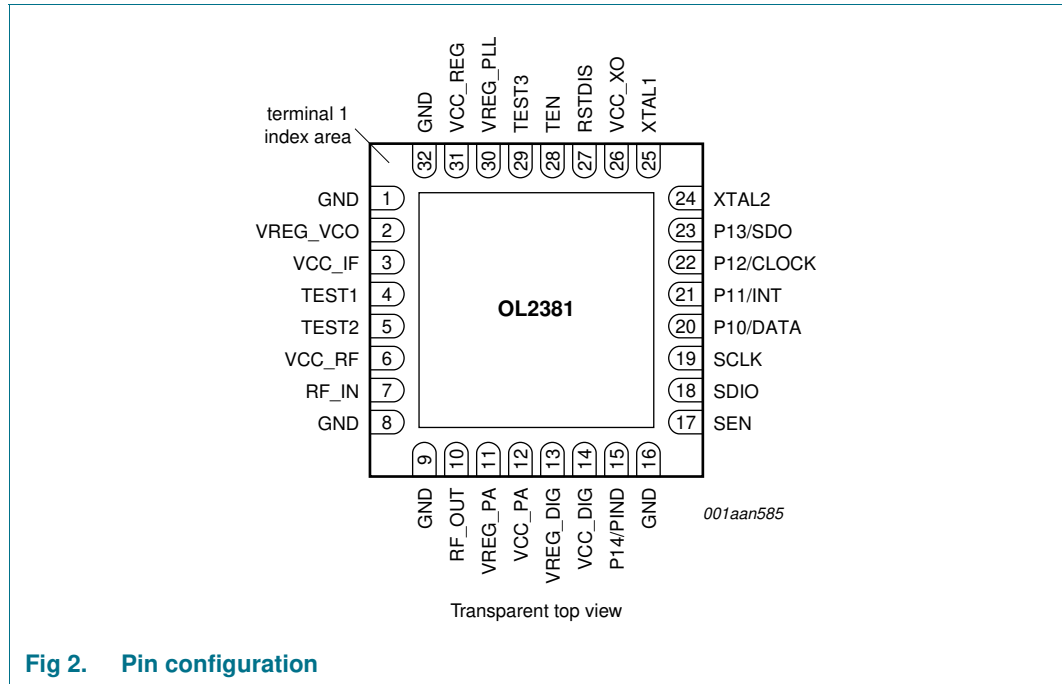


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Reset state	Description
GND	1	-	-	ground; use exposed heatsink as ground reference
VREG_VCO	2	A	Z	VCO regulator output voltage to decoupling capacitor
VCC_IF	3	A	A	IF section power supply
TEST1	4	A	Z	RX test I output
TEST2	5	A	Z	RX test Q output
VCC_RF	6	A	A	LNA power supply
RF_IN	7	A	A	RX RF signal input
GND	8	-	-	ground; use exposed heatsink as ground reference
GND	9	-	-	ground; use exposed heatsink as ground reference
RF_OUT	10	A	Z	TX RF signal output
VREG_PA	11	A	Z	power amplifier regulator output voltage to decoupling capacitor
VCC_PA	12	A	A	power amplifier power supply
VREG_DIG	13	A	A	digital regulator output voltage to decoupling capacitor
VCC_DIG	14	A	A	digital module supply voltage
P14/PIND	15	DO	Z	digital output port with increased drive capability for PIN diode control

Table 2. Pin description ...continued

Symbol	Pin	Type	Reset state	Description
GND	16	-	-	ground; use exposed heatsink as ground reference
SEN	17	DI	DI	serial interface enable
SDIO	18	DIO	DI	serial interface input/output
SCLK	19	DIO	DI	serial interface clock
P10/DATA	20	DleO	Z	digital output port, TX data input, RX data output, data output of debug interface
P11/INT	21	DO	POR, interrupt output	digital output port, interrupt output, several status indicators, reference clock output, frame indicator of debug interface
P12/CLOCK	22	DO	1 MHz reference clock	digital output port, TX/reference clock out, RX data clock, clock of debug interface
P13/SDO	23	DO	Z	digital output port, status indicators, serial interface data output
XTAL2	24	A	A	crystal reference clock frequency input
XTAL1	25	A	A	crystal connection
VCC_XO	26	A	A	crystal oscillator supply voltage
RSTDIS	27	DI	DI	reset disable signal
TEN	28	DI	DI	test enable input
TEST3	29	A	Z	PLL test output
VREG_PLL	30	A	Z	PLL regulator output voltage to decoupling capacitor
VCC_REG	31	A	A	PLL, VCO regulators power supply
GND	32	-	-	ground; use exposed heatsink as ground reference
exposed die pad	-	A	GND	ground connection

- [1] A = analog.
 DI = digital input.
 DO = digital output with enable signal.
 DIO = digital input without enable signal and output with enable signal.
 DleO = digital input and output both with enable signal.

7. Functional description

7.1 General architecture description

The OL2381 transceiver is designed for use in both complex base-stations, when paired with powerful microcontrollers, and low component-count remote units with low pin-count microcontrollers. The IC features unique configuration possibilities via external pin-level configuration or SFR bit manipulation. Several automatic sequences are implemented to ease device operation, all of which can be manually influenced or overridden by control-bits.

7.1.1 Power management

The device contains a configurable power-on reset block. The device control registers are reset as the external voltage rises to ensure that the device state is in Standby mode. This is implemented by ensuring that all blocks are off except the SPI and the digital regulator. Note that the digital regulator is operating in clamp mode at this time.

7.1.2 XTAL oscillator

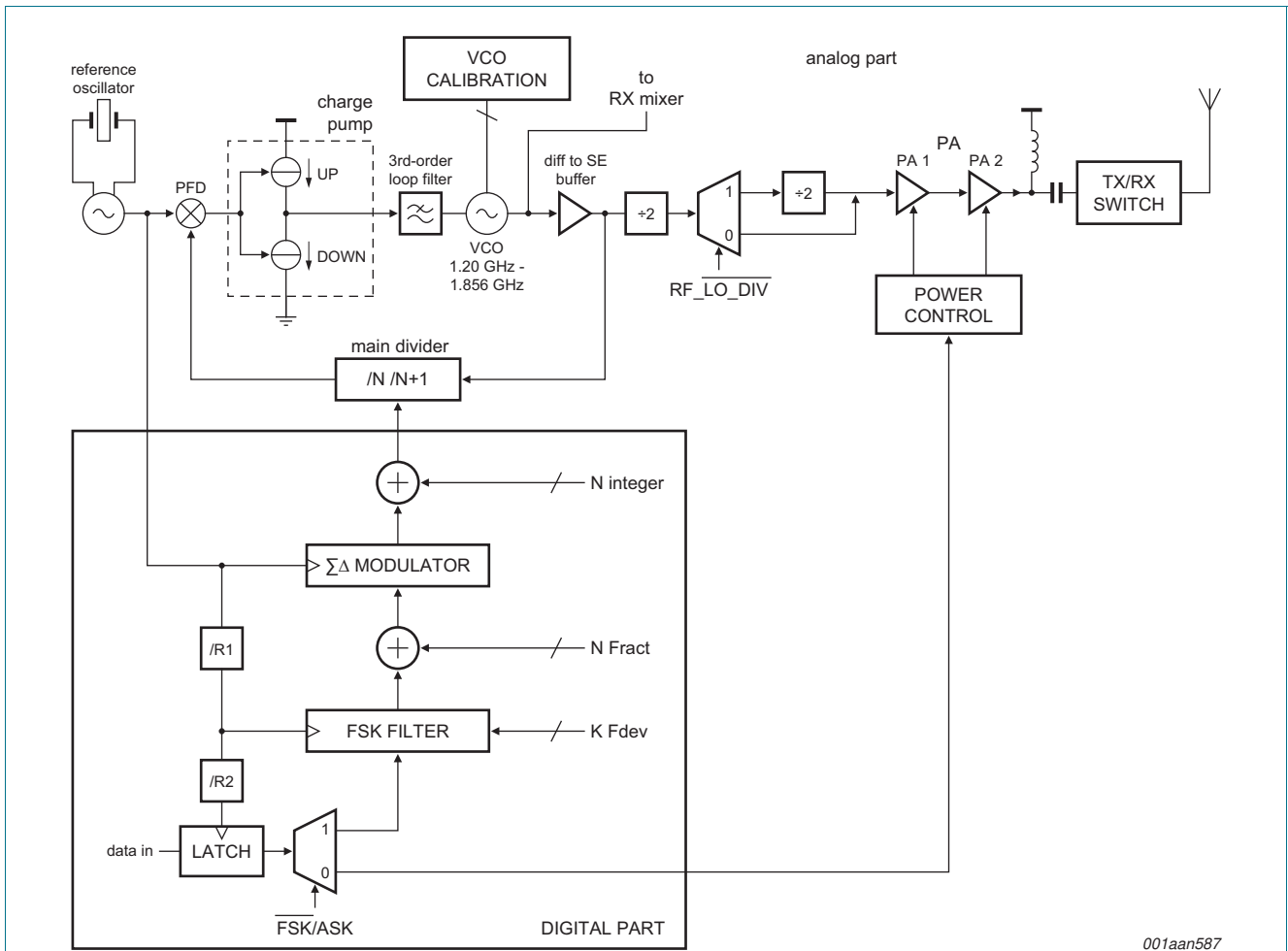
The main time-reference is derived from an amplitude-controlled XTAL oscillator. This 16 MHz reference is used as a reference clock for the PLL and as a timing reference for various analog calibration purposes.

7.1.3 Polling timer

Several base-station applications require a low-power polling timer for periodic device wakeup. This feature is essential to enable listening in pre-programmed time-windows when the OL2381 is used in RX mode applications. Internal configuration and trimming registers allow the setting of a wide range of different timer intervals while achieving an average timing accuracy of 2 %.

7.1.4 TX block

The TX section is able to operate within all ISM bands: 315 MHz, 434 MHz, 868 MHz and 916 MHz. The device provides a high degree of flexibility and is capable of ASK/FSK modulation, output power control and on-chip baud-rate generation with data rates up to 112 kchip/s. The device features multi-channel operation and enables carrier frequency adjustment and compensation of XTAL frequency offsets due to its high resolution fractional-N PLL architecture. The TX block features a high degree of integration, employing an on-chip VCO and PLL loop filter.



001aan587

Fig 3. TX block diagram

7.1.5 VCO calibration

On-chip calibration is available to reduce the VCO input voltage range and thus reduce the PLL loop bandwidth variation. The variation in system parameters such as locking time and LO phase noise can therefore be maintained within a tight window.

Calibration is performed by selecting the proper VCO sub-band according to the desired channel frequency. VCO sub-band selection and the PLL start-up sequence can be triggered by command and are supported by an automatic flow sequence. This flow can be overridden if required. Note that if the incorrect sub-band is chosen the VCO calibration is unable to tune to the desired frequency.

7.1.6 TX command

TX parameters (frequency, modulation, output power etc) can be predefined to enable fast and simple entry into TX mode (PA switched on).

7.1.7 RX block

The OL2381's RX path consists of a broadband resistive-feedback LNA, a mixer (mixing down the input signal to an IF of 300 kHz), a channel-filter, a limiter, an RSSI stage (AM demodulation) and a base-band signal processing block used for FM and AM data and clock recovery. The LNA, limiter and channel-filter gain settings can be configured via control bits. The channel filter bandwidth can also be adapted.

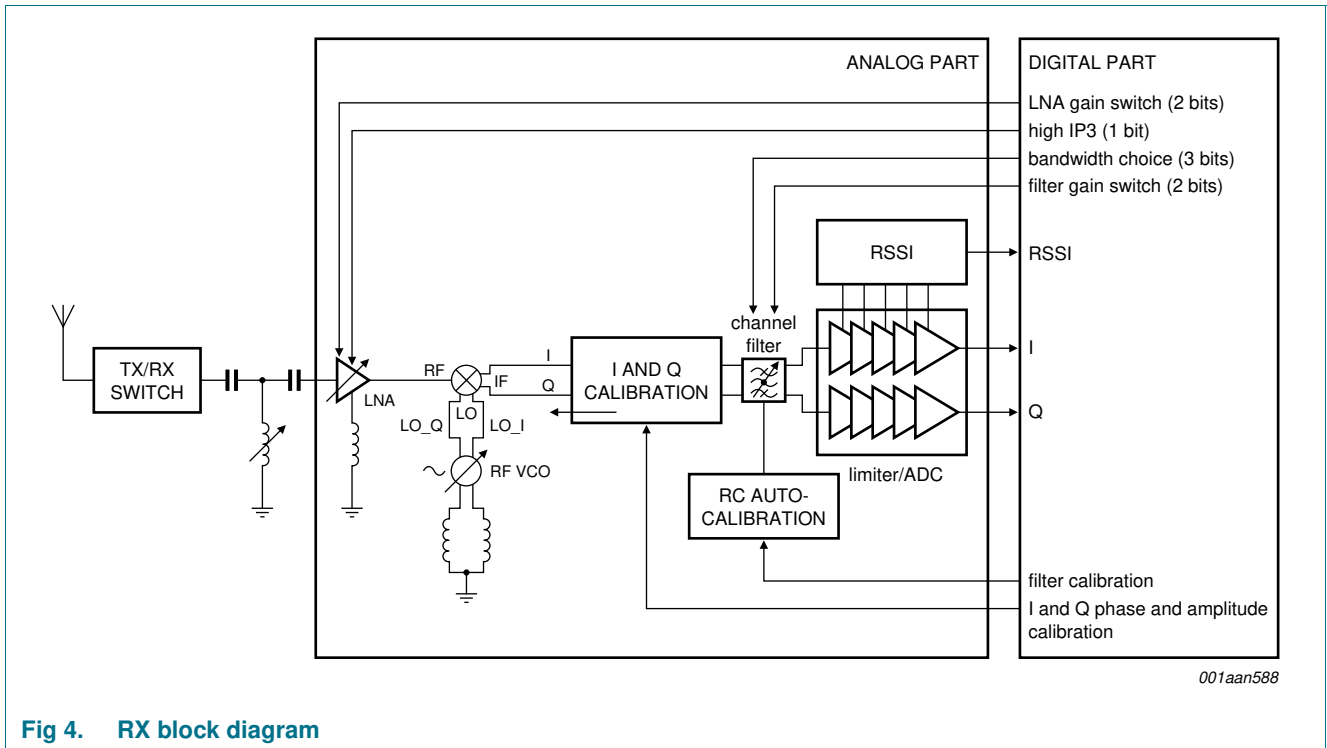


Fig 4. RX block diagram

7.1.8 Channel filter auto-calibration

Channel bandwidth accuracy requirements vary between applications. The modulation bandwidth changes with different bit rates. Bit rates can be 0.5 kbit/s to 112 kchip/s and the IF channel filter bandwidth must be set accordingly in the range 50 kHz to 300 kHz.

Channel bandwidth auto-calibration is implemented to maintain constant performance. This ensures stable cut-off frequencies and filter roll-off over process and temperature variations. This calibration is included in the RX command.

7.1.9 I/Q calibration

I/Q calibration can be implemented to improve the channel image rejection for certain applications. This calibration improves amplitude mismatch and phase quadrature between I and Q signals.

Both parameters can be trimmed by injecting an external RF signal operating in the image channel. The RSSI can then be used to determine the optimum settings to have the minimal remaining signal. This calibration is required for each frequency band.

The I/Q calibration settings are made available to -, and must be stored by, an external microcontroller.

7.1.10 Receive command

The predefined set of RX parameters (center frequency, modulation, etc.) enables Receive mode (receiver and LO buffers switched on) to be entered quickly after receiving the RX command. Several methods of signal signature recognition are implemented. These modes of semi-automatic signal processing can be pre-selected by the RX command.

7.1.11 Signal signature recognition unit

Several signal recognition units are implemented to provide fast and accurate signal detection. Signal signatures such as signal level (RSSI), modulation depth or baud-rate and coding can be automatically detected as wakeup criteria during the wakeup search phase.

7.1.12 Preamble detection

A configurable 1-bit to 32-bit pattern recognition unit can be implemented to aid power saving and avoid unintended wakeup due to ambient noise.

7.2 General operation

The OL2381 is a state machine-based transceiver to be used in conjunction with a microcontroller. Study this datasheet carefully to help choose the appropriate OL2381 configuration for a specific application. The interface to the microcontroller must be defined first, see [Section 7.3](#). Next, the correct basic settings must be identified. The operational frequency band must be chosen, all relevant registers must be programmed for TX and RX modes (exact setting of desired frequency, modulation, modulation depth, IF bandwidth, baseband filtering, etc). It is strongly recommended to study every aspect of this datasheet in detail and to verify correct device operation by measuring available debug-signals. The optimum operation and the highest device performance is achieved by fine-tuning and verification of all device settings. Use the automatic operating sequences after determining the optimum device configuration. Generally, the first operation is to bring the device from standby to power-up state, which is the precondition for any operation. This can be done manually, triggered by the external microcontroller, or automatically by the built-in polling timer. In this device mode, the XTAL oscillator is operational. SFR register bits (configuration data) can be changed. This mode can be left by issuing TX or RX commands. To save power and operating time the commands can be prepared by the 'prepare TX' or 'prepare RX' commands.

7.3 Interface description

7.3.1 Port connections

The minimum connection between a host controller and the OL2381 comprises three SPI lines: SDIO, SCLK and SEN. SPI communication and TX/RX data transfer can be achieved by multiplexing the SPI data and clock lines. The host controller's SPI must be set in slave mode after the RX/TX command is sent, the SCLK then shifts the out/in data via the host controller's SPI.

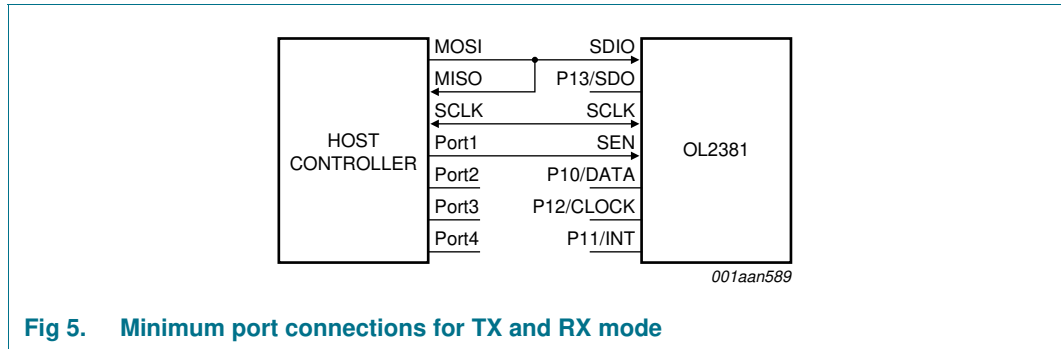


Fig 5. Minimum port connections for TX and RX mode

The device also supports full four-line SPI mode, the line SDIO serving as data input and P13/SDO as data output.

Alternatively, the device can be configured for separate data inputs and outputs. The lines SDIO, SCLK and, if selected, P13/SDO can be reserved for SPI command handling. In this case, TX and RX data is handled by the port pin P10/DATA, the clock is carried by port P12/CLOCK. The OL2381’s remaining ports can be used for additional status information.

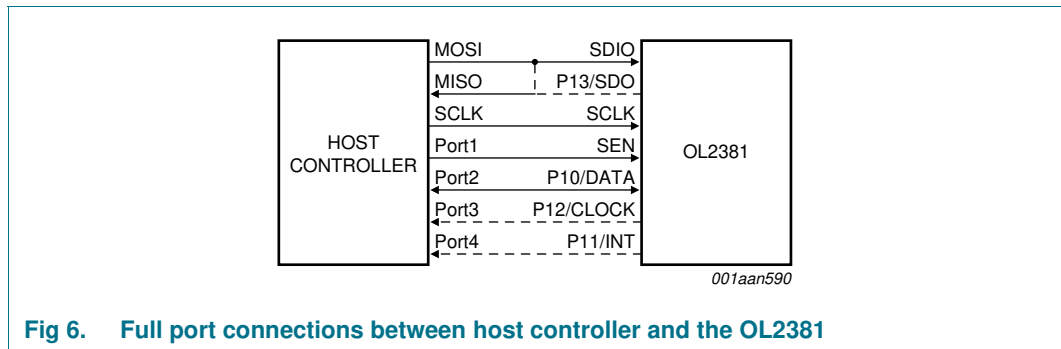


Fig 6. Full port connections between host controller and the OL2381

7.4 Special ports

7.4.1 TEN

The test enable input (pin TEN) must always be connected to GND. This pin is only required for a factory test and has no user-operable functionality.

7.4.2 TEST1, TEST2 and TEST3

Test pins for internal analog test-signals. In the application, these pins must be left open.

7.4.3 RSTDIS

The status of pin RSTDIS defines the polling timer state enable bit after power on. When the pin is LOW, the device is initialized with the polling timer enable bit set to 1.

7.5 General purpose ports

The device features five general purpose ports: P10 to P14, with selectable dedicated user functions; see [Section 7.8.3 “Reset and power mode register” on page 16](#). The port function is controlled by bits P1xCx. The width of these control bits for every port depends on the number of selectable signals.

All general purpose ports, except P11/INT and P12/CLOCK, are in 3-state after power-on reset. Port P11/INT is initialized as an output driving the active-LOW POR interrupt. Note that this interrupt is non-maskable.

Port P12/CLOCK is initialized to provide a 1 MHz reference clock as the default output.

7.5.1 P10/DATA

Priority of functions:

- Output signal of receiver debug interface
- RX data output, if bit SEP_RX_OUT is logic 1 and the receiver is activated

or

- TX data input when bit SEP_TX_LINES is logic 1 and the transmitter is activated

If register PORTCON2 bit SEP_TX_LINES is set and P12C[2:0] = 010b, the port delivers the TX clock as specified through register TXCON. This clock is activated after the TX command's ninth SCLK pulse and it runs until the power amplifier is turned off. This clock indicates the TX timing and informs the controller when the device samples the input data from the P10/DATA line.

If register PORTCON2 bit SEP_RX_OUT is set and if P12C[2:0] = 010b, the port delivers the RX clock associated with the data provided at P10/DATA. This clock is activated after the RX DATA command's ninth SCLK pulse. If the RX command is a PRDA, this clock is activated after successful preamble detection. In both cases the clock continues as long as the receiver state machine is in its DATA state. This clock is recovered from the RX signal timing and informs the controller when it can sample the data delivered at the P10/DATA line.

Note that in contrast to P10/DATA, where setting bit SEP_TX_LINES or bit SEP_RX_OUT overrules the normal port function, this is not the case for P12/CLOCK. The clock is only output if selected when P12C[2:0] = 010b.

Bit P10INV inverts output data, including RX data. If an inversion of TX data is desired, register TXCON's bit INV_TX_DATA must be used.

7.5.2 P11 and P12

P11 and P12 together with P10, form the serial interface when the receiver debug mode is activated; see [Section 7.41 "RX debug interface" on page 85](#).

7.5.3 P14

P14 can be used to control an external circuit, such as a TX/RX switch or an LNA.

7.6 Serial configuration interface description

7.6.1 General SPI information

The chip is configured via a three or 4 wire serial interface consisting of an 8-bit shift register and 80 × 8-bit registers holding the configuration data.

Data can be exchanged with multiple 8-bit frames (auto-incrementing) or in portions of 8 bits (1 byte), which provides an advantage when using a hardware SPI-interface. Data in the shift register is loaded into the addressed register on the last edge of SCLK within the last bit of the transferred byte.

7.6.2 SEN

A logic LOW applied to pin SEN disables the SPI interface. The internal state machine halts and every activity on pins SDIO and SCLK is ignored.

If the device is in Power-down mode, a positive edge on pin SEN activates the device. The crystal oscillator is always on, unless the device is in Power-down mode. The watchdog is cleared with a HIGH level on pin SEN; see [Section 7.11 “Watchdog” on page 25](#).

After the TX command, pin SEN has an additional function: At the falling edge of pin SEN the level on pin SDIO is latched and frozen.

7.6.3 SCLK

SCLK is the clock pin for the serial interface. Every edge of SCLK shifts data into or gets data from the SPI register-set. The second clock edge (SCLK) is used for data capturing. SDIO direction switching between input and output is accomplished with the first clock edge of the ninth bit. An additional clock edge is necessary at the start of a TX or RX command.

The clock polarity for an SPI command can be selected; see [Section 7.6.5](#).

If desired, pin SCLK can carry the baud-rate clock during a TX command and the recovered RX clock during a RX command.

7.6.4 SDIO

SDIO is the serial interface's bidirectional data input/output pin. Data in or data out operation is adapted automatically during SPI communication sequences.

If desired, pin SDIO can be used to input data if a TX command is executed or for RX data if a RX command is active.

7.6.5 General SFR access information

If SCLK is HIGH at the rising edge of SEN, the data is transferred with the rising edge of SCLK; see [Figure 7](#) and [Figure 8](#). If SCLK is LOW at the rising edge of SEN, the data is transferred at the falling edge of SCLK.

For continuity, all figures and examples in this data sheet assume SEN is LOW at the rising edge of SCLK, unless otherwise stated. The first edge of SCLK is referred to as the rising edge and the second as the falling edge.

7.7 Write and read access to SFR

7.7.1 Write access to SFR

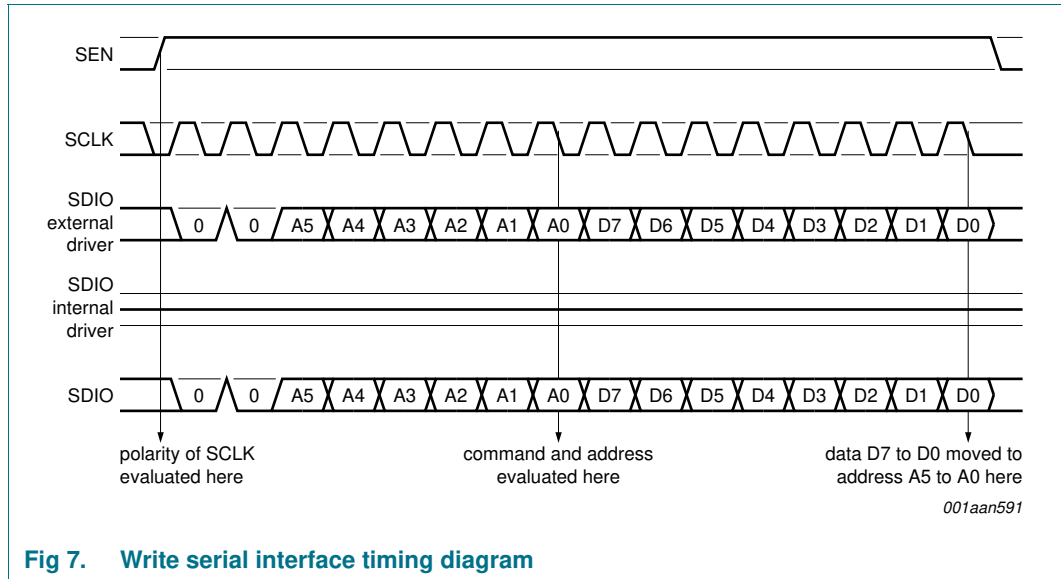


Fig 7. Write serial interface timing diagram

7.7.2 Read access to SFR

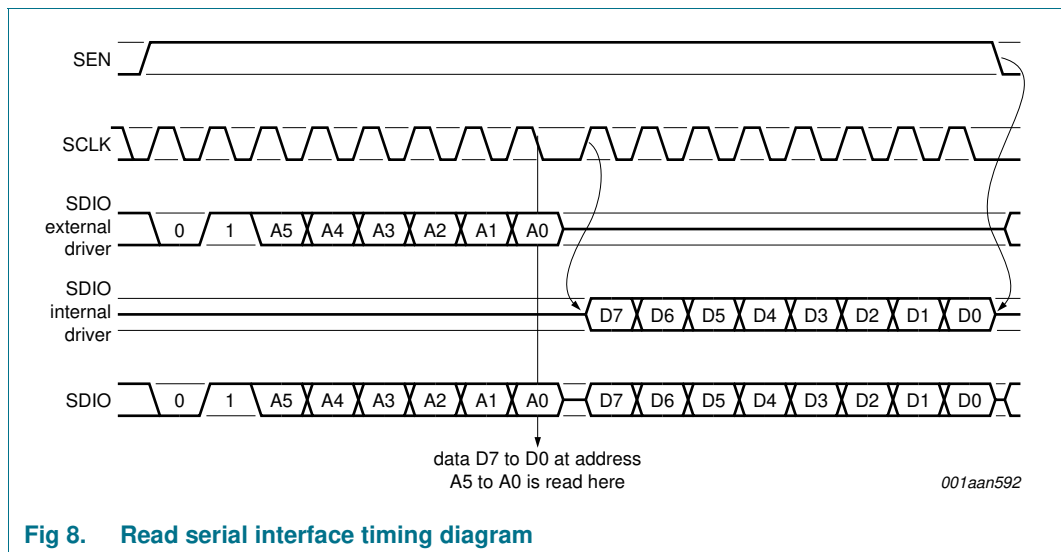


Fig 8. Read serial interface timing diagram

7.7.3 Separation of SDI and SDO line

A four-wire SPI interface can be implemented using pin SDIO for MOSI and pin P13/SDO for MISO. Timing and output control of pin SDO is the same as for the internal SDIO driver.

7.7.4 Read access to SFR with separate SDO line

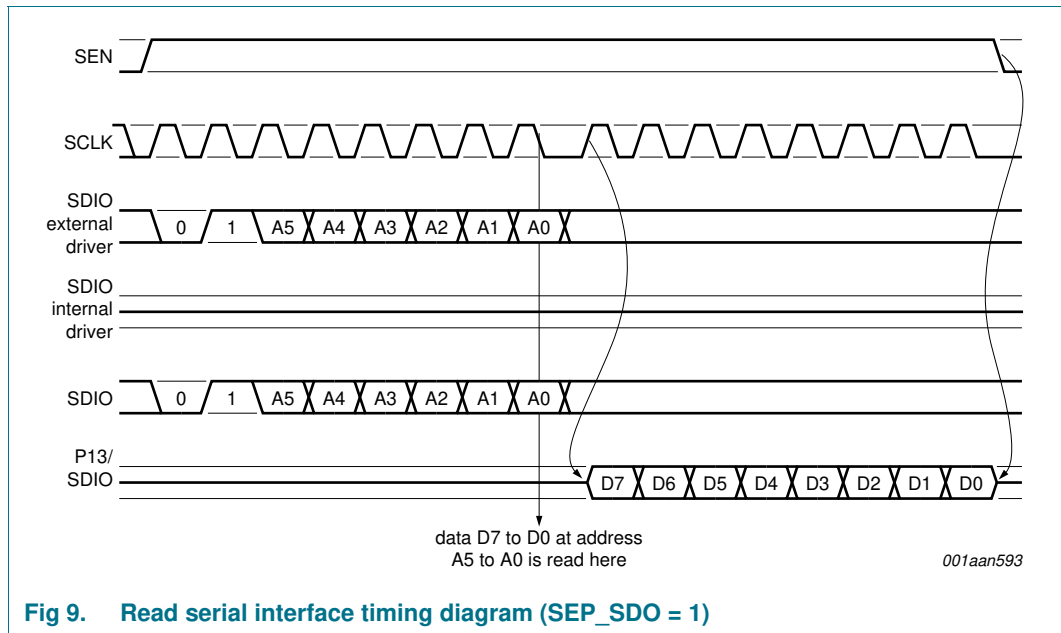


Fig 9. Read serial interface timing diagram (SEP_SDO = 1)

7.7.5 Read and write access to SFR with auto-increment function

If the SPI clock (SCLK) is still applied after the first 8 data bits are transferred, the auto-increment function automatically increments the address by one for the following 8 data bits. This enables data to be written to a continuous range of bytes without having to set the address for every single data-byte. The auto-increment function is terminated on the falling edge of SEN.

If the address reaches the end of the address range (3Fh) an additional increment causes the address to start at 00h again. This wrap around is accomplished in the current address bank. The auto-increment function has no influence on the bank selection.

7.7.6 Write access to SFR with auto-increment function

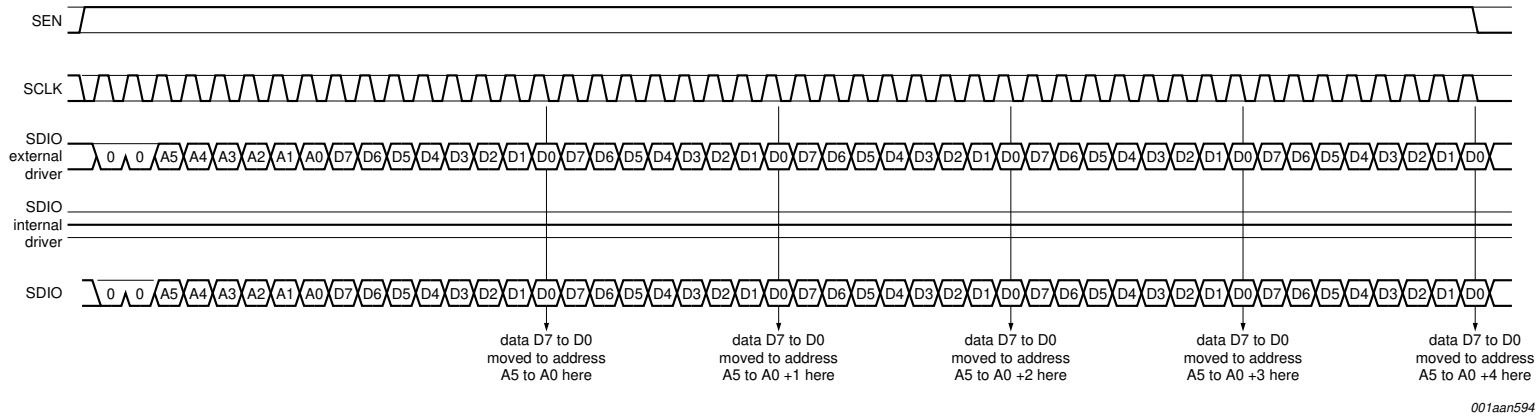


Fig 10. Write serial interface auto-increment timing diagram

SEN must be forced LOW after registers are written to indicate end of write. [Figure 10](#) is an example showing 5 successive bytes stored.

7.7.7 Read access to SFR with auto-increment function

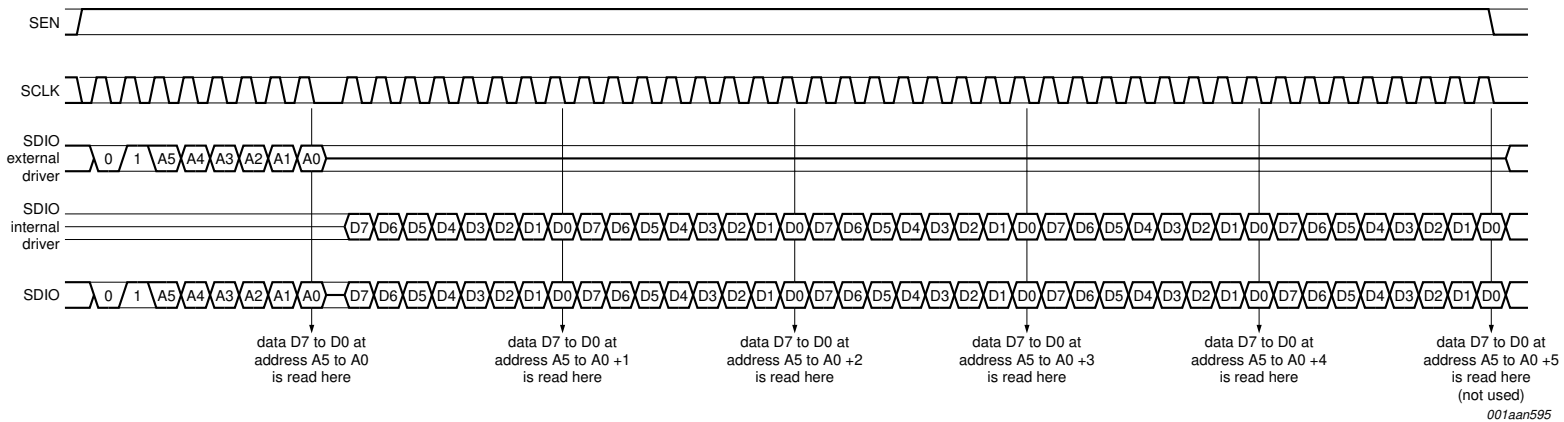


Fig 11. Read serial interface auto-increment timing diagram (SEP_SDO = 0)

SEN must be forced LOW after registers are read to indicate end of read. [Figure 11](#) is an example showing 5 successive bytes read.

7.8 Device mode description

7.8.1 Automatic start-up procedures

The device features the following automatic start-up procedures for easy device handling and configuration:

- Power-on and crystal oscillator start-up
- PLL and VCO start-up including calibration
- Preparation for TX mode
- Preparation for RX mode
- VCO auto-calibration at every center frequency change

7.8.2 General description

The automatic start-up procedures are implemented to aid the quick and easy transition between operational states. Most procedures are controlled by changing bits in the PWRMODE register. Certain configurations can be directly entered by the TX or RX commands.

7.8.3 Reset and power mode register

The PWRMODE register acts as the device's 'main power on/off/standby switch'. Setting the RESET bit of this register brings the device into the reset condition equal to the power-on reset state. This power-down state is also reached automatically at first power-on (battery insertion). If this bit is set with a write command, the effect on all registers with a reset condition is a 'hard-reset'. If, with the same SPI write command, other bits are simultaneously written to the PWRMODE register, they are changed automatically to the power-on reset state; see [Section 8.2.1.10 "General power mode register PWRMODE" on page 100](#).

7.8.3.1 First power-on reset

The non-maskable interrupt flag IF_POR is set when the initial power-on reset takes place (battery insertion).

7.8.3.2 Power-down

Setting bit PD brings the device into low current consumption standby mode. All analog receiver and transmitter circuitry including the crystal oscillator are turned off and all dynamic digital activity is stopped. Only the SPI and the polling timer, if enabled, are active. Bit PD is also under automatic device control and is set under the following conditions:

- power-on reset or setting bit RESET (setting bit RESET overrides all others)
- the watchdog timer times out

7.8.3.3 Device mode states

Three important static device internal enable signals are decoded from DEV_MODE: PLEN, TXEN and RXEN.

- PLEN is set whenever the DEV_MODE is not logic 00
- RXEN is set only if DEV_MODE is logic 10
- TXEN is set only if DEV_MODE is logic 11

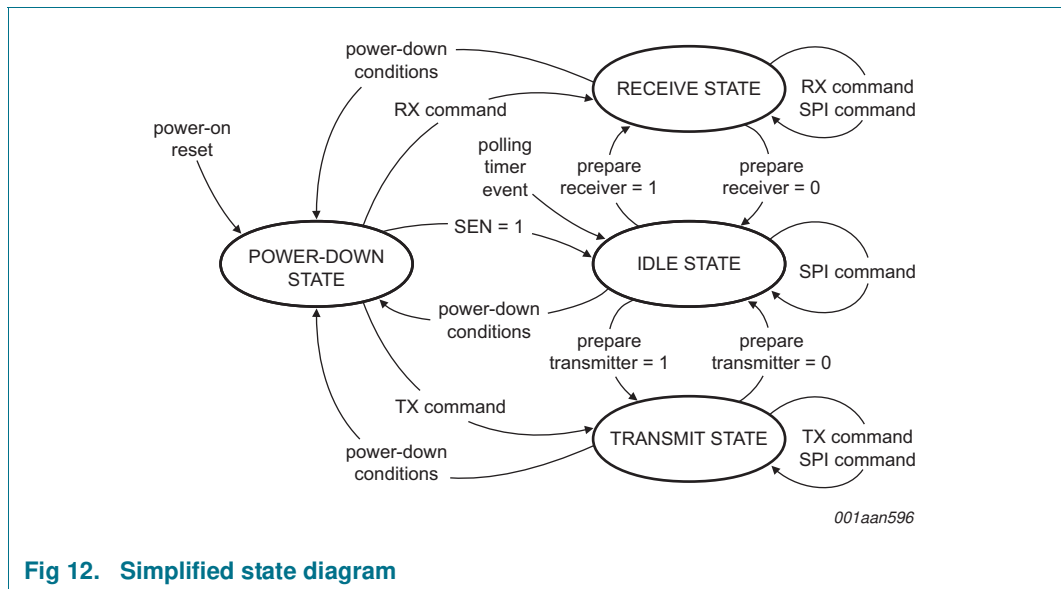


Fig 12. Simplified state diagram

An important implication of this is that a TX operation is immediately aborted if the active mode is switched to anything except TX mode, for example, switching the device into RX mode immediately shuts down the power amplifier without smoothly ramping down the RF power.

Conversely, entering TX mode immediately aborts any RX operation.

DEV_MODE bits can be either set directly by writing the PWRMODE register or by sending a RX or a TX command, where a RX command sets DEV_MODE to logic 10 and a TX command sets DEV_MODE to logic 11.

Setting bit RESET or setting bit PD (power-down) resets DEV_MODE to logic 00, where only the crystal oscillator is (potentially) enabled.

An alternative to setting the device mode can be to send a TX command and delay the '9th edge'. This sets the frequency and initiates the device as if in TX mode. The PA is then switched on at the TX command's 9th edge.

7.8.4 Flow description

The following actions are performed if the device leaves power-down state and enters active state. The internal control signals of these states are explained in more detail in later sections.

Power-down state indicator is cleared.

7.8.4.1 Digital regulator start-up

The digital voltage regulator is turned on whenever the device leaves the power-down state.

7.8.4.2 XTAL oscillator start-up

The crystal oscillator or the buffer for the external clock is turned on depending on the states of CLOCKCON register bits XODIS and EXT_CLK_BUF_EN.

Bit XO_RDY is logic 1 once the crystal oscillator has settled. The device waits for several clock periods until the clock output's frequency and duty cycle have fully settled to within the required specification. The end of this waiting period is indicated by bit REFCLK_RDY changing to logic 1. This enables the master clock gate at the root of the clock distribution tree and if applicable, the reference clock for the digital section is enabled. A polling timer recalibration is also initiated at this point.

7.8.4.3 PLL start-up

This sequence is controlled by the internal control signal PLEN. The voltage regulators for the PLL and VCO (REG_VCO_ON, REG_PLL_ON) are turned on.

Wait until the voltage regulators have settled. This sequence ends, if LO_PWR_RDY = 1.

7.8.4.4 Turn on VCO

The phase frequency detector (PFD_ON), prescaler (PRESC_ON), clock for the PLL (CLK_PLL_ON) and PLL lock detection are turned on with the next clock cycle.

7.8.4.5 Perform VCO calibration

This sequence is complete once the PLL is locked (LO_RDY is set). A manual VCO calibration immediately stops any TX or RX command.

7.8.4.6 Preparation for TX mode

This mechanism is invoked by issuing device mode logic 11 (prepare for TX) or by sending a TX command.

The voltage regulator for the power amplifier (bit REG_PA_ON) and the VCO clock divider for transmitter path (bit TXON) are enabled.

This sequence ends if the power amplifier's regulator started properly (brown-out detection not active).

7.8.4.7 Preparation for RX mode

This mechanism is invoked by issuing device mode logic 10 (prepare for RX) or by sending a RX command.

The bandgap reference circuit for the receiver section (bit RX_GAP_ON), VCO clock divider for the receiver section (bit PLL_LOCK), reference clock for the RX path (bit CLK_RXA_ON), and the analog section of receiver (bit RXA_ON) are enabled.

7.8.4.8 Perform channel filter calibration

The channel filter calibration is performed every time the device enters RX mode. This sequence ends if the channel filter calibration ends.

7.8.5 Changing device modes

Intermediate device modes may be required in an operation sequence e.g. start digital regulator and XTAL to initialize/change SFR contents or to re-trim the polling timer. This can be carried out by changing the corresponding registers. However, the direct

commands may be more useful if the only operation required is the entering of TX or RX mode. The corresponding sequences start automatically and operation enabled after all internal settling times are met.

7.8.6 Interrupts

The OL2381 can generate various interrupts which can be enabled by the IEN register and read from the IFLAG register; see [Section 8.2.1.11 “Interrupt enable register IEN” on page 101](#). The IFLAG register is always cleared after it is read. Certain pins can also be configured to present these interrupts; see [Section 7.3 “Interface description” on page 9](#).

7.9 Power supply and reset

Each main functional block is equipped with its own dedicated supply voltage pin. Therefore, several supply pins are available on the package and all must be connected. Note that all ground connections of these functional blocks are bonded to the exposed die pad of the package (metal plate underneath the die). Some blocks are supplied via dedicated integrated low-dropout voltage-regulators. Note that for all regulators the output voltage is available both internally and externally on a pin for connection of a decoupling capacitor. The following blocks have regulated supplies.

Table 3. Blocks with regulated supplies

Block	Regulator supply pin	Pin to decouple
PLL	VCC_REG	VREG_PLL
VCO	VCC_REG	VREG_VCO
PA	VCC_PA	VREG_PA
digital	VCC_DIG	VREG_DIG

7.9.1 Voltage regulators operation

All regulators are operated automatically by selecting the corresponding device modes. The device modes are set by DEV_MODE[1:0] in register PWRMODE; for details see [Section 7.8.3 “Reset and power mode register” on page 16](#).

The regulators can also be independently controlled by the control bits located inside the TEST registers. Individual operation of the voltage regulators can be necessary for debug or measurement purposes. The following paragraphs describe each individual regulator and its purpose.

7.9.2 Digital regulator

Before the device can be operated, the digital regulator must be switched on. In standby state (power-down state) the digital regulator is bypassed and supplies the digital section with a low supply voltage to guarantee data retention in the configuration registers. If the digital regulator is switched on, the voltage reaches its stabilized value of approximately 1.8 V. The digital regulator can be activated or deactivated by bit REG_DIG_DIS in TEST1 register. Clearing the bit enables the regulator, depending on the selected device mode. Setting the bit always disables the regulator.

7.9.3 PLL regulator

To start any PLL operation the PLL regulator must be switched on. This happens automatically with operation of bit REG_PLL_ON in the TEST2 register.

Remark: this bit only starts the PLL regulator, all PLL functional blocks are enabled individually by separate control-bits.

7.9.4 VCO regulator

For stability and immunity reasons the VCO is supplied via an independent voltage regulator. This regulator can be manually controlled via bit REG_VCO_ON in the TEST2 register.

Remark: this bit only starts the VCO regulator. VCO operation is enabled individually by a separate control-bit.

7.9.5 PA regulator

This regulator is enabled if PA operation is desired. This can be manually controlled by setting bit REG_PA_ON.

Remark: this bit only starts the PA regulator. TX operation must be enabled by setting the corresponding command on the SPI interface.

7.9.6 Device reset

A device reset occurs whenever the supply voltage is applied on the VCC pins (battery insertion). The device utilizes two power-on detection mechanisms, one digital and one analog. These reset circuits constantly monitor the supply voltage. Setting bit RESET in the PWRMODE register performs the same operation by software. This is equivalent to a power-on reset. If bit RESET is set via a command, it is cleared automatically when SPI signal SEN goes LOW after the next write register command.

7.10 Main control and timing blocks

7.10.1 Crystal oscillator

7.10.1.1 Circuit description

The crystal oscillator is the source of the reference clock for the PLL, the digital section and the mixed signal blocks in the receiver chain. The crystal oscillator circuit diagram is shown in [Figure 13](#).

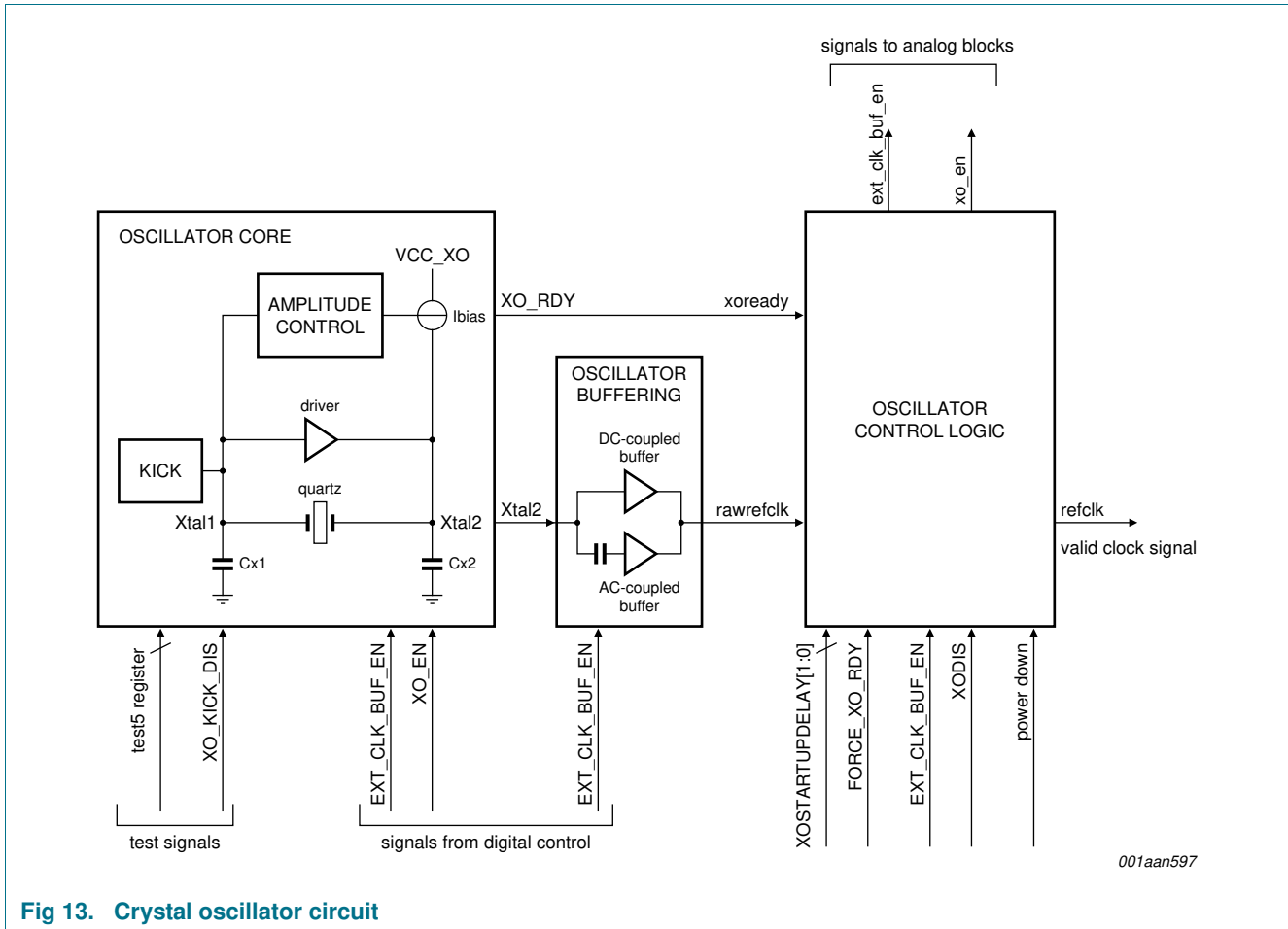


Fig 13. Crystal oscillator circuit

The crystal oscillator consists of three main blocks: the oscillator core, the oscillator buffer and the oscillator control logic.

The oscillator core is a low power quartz based Pierce oscillator. The oscillation frequency is defined by the quartz and the tuning capacitors CX1 and CX2. The driver's low capacitance has negligible impact on the frequency value. The oscillator core is supplied by pin VCC_XO.

When the oscillation starts and the amplitude successfully detected, the amplitude control releases the signal XO_RDY to the oscillator control logic for validation. This signal indicates that the amplitude control loop has entered regulation mode and not that the oscillator has settled. An extra delay is still needed to ensure the frequency accuracy; see [Table 116 "XOSTARTUPDELAY bit functions" on page 124](#).

After start-up, the amplitude control avoids clipping and excessive driving power in the crystal unit.

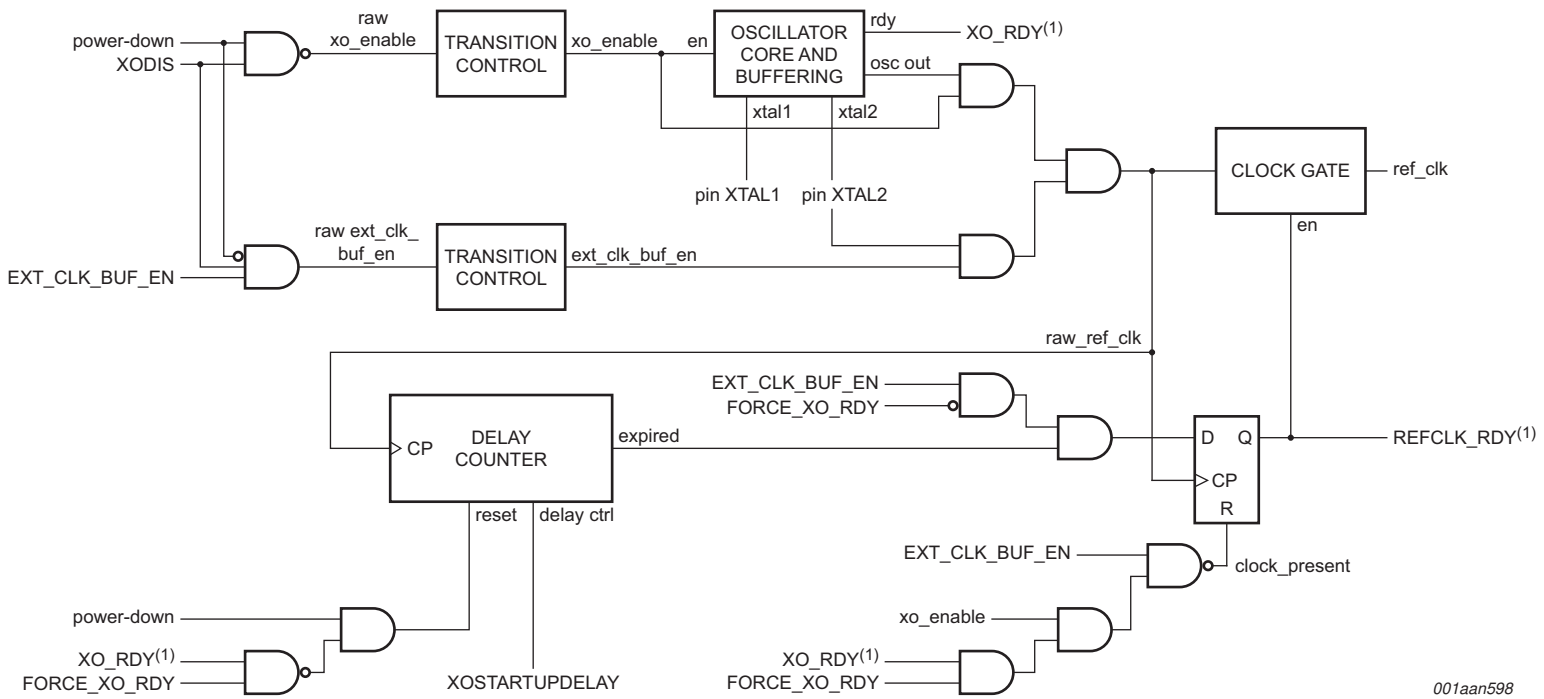
The oscillator control logic validates the oscillator signal and provide configuration facilities. The oscillator control logic is supplied by the digital regulator to the level VREG_DIG.

The oscillator buffer consists of two amplifiers connected in parallel: one low-noise AC-coupled amplifier for crystal operation and one high-input voltage DC-coupled amplifier for testing purposes only. The buffer plays the role of level-shifter for the signals in PLL and digital supply domains. The buffer circuitry is supplied by the PLL and digital regulators accordingly.

Alternatively, an external clock signal can be applied at pin XTAL2; see the external clock buffer description in [Section 7.10.2 “Oscillator control and control bits” on page 23](#). The applied signal must comply with the logic levels in the digital core (0 V for LOW and 1.8 V for HIGH). With the OL2381 properly configured, the DC-coupled amplifier replaces the low-noise AC-coupled amplifier. This provides the possibility to skip the internal oscillator's start-up sequence and also allows the customer to stop the clock sequence for test purposes.

Remark: The use of an external clock signal requires special care in the hardware configuration. The oscillator core circuitry connected to pin XTAL2 cannot withstand levels higher than 2.8 V. Therefore, the use of this test mode with supply voltages higher than 2.8 V requires a hardware modification for pin VCC_XO. The recommended solution is to connect pin VCC_XO to pin VREG_DIG. In that configuration the circuit's integrity is ensured but the digital noise needs to be considered.

The crystal oscillator is always active either in oscillator mode or in external clock buffer mode when the device is not in Power-down state.



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(1) Denote internal and official status signals.

Fig 14. Diagram for crystal oscillator with clock selection circuitry

7.10.2 Oscillator control and control bits

The oscillator control logic is described in [Figure 14](#). Upper case signal names denote control bits in the OL2381's register set. Upper case signal names labeled '(1)' denote (internal and 'official') status signals. Lower case signal names denote internal signals.

The enable logic is visible at the top left corner for both modes: the crystal oscillator mode and the external clock buffer mode. The crystal oscillator is turned on when both, `power-down` and `XODIS`, are false. The transition control ensures that no glitches can be generated when turning the oscillator on and off. The external clock buffer is turned on when the device is not in power-down mode and both control bits, `XODIS` and `EXT_CLK_BUF_EN` are set; see [Section 8.2.1.15 "Clock connection register CLOCKCON" on page 103](#). As a consequence, putting the device in power-down mode disables all clock activity, and turning the crystal oscillator on has priority over turning the external clock buffer on.

If the crystal oscillator is turned on (`XO_ENABLE` becomes true) and a crystal is connected to the oscillator, the raw clock becomes available after the oscillation reaches a significant amplitude, which is then signaled with the internal `XO_RDY` status signal. This internal status signal can be routed to pin P12/CLOCK for observation. While the crystal oscillator is disabled, it is ensured that the clock from this clock source is held at the zero level.

If the external clock buffer is activated (bit `EXT_CLK_BUF_EN` is true) the signal connected to pin XTAL2 is taken as the clock source. While the external clock buffer is disabled, it is ensured that the clock from this clock source is held at the zero level.

Since only one clock source can deliver a clock at a given time they can be easily merged. The clock is only fed into the circuit when the clock gate is enabled. The following paragraphs explain the conditions for enabling this clock gate separately for each clock source.

When using the crystal oscillator, the delay counter, in [Figure 14](#), is held in reset state during Power-down mode or if both, the internal status signal `XO_RDY` and the expert control bit `FORCE_XO_RDY`, are false. If the oscillator signals `XO_RDY` after start-up (or if the `FORCE_XO_RDY` is set), the delay counter is released from reset, which lets it count the raw clock pulses from the oscillator. Note that counting will not occur if the oscillation amplitude is too low or if the clock pulses are too 'thin' (duty cycle near 0 % or near 100 %). Therefore it is ensured that the delay counting will not start before the raw clock has a usable shape. After a programmable count ([Table 116 on page 124](#)) is reached, the counter stops and signals the end of the delay.

The digital oscillator start-up delay can be controlled by bits `XO_STARTUPDELAY[1:0]` in register `EXPERT1`.

After the delay counter's end status reaches the `REFCLK_RDY` flip-flop, (shown at the lower right corner of [Figure 14](#)), it is sampled by the raw clock, now stabilized, and this declares the reference clock ready. This also enables the clock gate which passes the clock on to the circuit starting with the following clock pulse. The `REFCLK_RDY` status flip-flop is immediately reset when the raw clock is no longer present, which happens when the crystal oscillator is turned off or bit `XO_RDY` is false due to any reason which may have stopped the oscillation.

Note that special care is needed when non-recommended crystals are used. The use of non-recommended crystals and resonators may have a negative impact on the start-up behavior, on the frequency stability and on the PLL noise performance.

The oscillation amplitude is always large enough for recommended crystals so the amplitude control can properly detect that the start-up and noise generated by the AC-coupled buffering is appropriate for PLL operation.

If the crystal is replaced by a resonator with a low Q factor, the resulting amplitude may not be large enough for the `XO_RDY` status to be properly detected, although the generated clock may still be usable. To use the OL2381 under such conditions, the `XO_RDY` status must be overridden by using the expert control bit `FORCE_XO_RDY`. Note that the delay counting mechanism will not start counting before the raw clock reaches a certain quality.

If the external clock buffer is used, it is assumed that the clock source, which is connected to pin XTAL2, provides a stable clock with a duty cycle close to 50 % at the time when bit EXT_CLK_BUF_EN is set. Therefore the delay counter is not needed in this case. But even without the delay counter, the circuit provides a well-controlled startup sequence, which is enforced by the REFCLK_RDY flip-flop and the clock gate, so that no glitches are generated when the clock buffer is turned on or off. Note that not using the delay counter in this normal case requires the FORCE_XO_RDY expert control bit to be in the cleared state.

However, if bit FORCE_XO_RDY is set when using the external clock buffer, the delay mechanism is activated. This is how the delay counter is tested in the production test but it may also help to overcome start-up problems in the external clock source. The XO_RDY, REFCLK_RDY signals can be observed for oscillator testing via the test buffer. The resulting clock can be probed at pin CLOCK.

7.11 Watchdog

The device features a watchdog timer to recover from situations when activation is not desired. The watchdog timer runs with the reference clock and it is activated, if the device is not in Power-down mode.

The watchdog is cleared and temporarily stopped under the following circumstances:

- Pin SEN is HIGH
- A terminating wakeup search is executed, i.e. either a pessimistic wakeup search is activated (bit WUPSMODE = 0) or the timer for the wakeup search is activated during an optimistic wakeup search (bit WUPSMODE = 1 and bits WUPSTIMEOUT not equal to 0).
- A terminating preamble detection is executed, i.e. the timeout for the preamble must be activated (bit EN_PREADET_TIMEOUT = 1 and bits WUPSTIMEOUT not equal to 0).

Bit EN_PREADET_TIMEOUT can be found in register SIGMON1; see [Section 8.2.2.2 “Signal monitoring control register SIGMON1” on page 115](#). Bit WUPSMODE can be found in register SIGMON0; see [Section 8.2.2.1 “Signal monitoring register SIGMON0” on page 114](#). Bits WUPSTIMEOUT can be found in register WUPSTO; see [Section 8.2.2.4 “Register WUPSTO” on page 116](#).

The watchdog timeout can be adjusted according to [Equation 1](#).

$$\text{watchdogtimeout} = \frac{2^{15} + \text{WUPSTIMEOUT}}{\text{CLK}_{REF}} \quad (1)$$

where:

$\text{CLK}_{REF} = 16 \text{ MHz}$

watchdogtimeout = desired watchdog timeout

It is not possible to turn off the watchdog completely. The watchdog can be disabled for an arbitrary period only if pin SEN is set HIGH.