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OL2385

Industrial RF transceiver

Rev. 1.0 — 15 June 2016

Product data sheet
COMPANY PUBLIC

1. General information

1.1 General description

The device is a fully integrated single-chip transceiver intended for use in an industrial environment.

The device incorporates several commonly used building blocks including a crystal stabilized oscillator, a fractional-N based Phase Locked Loop (PLL) for accurate frequency selection in both TX and RX, Low Noise Amplifier (LNA), attenuator for Automatic Gain Control (AGC), I/Q down-mixer and two high resolution Analog to Digital Converters (ADC).The conversion into the digital domain is done in an early phase, enabling a software defined radio like approach.

By transforming signals in the digital domain in an early phase, one highly configurable RX channel is available including channel mixer, channel filter, ASK/FSK demodulator, clock-data recovery, bit processor and a micro-controller memory interface (DMA) allowing the micro-controller to complete the data handling and handshaking.

The device has an embedded RISC micro-controller optimized for high performance and low power as well as an EROM for customer applications. The device also includes a medium power UHF transmit system with a high dynamic range of -35dBm to +14dBm which makes it ideal for the use in narrow band communication systems. The TX system allows transmission with data rates up to 400 kbit/s NRZ.

Power ramping and splatter avoidance filters are included to ensure that the transmit spectrum fulfills all the common standards in Europe, USA and Asia. The phase noise of the transmitter supports ARIB operation.

The device includes a series of timers to allow for autonomous polling and wake-up applications. The TX and RX data buffers are located in the RAM with autonomous direct memory access (DMA), reducing the 'real-time' overhead for the accompanying micro-controller. The device can be interfaced via SPI, UART or LIN protocol compatible UART. Simplified programming of the device is facilitated by the HAL (Hardware Abstraction Layer).

The transceiver is configured to operate with low active and standby power consumption, ideal for battery powered applications.

2. Features and benefits

- Single IC for worldwide usage in bands between 160 MHz and 960 MHz
- Wide dynamic range with AGC to achieve excellent blocking performance
- I/Q down conversion with digital IF processing and automatic gain compensation
- Integrated I/Q phase and amplitude mismatch compensation
- Receiver path with 2 multiplexed antenna inputs enables different antenna matching
- Advanced signal monitoring and data management for fast and reliable signal detection and processing
- High dynamic range RSSI measurement
- Programmable PA with digitally controlled power ramping and shaping
- Operation up to 400 kbit/s 4FSK for high data rate applications
- RX and TX data buffer in RAM with independent DMA channels
- Integrated temperature sensor for crystal temperature drift compensation
- Support of high accuracy external temperature sensor for ARIB systems
- Integrated 16-bit extended micro RISC kernel for system on chip solutions with up to 32 kByte EROM
- 10 independent DMA channels for powerful data transfer and configuration
- Integrated copy machine for fast data transfer
- Coprocessor for bit manipulation and code redundancy cycle calculation (CRC)
- Several timers for firmware development including 3 general purpose timers, 3 RX channel timers, low power mode polling timer and watch dog timer
- Clock driver for micro controller crystal sharing
- Controlled via SPI, UART, LIN compatible UART
- 10 bit ADC sensor interface with up to 100 kSps sampling rate
- Tool chain (compiler, assembler, linker, debugger) with in circuit debug capability
- API available to simplify custom firmware development
- IREC evaluation and demonstration kit available for basic RF operation
- Remote control protocol (RCP) to operate RF without custom firmware via SPI/UART

3. Applications

The IC supports the following system applications:

- Smart Metering (sub-GHz Zigbee, wireless M-bus)
- Home and building security and automation (KNX-RF)
- Remote control devices
- Wireless medical applications
- Wireless sensor network
- Industrial monitoring and control
- Low Power Wide Area networks (SigFox)

4. Quick reference data

Table 1. Quick reference data

	Parameter	Conditions	Min	Typ	Max	Unit
1	General					
1.1	UHF Carrier Frequency		158		960	MHz
1.2	Power Down Current			700		nA
1.3	Supply Voltage		1.9		5.5	V
1.4	Operating Temperature		-40		+85	°C
2	Transmitter					
2.1	Supply Current	XTAL		0.25		mA
		Tx @ 0 dBm		9		mA
		Tx @ 14dBm		29		mA
2.2	Max Output Power		14			dBm
2.3	Phase Noise @ 100 kHz Offset	169 MHz band		-120		dBc/Hz
		434 MHz band		-117		dBc/Hz
		868 MHz band		-109		dBc/Hz
		925 MHz band		-108		dBc/Hz
3	Receiver					
3.1	Supply Current	@ 45 kHz BW		11		mA
		@ 10 kHz BW		11		mA
3.2	Data Rate				400	kbit/s
3.3	Sensitivity	ASK/OOK @ 10 kHz BW		-123		dBm
3.3.1		FSK @ 50 kHz BW		-112		dBm
3.3.2		FSK @ 10 kHz BW		-124		dBm
3.5	Adjacent channel rejection	868 MHz		>50		dB
3.6	Image channel rejection (calibrated)			60		dB
3.7	Channel Filter Band Width		4		360	kHz
3.8	RSSI	Dynamic Range @ 10kHz BW	120			dB
3.10		Variation	-3		3	dB
4	Micro-controller					
4.1	EROM				32	kByte
4.2	Customer RAM				7	kByte

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
OL2385AHN/00100[1]	HVQFN48	Plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm; terminal pitch 0.5 mm; wettable flanks	SOT619-13
OL2385AHN/001A0[2]	HVQFN48	Plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm; terminal pitch 0.5 mm; wettable flanks	SOT619-13
OL2385AHN/001B0[3]	HVQFN48	Plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm; terminal pitch 0.5 mm; wettable flanks	SOT619-13
OL2385AHN/001C0[4]	HVQFN48	Plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm; terminal pitch 0.5 mm; wettable flanks	SOT619-13

[1] Generic version without preflashed software

[2] SigFox software stack preflashed

[3] WMBus 2013 software stack preflashed

[4] sub-GHz ZigBee MAC layer software stack preflashed

6. Marking

Table 3. Marking information

Line	Example	Description
A	OL2385	2385 = Type number
B	*******	ID: *****xx (* = Diffusion lot number + x = Assembly ID); In case the number of digits exceeds 7, ID is truncated by sequentially removing positions from left to right.
C	ZSDyww*	Z = Manufacturer Code SSMC S = Assembly Centre Kaohsiung D = RoHS2006 yww = Date Code (Y = year, W = calendar week) * = Release Status X = customer engineering sample (CES) Y = customer qualification sample (CQS) _ = released samples (RFS)
D	2385ABrrff	2385 = Type number A = std version B = BOM version rr = Rom Code version ff = SW version

7. Block diagram

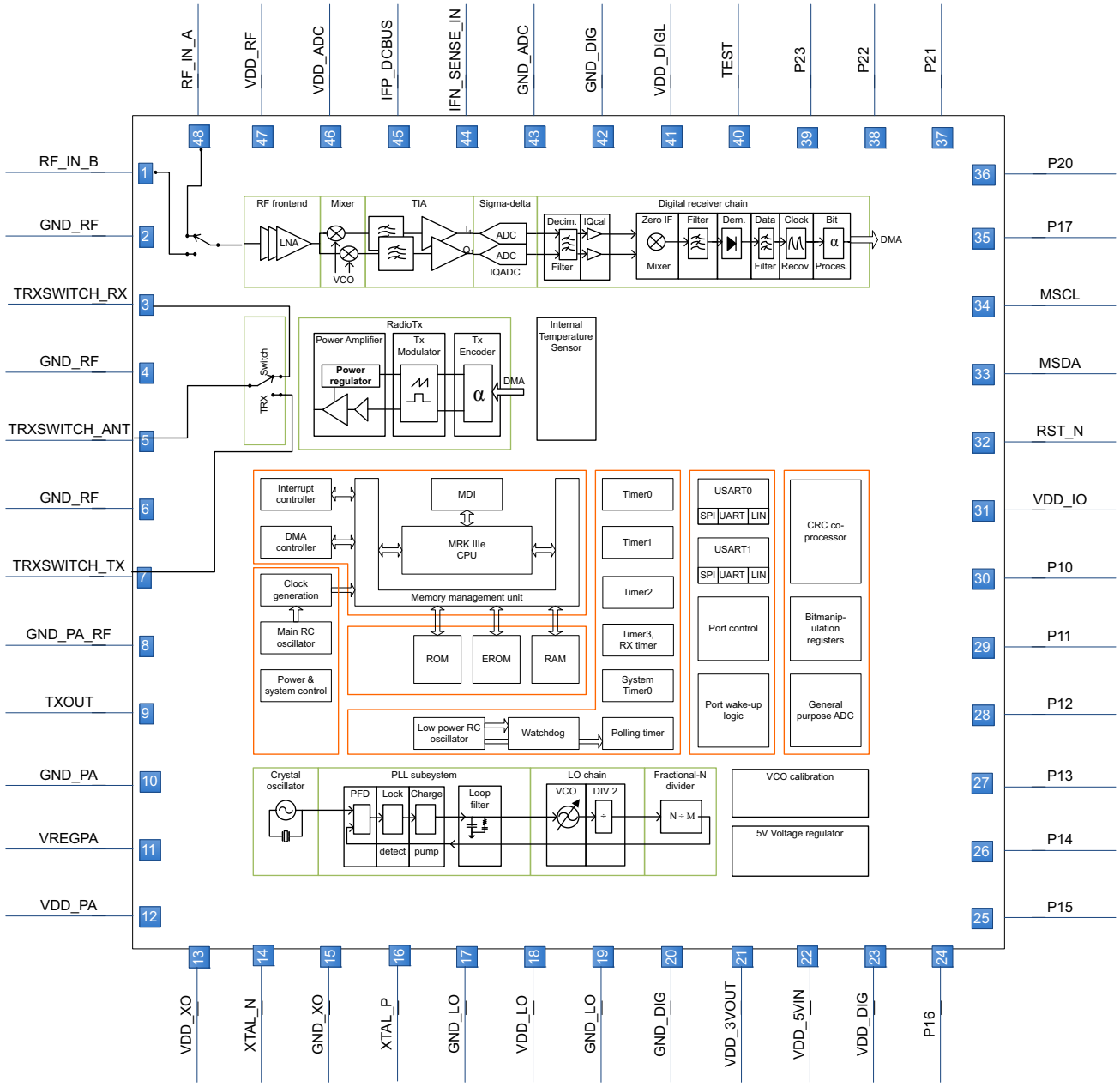

Fig 1. Block diagram

8. Pinning information

The circuit is packaged in a HVQFN48 with wettable flanks.

8.1 Pinning

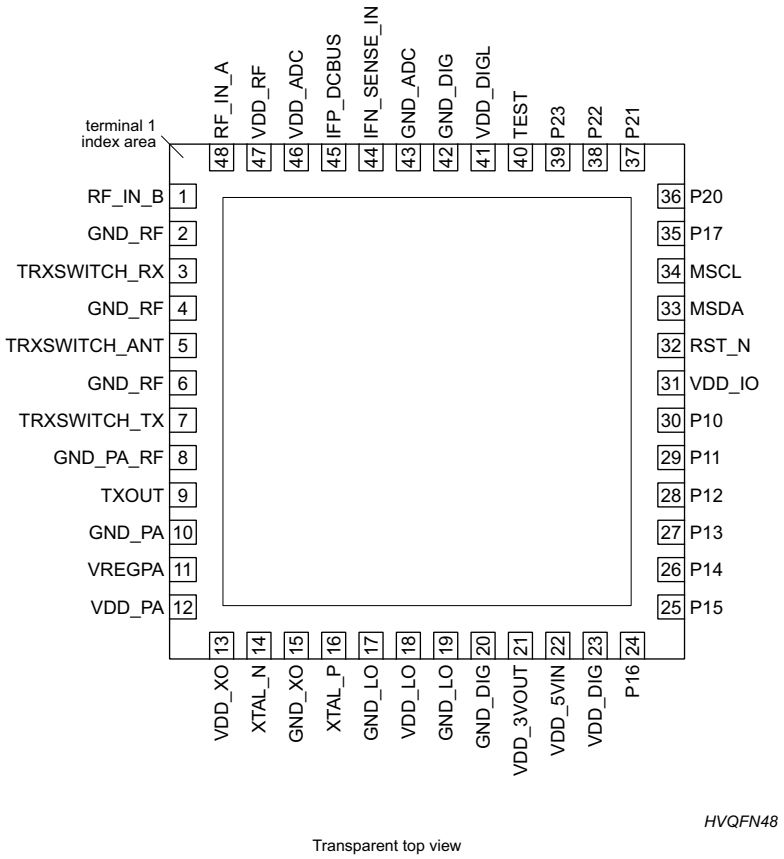

Fig 2. Pinout HVQFN48

8.1.1 Pin 1 keep out area

For the purpose of package orientation, so called "pin 1" identification is included. This can either be as an additional small pin / pad as shown in design 1 (left) of Figure 3, or a notch in the die pad as shown in design 2 (right) of Figure 3.

Note that the pin 1 identifier is electrically connected to the ground plate.

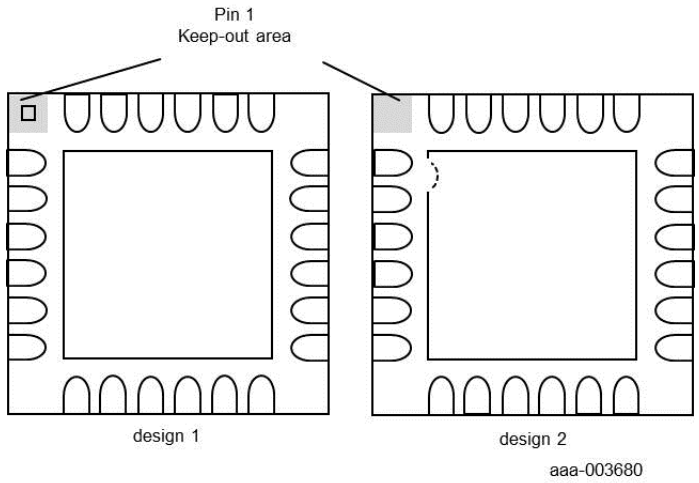

Fig 3. Pin 1 keep out area

8.2 Pin description

Table 4. Pinning description

Symbol	Pin	Description
RF_IN_B	1	RF receiver input B (internally multiplexed with RF receiver input A)
GND_RF [6]	2	Ground
TRXSWITCH_RX	3	TRX switch (interface to RX part)
GND_RF [6]	4	Ground
TRXSWITCH_ANT	5	TRX switch (interface to antenna)
GND_RF [2][6]	6	Ground - connected to exposed die pad area
TRXSWITCH_TX	7	TRX switch (interface to TX part)
GND_PA_RF	8	Ground
TXOUT [7]	9	Power amplifier output
GND_PA	10	Ground
VREGPA	11	Regulated power amplifier supply, requires external choke to TXOUT
VDD_PA	12	Power supply for PA block in transmit path
VDD_XO	13	Power supply for crystal oscillator
XTAL_N	14	Crystal oscillator input
GND_XO	15	Ground
XTAL_P	16	Crystal oscillator output
GND_LO	17	Ground
VDD_LO	18	Power supply for local oscillator
GND_LO	19	Ground
GND_DIG	20	Ground (digital)
VDD_3VOUT	21	3 V output voltage of the 5 V to 3 V LDO
VDD_5VIN	22	5 V input voltage of the 5 V to 3 V LDO
VDD_DIG	23	Power supply for digital part
P16	24	GPIO, wake-up, USART0, USART1

Table 4. Pinning description

Symbol	Pin	Description
P15	25	GPIO, timer input, timer output, USART0, USART1
P14	26	GPIO, timer output, USART0, USART1
P13	27	GPIO, USART0
P12	28	GPIO, wake-up, timer input, USART0, USART1
P11	29	GPIO, fail safe wake-up, timer input, USART0, USART1
P10	30	GPIO, fail safe wake-up, timer output, RX and TX clock output
VDD_IO	31	Power supply for digital I/Os
RST_N [8]	32	Reset input (active low), internal pull-up resistor
MSDA [9]	33	Monitor and debug interface serial data (input/output; internal pull-up in input mode)
MSCL [10]	34	Monitor and debug interface serial clock (output)
P17	35	GPIO, wake-up, timer input, timer output, RX data output, TX data input, USART0, USART1
P20	36	GPIO, wake-up, timer output, USART1
P21	37	GPIO, GP ADC input NEG
P22	38	GPIO, wake-up, GP ADC input POS, timer output
P23	39	GPIO, wake-up, GP ADC reference voltage, USART1
TEST [1]	40	Test pin (must be connected to ground in the application)
VDD_DIGL [3][4][5]	41	LDO output voltage
GND_DIG	42	Ground (digital)
GND_ADC	43	Ground
IFN_SENSE_IN	44	Selectable ADC negative input / pin used for test purposes
IFP_DCBUS	45	Selectable ADC positive input / pin used for test purposes
VDD_ADC	46	Power supply for ADC in receiver chain
VDD_RF	47	Power supply for receive path
RF_IN_A	48	RF receiver input A (internally multiplexed with RF receiver input B)

[1] Pin TEST must be connected to ground in the application.

[2] The exposed die pad area must be connected to ground.

[3] VDD_DIGL is the internal supply of the digital part and shall only be externally connected to a blocking capacitor 15 nF (nominal).

[4] VDD_DIGL must neither be pulled to high voltages nor to GND

[5] Do not use VDD_DIGL to supply external devices

[6] All GND_RF are connected internally

[7] TXOUT is not to be supplied externally except for an inductor connected to VREGPA

[8] RST_N shall be connected only with a 4.7 kΩ resistor in series.

[9] MSDA features an on-chip pull-up resistor to VDD_IO and may be left open or terminated to VDD_IO, as desired.

[10] MSCL is an output and shall be unconnected in the application.

9. Design information

9.1 Introduction

The device can be used in many applications where the flexibility of the micro-controller in combination with the dedicated receive and transmit hardware are exploited. The range of applications of such a device span from simple transmitter applications triggered by a key press to complex half duplex RF multi protocol transceivers. In order to describe the wealth of features and possibilities it is necessary to describe more detailed the key functional blocks of the device. Functions, such as power management and wake-up procedures (where the micro-controller is not controlling the process directly), permeate the complete device and are described in the coming sections. The main functions are the micro-controller subsystem, including the frequency generation system (the core of all RF functionality), the transmitter system and the receiver systems.

9.2 Power management

9.2.1 Modes of operation

The device supports operation in a 3 V, 5 V or a mixed 3 V and 5 V environment supporting the following supply use cases:

1. Device and digital interface supplied with regulated 5 V supply
   - Digital signaling between all devices in the system is done at 5 V level.
2. Device and digital interface supplied with regulated 3 V (3.3 V) supply
   - Digital signaling between all devices in the system is done at 3 V (3.3 V) level.
3. Device supplied with regulated 3 V (3.3 V) supply and digital interface supplied with regulated 5 V supply
   - Digital signaling between all devices in the system is done at 5 V level.
4. Device and digital interface supplied with a single primary lithium battery cell (3.6 V … 1.9 V)
   - Digital signaling between all devices in the system is done at the unregulated battery voltage level.
5. Supply with a single rechargeable battery cell (4.2 V … 3.0 V) and an accompanied voltage regulator (3.6 V … 2.5 V)
   - Device is supplied with the regulated voltage.
   - Digital signaling between all devices in the system is done at the unregulated battery voltage level.

Connection diagrams for these different use cases are depicted in Figure 4.

9.2.2 External power supply domains

Several power supply pins are present to provide the required supply isolation between various RF, analogue and digital blocks (external power supply domains). The power supply pins have to be directly connected to a regulator output or a battery. External supply switches are not required.

Adequate blocking capacitors have to be connected to the external supply pins.

Table 5. External power supply domains

Power supply pin	Voltage range	Description
VDD_IO, GND_IO	3 V, 5 V	Main power supply domain of the device; supplies the I/O port pins, the power-on reset circuit and an internal low-power regulator which supplies the power state logic, the I/O port control latches, the polling timer and the watchdog.
VDD_LO, GND_LO	3 V	Power supply for the local oscillator (fractional-N PLL).
VDD_XO, GND_XO	3 V	Power supply for the crystal oscillator.
VDD_RF, GND_RF	3 V	Power supply for the radio frontend including the LNA, the input attenuators and the mixer for receive mode.
VDD_PA, GND_PA	3 V	Power supply for the power amplifier regulator output and the power amplifier control for transmit mode.
VDD_ADC, GND_ADC	3 V	Power supply for the sigma-delta ADCs in the radio receiver.

Table 5. External power supply domains

Power supply pin	Voltage range	Description
VDD_DIG, GND_DIG	3 V	Power supply for the digital part.
VDD_5VIN	5 V	Supply voltage input for the internal power regulator. This regulator generates the required supply voltage for the device's VDD supply pins in the 3 V domains.
VDD_3VOUT	3 V	Regulated supply voltage output of the internal power regulator.

[1] Voltage ranges are given here only for information purpose. Please refer to the electrical characteristics for detailed voltage range specification.

The external power supply domains with the associated power supply pins are briefly described in the Table 5.

The package HVQFN has an exposed die pad at the back which is intended as heat sink and additional ground connection.

The device includes an internal power regulator which can be used to generate a voltage less than 3.6 V when such a voltage is not available. This regulator utilizes the two supply pins VDD_5VIN and VDD_3VOUT. The regulator is only on if the device is in power supply state ACTIVE. In all other power supply states the regulator is off. VDD_5VIN can be supplied permanently and the input voltage must be greater than 3.6 V.

The application has to ensure that the current drawn from the internal power regulator does not exceed the maximum limit given in the section electrical characteristics. If this limit is exceeded all supply voltage pins in the 3 V domain must be connected to an external voltage regulator. It is not allowed to supply parts of the device with the internal and other ones with an external 3 V supply.

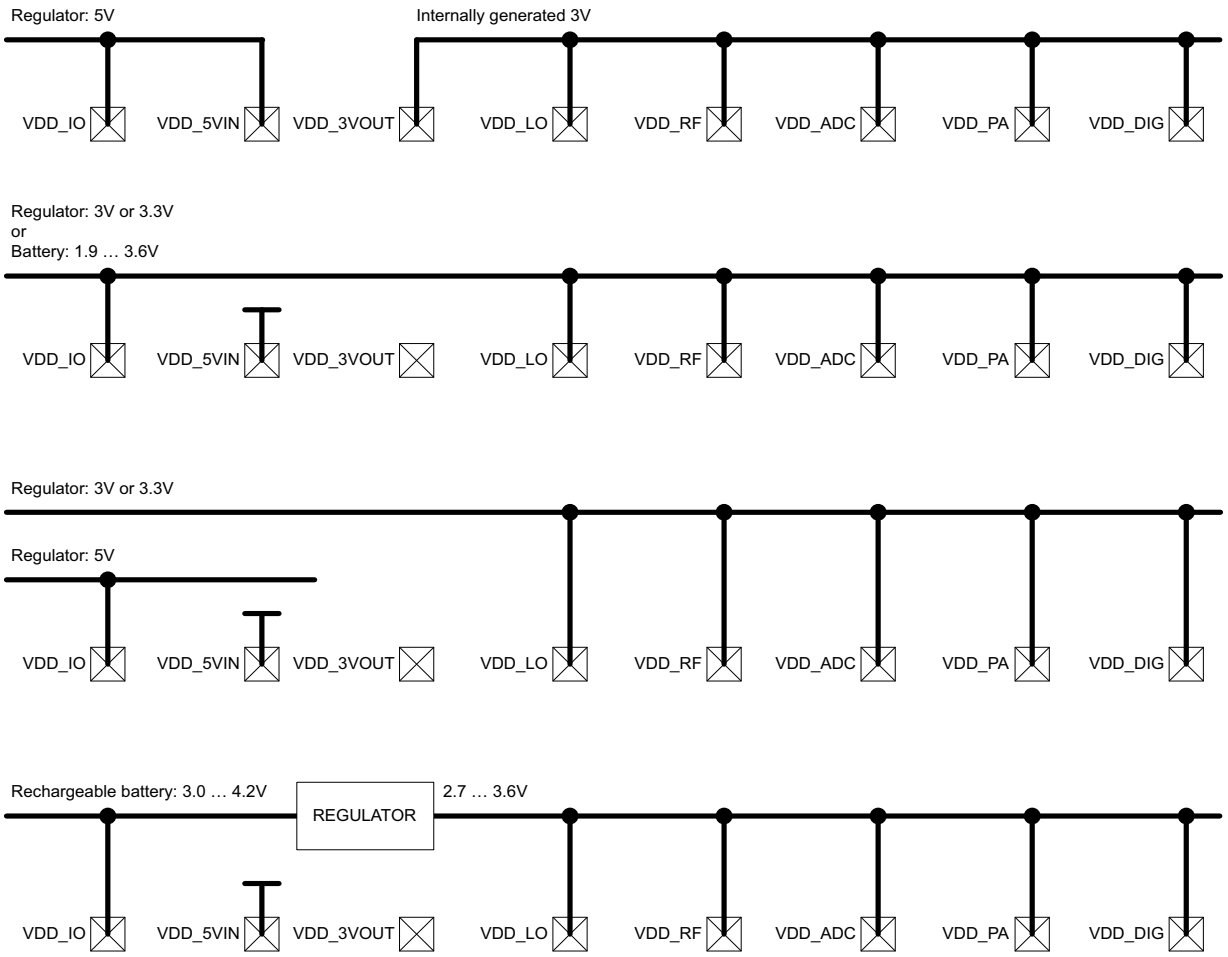

Fig 4. Connection of external power supply domains for different power supply use cases

9.2.3 Recommended external capacitors in the supply domains

- The device is supplied by an external supply with 3 V or 3.3 V:
  - Pin 21 VDD_3VOUT: open, not connected
  - Pin 22 VDD_5VIN: connected to GND
  - Pin 31 VDD_IO: 10 nF (±20 %) capacitor
  - Pin 41 VDD_DIGL: 15 nF (±20 %) capacitor (mandatory)
  - Pin 47 VDD_RF: 10 nF (±20 %) capacitor
  - Pin 12 VDD_PA: 10 nF (±20 %) capacitor
  - Pin 23 VDD_DIG: 10 nF (±20 %) capacitor
  - Pin 18 VDD_LO: 22 nF (±20 %) capacitor
  - Pin 13 VDD_XO: 68 nF (±20 %) capacitor
  - Pin 46 VDD_ADC: 10 nF (±20 %) capacitor

- The device is supplied by an external supply with 5V and the internal 5V to 3V regulator is used:
  - Pin 21 VDD_3VOUT: 10nF capacitor (±20%)
  - Pin 22 VDD_5VIN: connected to external 5 V supply, 100nF (±20%) capacitor plus optional 2.2µF capacitor
  - Pin 31 VDD_IO: 10nF (±20%) capacitor
  - Pin 41 VDD_DIGL: 15nF (±20%) capacitor (mandatory)
  - Pin 47 VDD_RF: 10nF (±20%) capacitor
  - Pin 12 VDD_PA: 10nF (±20%) capacitor
  - Pin 23 VDD_DIG: 10nF (±20%) capacitor
  - Pin 18 VDD_LO: 22nF (±20%) capacitor
  - Pin 13 VDD_XO: 68nF (±20%) capacitor
  - Pin 46 VDD_ADC: 10nF (±20%) capacitor

9.2.4 Power supply states

The device supports four different power states:

- RESET state
- POWER-OFF state
- ACTIVE state
- STANDBY state

The state diagram for the functional power supply states is given in Figure 5:

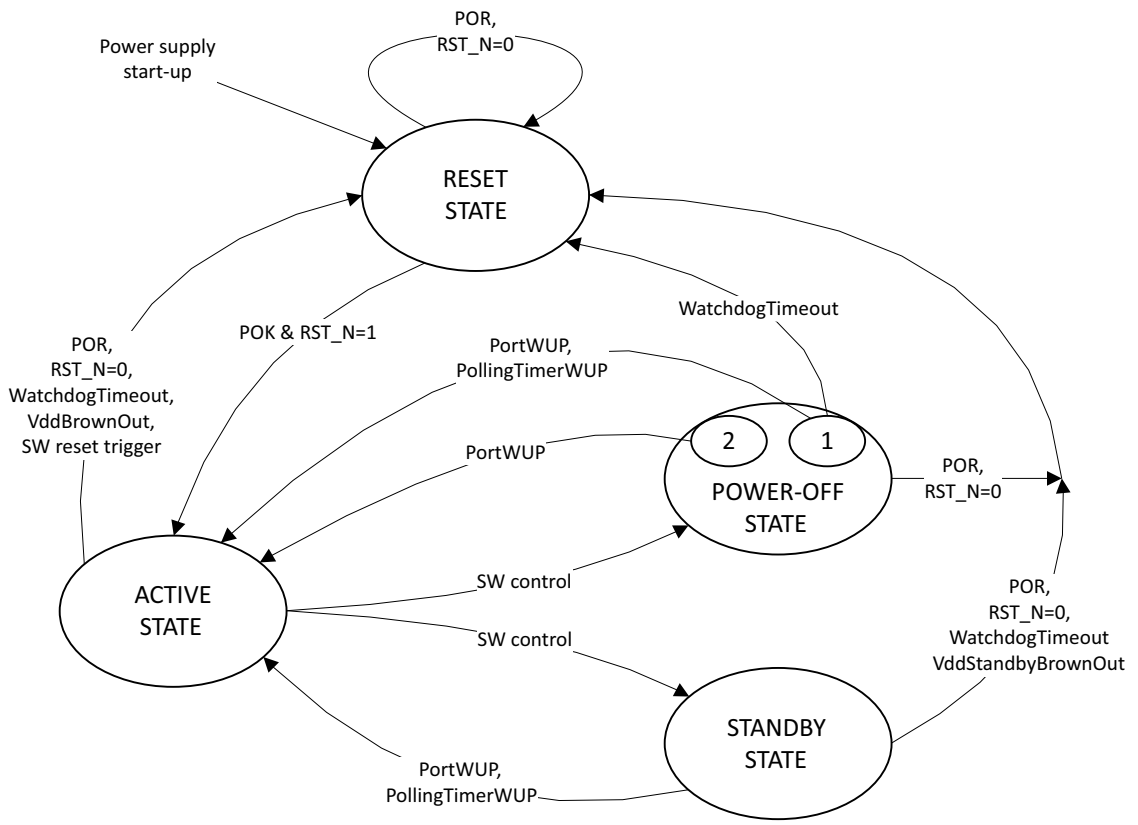

Fig 5. Power supply state diagram

9.3 Local oscillator

The radio frequencies needed for reception and transmission are created using a local oscillator. The signals for the reference namely crystal oscillator, mixer signals and the mixer phases for both transmission and reception are generated here. The purity, stability and matching of these signals define the maximum performance that can be achieved by the RF system; therefore the blocks are optimized for these performance parameters. The choice of the architecture of the Fractional-N_PLL and that of the voltage controlled oscillator (VCO) guarantees highest performance and flexibility with the minimum of current consumption.

The transmission of FSK is achieved by modulation of the PLL and therefore the loop filter supports a high bandwidth to allow data rates up to 400kbit/s.

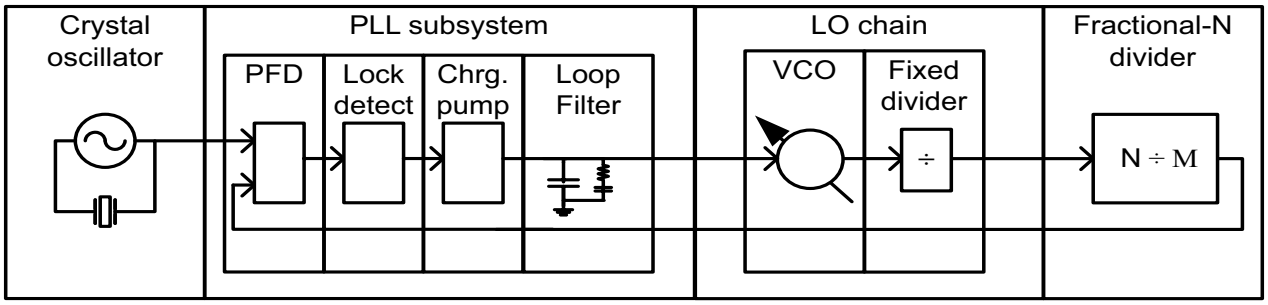

Fig 6. Local Oscillator

9.4 UHF transmitter subsystem

9.4.1 General description

The UHF transmitter consists of a modulator block for narrow band FSK and ASK, which controls the PLL to generate the RF signal and two power amplifier blocks. A 12 dBm PA block, which is able to deliver +14 dBm output power, and a 0 dBm block to save power.

The modulation is digitally controlled, either directly to the power amplifier regulator for ASK and power ramping, or via the main LO by controlling the fractional divider to generate FSK modulation in the LO.

- TX Modulator for ASK and FSK
- High current regulator with fast response
- Power amplifier delivering 14dBm max.
- Power amplifier switchable to deliver 0dBm max.
- Power can be regulated in 0.25dB steps

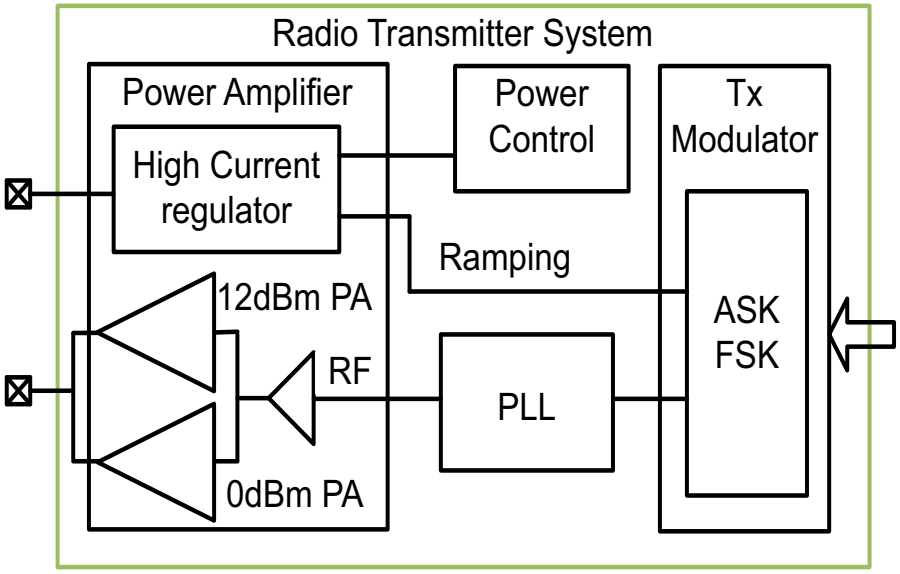

Fig 7. Radio transmitter system

9.4.2 TRX switch

The TRX switch is a fully featured RF switch used to optimize the component count on the application boards. Many system require a software controlled RF switch function to select between antennas and auxiliary inputs. Although the circuit has two dedicated RF inputs the flexibility in combining the RX and TX paths after the relevant RF matching adds real benefit for the product.

9.4.2.1 Features

- 50 Ohm low loss paths from TX to Antenna
- 50 Ohm low loss path RX to antenna
- High isolation when switch is open
- Save external components

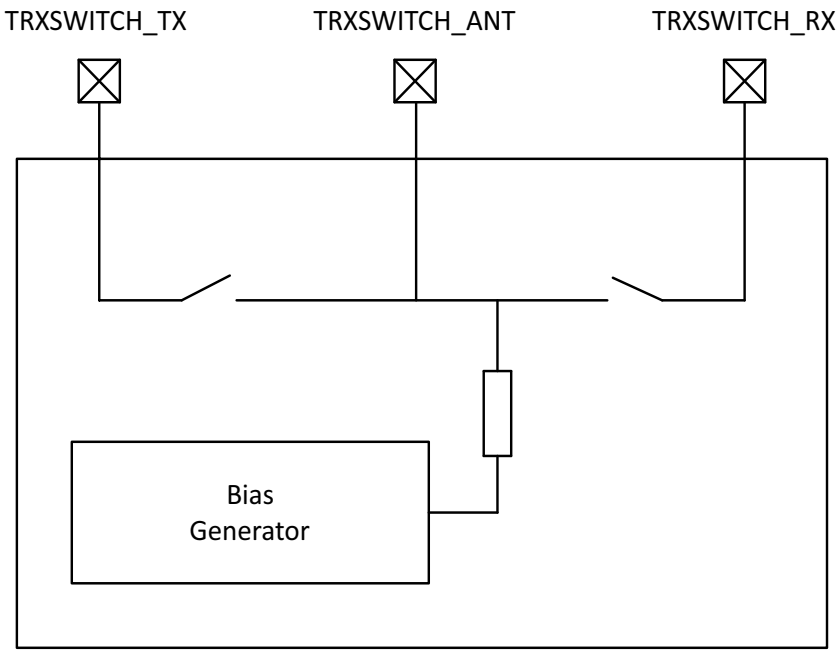

Fig 8. Transmit receive switch

9.5 UHF receiver subsystem

The UHF receiver subsystem consists of a low IF RF down conversion system. With low gain in the RF and a high resolution ADC used in the baseband to provide the necessary dynamic range. The system includes a low noise figure and high linearity LNA stage, supported by passive attenuator blocks controlled by an AGC loop. Down conversion and high gain baseband amplifiers ensure that the dynamic range of the ADC is exploited fully. The digital receiver front-end includes the preprocessing and I/Q compensation. The digital receive chain performs the channel selection, demodulation and framing. The complete system is shown in Figure 9.

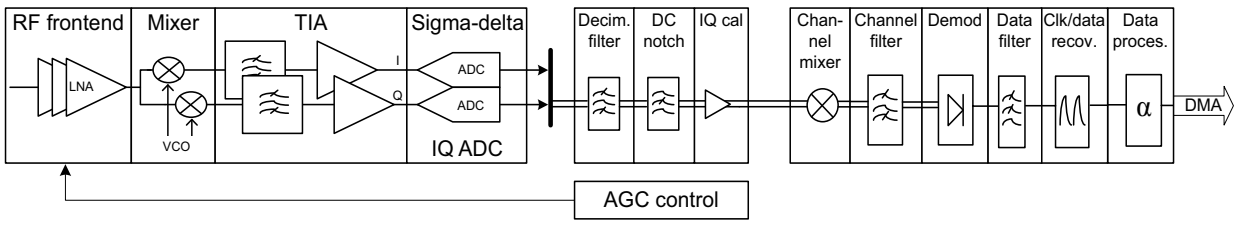

Fig 9. UHF receiver subsystem

9.5.1 Features

- RX Antenna switch with 2 inputs
- Wide band receiver for carrier frequencies in the range of 158 to 960 MHz
- Low noise figure: 5 dB typically @ 434 MHz
- Digitally controlled automatic gain control
  - 18 attenuation steps of 2 dB at RF input
  - 15 attenuation steps of 2 dB at mixer input
- IQ down conversion - high phase accuracy
- IF bandwidth with +/-400 kHz (3dB)
- RF and IF level detectors for AGC loop
- Programmable bias for amplifier stages
- DC offset correction in the baseband
- Digital IF preprocessing
- Narrow band receive chain with DMA

9.5.2 Antenna switch

In order to have the possibility to use the device at more than one frequency band or in an antenna diversity application, an integrated antenna switch is implemented.

9.5.3 LNA

The LNA is a wide-band inductor-free, highly-linear, low-power and low-noise amplifier. The LNA uses internal feedback for obtaining its high linearity and a well defined gain as well as good input matching over temperature and voltage. The LNA has a single-ended

input with a wide-band input matching optimized for 200 Ohms. A current reuse scheme is employed to maintain maximum performance with minimum current consumption. Power consumption is controllable depending on the demands of the system. The advanced feedback structure in combination with the attenuator set-up results in very low LO radiation.

9.5.4 Attenuators

Passive 2 dB step attenuators are positioned in front of the LNA and in front of the mixer in order to control the gain of the receiver. The RF inputs have integrated ESD protection and integrated AC coupling for easy application. A matching network can be applied off-chip for best performance and adaptation to different source impedances.

9.5.5 Mixer

The mixer multiplies the single-ended RF signal with a balanced quadrature (I and Q) LO signal in order to differentiate between the wanted and image channel. A special algorithm is used to remove the impact of analog mismatch on the image rejection. This usually leads to intrusion (leakage) of the image channel into the wanted channel.

9.5.6 Baseband amplifier (TIA) and DC offset compensation

The baseband amplifier stage (TIA - transimpedance amplifier) amplifies the balanced quadrature (I and Q) mixer output signals to the optimal level for the ADC and performs the anti-aliasing filtering in front of the sigma-delta ADC. Internal DC offset correction loops guarantee maximum image suppression and high linearity and dynamic range.

9.5.7 SD ADC

The SD ADC is a 1-bit higher order oversampled sigma-delta ADC with very low current consumption. The sigma delta switched time core makes use of the most modern feedback techniques to ensure stability and performance over a wide frequency band, process and temperature variation. It features fast auto-calibration for optimum performance. The calibration time is typically below 1 µs. The output is a single bit data-stream which is further processed by the digital baseband.

9.5.8 Digital receiver block diagram

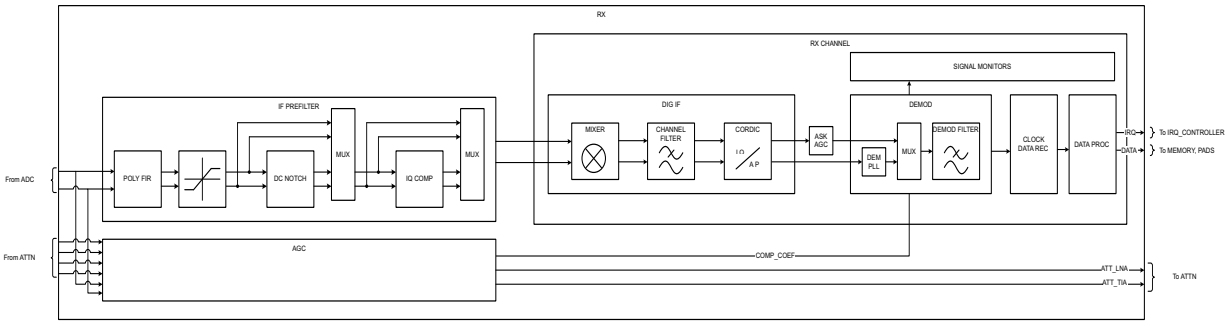

Fig 10. Digital receiver block diagram

9.5.9 Digital IF preprocessing

9.5.9.1 Features

- Decimation filter
- DC notch filter with optional bypass
- IQ mismatch compensation with optional bypass

The IF prefilter blocks perform sampling rate reduction from the highly oversampled 1-bit sigma delta bit stream into a Nyquist sampling multi bit signal. Furthermore the decimated signal is high pass filtered to remove unwanted DC components which could disturb further processing in the IQ compensation unit. The IQ compensation unit removes the unwanted image frequency components from the complex low IF signal.

9.5.9.2 Block diagram

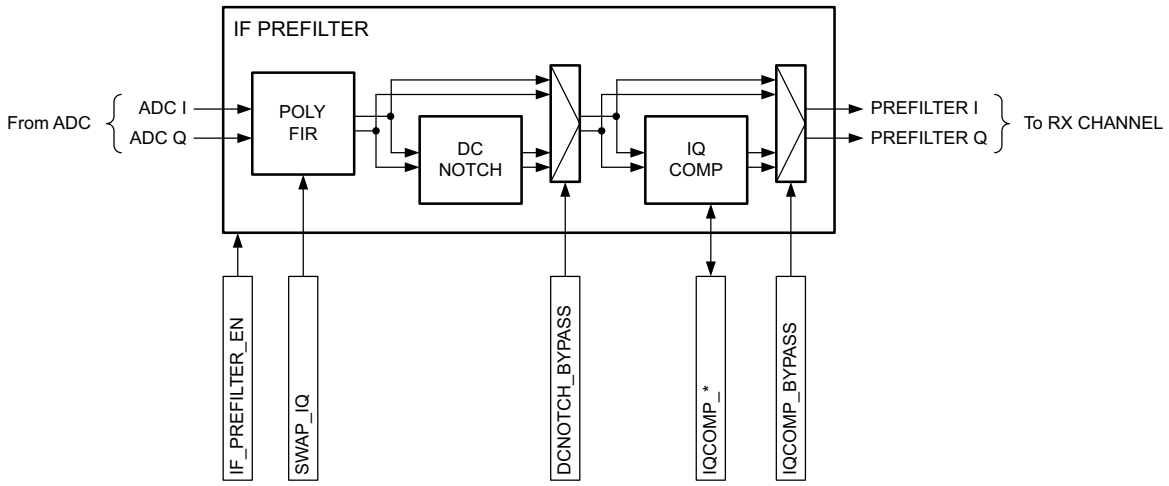

Fig 11. Digital receiver front-end

9.5.9.3 Description

The IF prefilter block has a dedicated enable bit field which allows power saving in case the receiver is not enabled at all.

Due to the tuner design, the resulting spectral view at the intermediate frequency is inverted (higher frequencies are mapped to lower and vice versa). In order to compensate that, it is possible to swap the I and Q components. If the IQ swap is enabled, the frequency order at IF is matching to the RF.

9.5.10 Automatic gain control

9.5.10.1 Features

- Highly programmable for best flexibility
- 2dB gain steps
- Automatic or manual mode

9.5.10.2 Block diagram

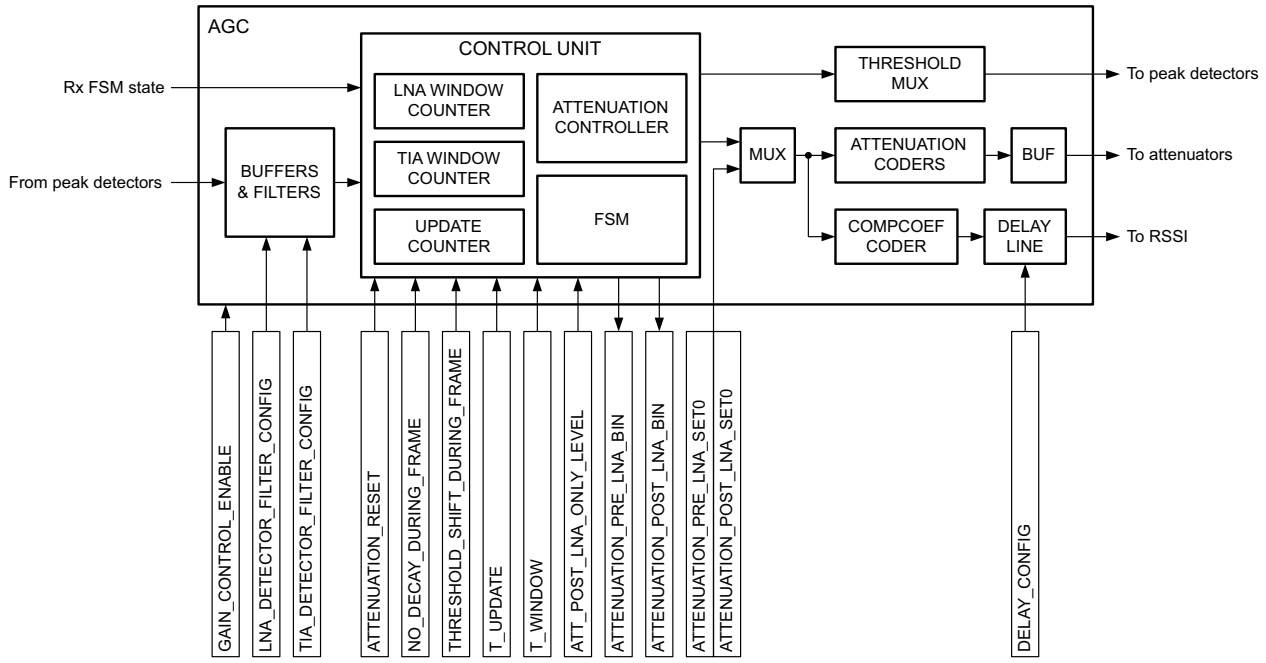

Fig 12. AGC block diagram

9.5.10.3 Description

The automatic gain control (AGC) ensures that the analog front-end is protected from high power signals and therefore ensures high linearity figures throughout the whole dynamic range of the receiver.

The AGC can work in manual or automatic gain control mode. The manual mode is intended for debugging system level use cases and for device test.

In automatic mode the AGC measures signal strength, makes a decision to get the best performance and drives the gain of the analogue front-end.

For measuring signal strength pairs of underload and overload peak detectors are present at the LNA and at the TIA. The detectors are fast-response voltage comparators checking if the signal envelope belong to the range specified by the underload and overload threshold values.

The AGC control strategy has been optimized for providing the best noise figure and maintaining all linearity requirements. Therefore the first steps of the attenuation are always done with the baseband (TIA) attenuator. The next steps are done with the

front-end (LNA) attenuator until it has reached its maximum attenuation. The remaining attenuation steps are done with the baseband attenuator again. The attenuation level at which attenuation control is given from the baseband to the front-end attenuator (takeover threshold) can be modified by software. The control strategy has been presented on the attenuation distribution figure below. It shows how the attenuation sum A_S is distributed between front-end A_{FE} and baseband A_{BB} attenuations with regards to the requested attenuation A_R.

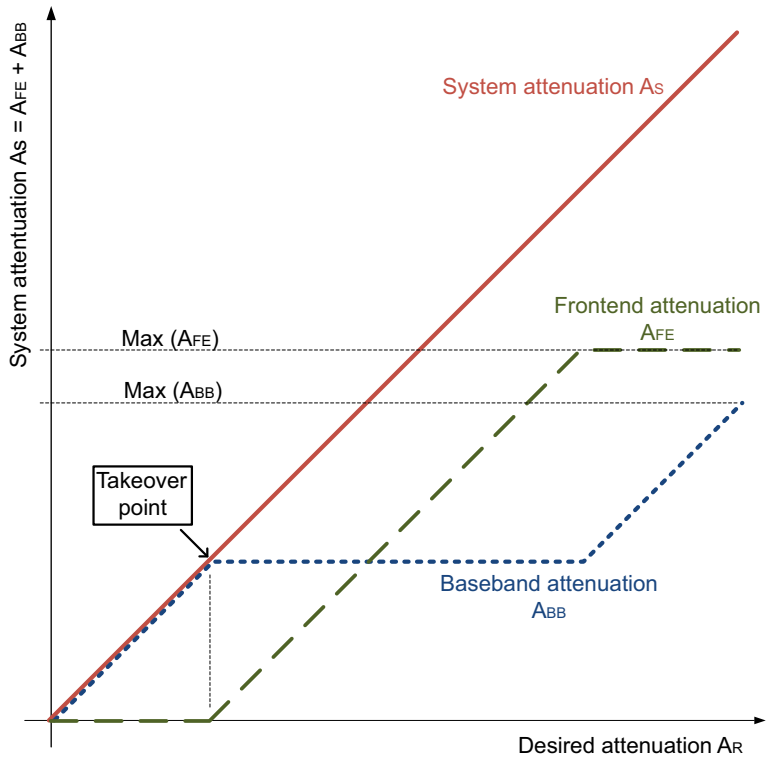

Fig 13. Attenuation Distribution