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LPC2478

Single-chip 16-bit/32-bit micro; 512 kB flash, Ethernet, CAN, LCD, USB 2.0 device/host/OTG, external memory interface

Rev. 3.1 — 16 October 2013 Product data sheet

1. General description

NXP Semiconductors designed the LPC2478 microcontroller, powered by the ARM7TDMI-S core, to be a highly integrated microcontroller for a wide range of applications that require advanced communications and high quality graphic displays. The LPC2478 microcontroller has 512 kB of on-chip high-speed flash memory. This flash memory includes a special 128-bit wide memory interface and accelerator architecture that enables the CPU to execute sequential instructions from flash memory at the maximum 72 MHz system clock rate. This feature is available only on the LPC2000 ARM microcontroller family of products. The LPC2478, with real-time debug interfaces that include both JTAG and embedded trace, can execute both 32-bit ARM and 16-bit Thumb instructions.

The LPC2478 microcontroller incorporates an LCD controller, a 10/100 Ethernet Media Access Controller (MAC), a USB full-speed Device/Host/OTG Controller with 4 kB of endpoint RAM, four UARTs, two Controller Area Network (CAN) channels, an SPI interface, two Synchronous Serial Ports (SSP), three I^2C interfaces, and an I^2S interface. Supporting this collection of serial communications interfaces are the following feature components; an on-chip 4 MHz internal oscillator, 98 kB of total RAM consisting of 64 kB of local SRAM, 16 kB SRAM for Ethernet, 16 kB SRAM for general purpose DMA, 2 kB of battery powered SRAM, and an External Memory Controller (EMC). These features make this device optimally suited for portable electronics and Point-of-Sale (POS) applications. Complementing the many serial communication controllers, versatile clocking capabilities, and memory features are various 32-bit timers, a 10-bit ADC, 10-bit DAC, two PWM units, and up to 160 fast GPIO lines. The LPC2478 connects 64 of the GPIO pins to the hardware based Vector Interrupt Controller (VIC) allowing the external inputs to generate edge-triggered interrupts. All of these features make the LPC2478 particularly suitable for industrial control and medical systems.

2. Features and benefits

- ARM7TDMI-S processor, running at up to 72 MHz.
- 512 kB on-chip flash program memory with In-System Programming (ISP) and In-Application Programming (IAP) capabilities. Flash program memory is on the ARM local bus for high performance CPU access.
- 98 kB on-chip SRAM includes:
  - 64 kB of SRAM on the ARM local bus for high performance CPU access.
  - 16 kB SRAM for Ethernet interface. Can also be used as general purpose SRAM.
  - 16 kB SRAM for general purpose DMA use also accessible by the USB.
  - 2 kB SRAM data storage powered from the Real-Time Clock (RTC) power domain.

- LCD controller, supporting both Super-Twisted Nematic (STN) and Thin-Film Transistors (TFT) displays.
  - Dedicated DMA controller.
  - Selectable display resolution (up to 1024 × 768 pixels).
  - Supports up to 24-bit true-color mode.
- Dual Advanced High-performance Bus (AHB) system allows simultaneous Ethernet DMA, USB DMA, and program execution from on-chip flash with no contention.
- EMC provides support for asynchronous static memory devices such as RAM, ROM and flash, as well as dynamic memories such as single data rate SDRAM.
- Advanced Vectored Interrupt Controller (VIC), supporting up to 32 vectored interrupts.
- General Purpose DMA (GPDMA) controller on AHB that can be used with the SSP, I^2S-bus, and SD/MMC interface as well as for memory-to-memory transfers.
- Serial Interfaces:
  - Ethernet MAC with MII/RMII interface and associated DMA controller. These functions reside on an independent AHB.
  - USB 2.0 full-speed dual port device/host/OTG controller with on-chip PHY and associated DMA controller.
  - Four UARTs with fractional baud rate generation, one with modem control I/O, one with IrDA support, all with FIFO.
  - CAN controller with two channels.
  - SPI controller.
  - Two SSP controllers, with FIFO and multi-protocol capabilities. One is an alternate for the SPI port, sharing its interrupt. SSPs can be used with the GPDMA controller.
  - Three I^2C-bus interfaces (one with open-drain and two with standard port pins).
  - I^2S (Inter-IC Sound) interface for digital audio input or output. It can be used with the GPDMA.
- Other peripherals:
  - SD/MMC memory card interface.
  - 160 General purpose I/O pins with configurable pull-up/down resistors.
  - 10-bit ADC with input multiplexing among 8 pins.
  - 10-bit DAC.
  - Four general purpose timers/counters with 8 capture inputs and 10 compare outputs. Each timer block has an external count input.
  - Two PWM/timer blocks with support for three-phase motor control. Each PWM has an external count input.
  - RTC with separate power domain. Clock source can be the RTC oscillator or the APB clock.
  - 2 kB SRAM powered from the RTC power pin, allowing data to be stored when the rest of the chip is powered off.
  - WatchDog Timer (WDT). The WDT can be clocked from the internal RC oscillator, the RTC oscillator, or the APB clock.
- Single 3.3 V power supply (3.0 V to 3.6 V).
- 4 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as the system clock.
- Four reduced power modes: idle, sleep, power-down and deep power-down.
- Four external interrupt inputs configurable as edge/level sensitive. All pins on port 0 and port 2 can be used as edge sensitive interrupt sources.

- Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, USB activity, Ethernet wake-up interrupt, CAN bus activity, port 0/2 pin interrupt).
- Two independent power domains allow fine tuning of power consumption based on needed features.
- Each peripheral has its own clock divider for further power saving. These dividers help reduce active power by 20 % to 30 %.
- Brownout detect with separate thresholds for interrupt and forced reset.
- On-chip power-on reset.
- On-chip crystal oscillator with an operating range of 1 MHz to 25 MHz.
- On-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the RTC oscillator.
- Boundary scan for simplified board testing.
- Versatile pin function selections allow more possibilities for using on-chip peripheral functions.
- Standard ARM test/debug interface for compatibility with existing tools.
- Emulation trace module supports real-time trace.

3. Applications

- Industrial control
- Medical systems
- Portable electronics
- Point-of-Sale (POS) equipment

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2478FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC2478FET208	TFBGA208	plastic thin fine-pitch ball grid array package; 208 balls; body 15 × 15 × 0.7 mm	SOT950-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash (kB)	SRAM (kB)					External bus	Ethernet	USB OTG/ OHC/ device + 4 kB FIFO	CAN channels	SD/ MMC	GP DMA	ADC channels	DAC channels	Temp range
		Local bus	Ethernet buffer	GP/USB	RTC	Total									
LPC2478FBD208	512	64	16	16	2	98	Full 32-bit	MII/RMII	yes	2	yes	yes	8	1	−40 °C to +85 °C
LPC2478FET208	512	64	16	16	2	98	Full 32-bit	MII/RMII	yes	2	yes	yes	8	1	−40 °C to +85 °C

5. Block diagram

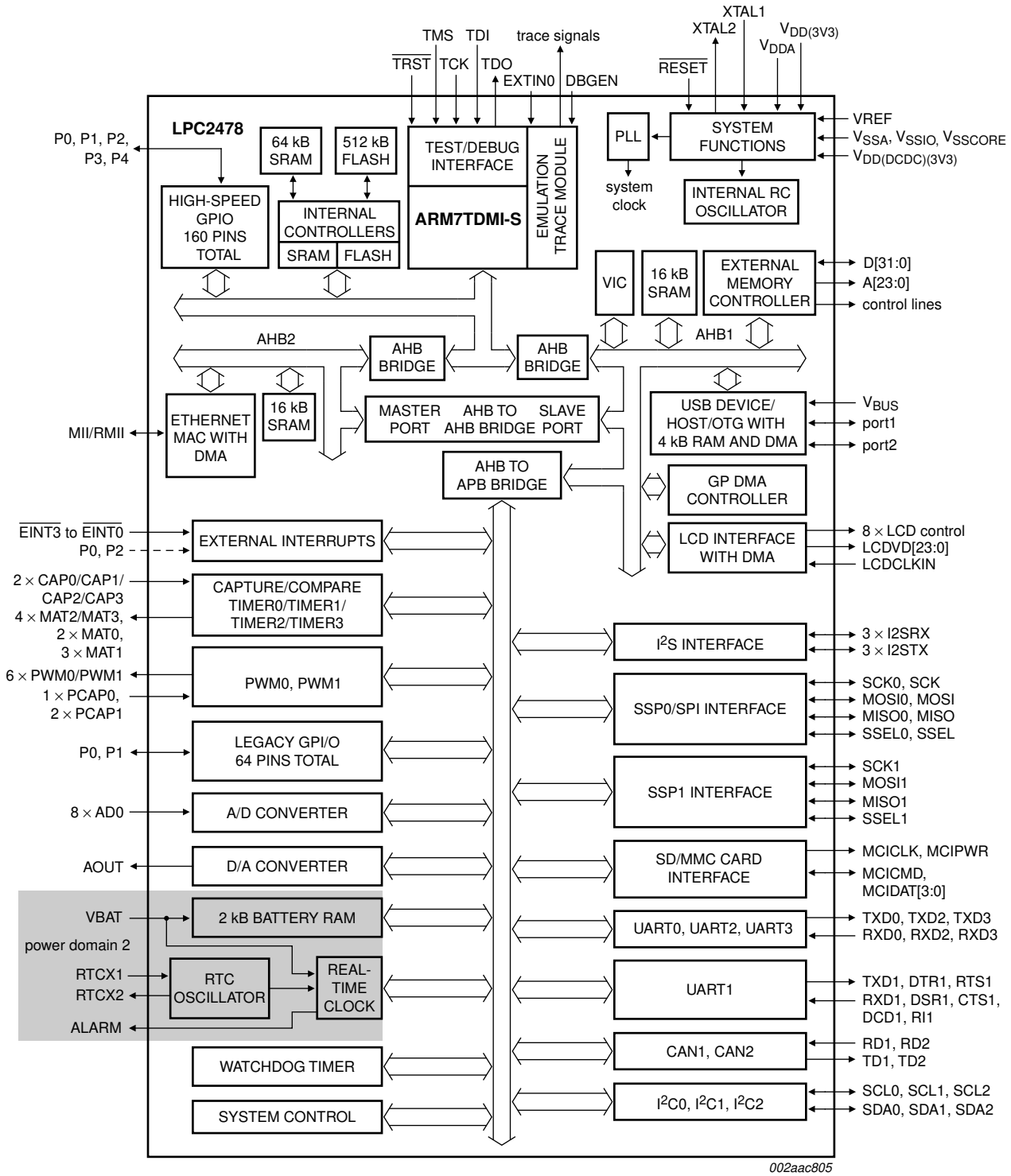


Fig 1. LPC2478 block diagram

6. Pinning information

6.1 Pinning

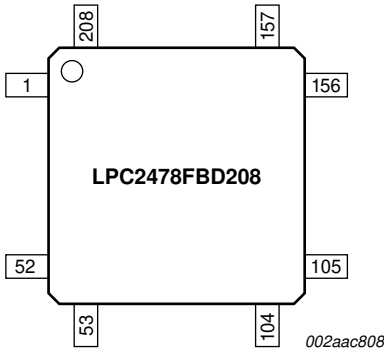
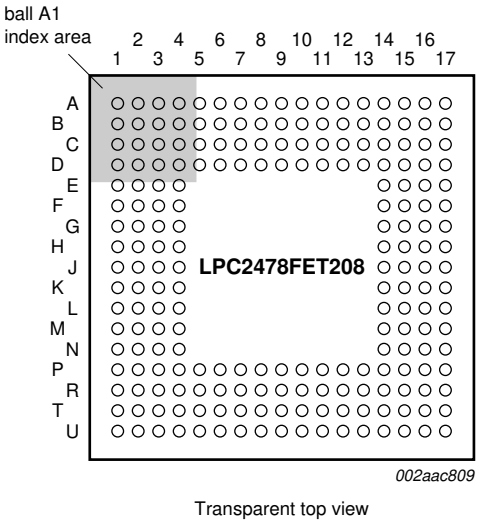


Fig 2. LPC2478 pinning LQFP208 package



Transparent top view

Fig 3. LPC2478 pinning TFBGA208 package

Table 3. Pin allocation table

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
1	P3[27]/D27/ CAP1[0]/PWM1[4]	2	V_{SSIO}	3	P1[0]/ENET_TXD0	4	P4[31]/$\overline{CS1}$
5	P1[4]/ENET_TX_EN	6	P1[9]/ENET_RXD0	7	P1[14]/ENET_RX_ER	8	P1[15]/ ENET_REF_CLK/ ENET_RX_CLK
9	P1[17]/ENET_MDIO	10	P1[3]/ENET_TXD3/ MCICMD/PWM0[2]	11	P4[15]/A15	12	V_{SSIO}

Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
13	P3[20]/D20/ PWM0[5]/DSR1	14	P1[11]/ENET_RXD2/ MCIDAT2/PWM0[6]	15	P0[8]/I2STX_WS/ LCDVD[16]/MISO1/ MAT2[2]	16	P1[12]/ENET_RXD3/ MCIDAT3/PCAP0[0]
17	P1[5]/ENET_TX_ER/ MCIPWR/PWM0[3]		-		-		-
Row B							
1	P3[2]/D2	2	P3[10]/D10	3	P3[1]/D1	4	P3[0]/D0
5	P1[1]/ENET_TXD1	6	V_{SSIO}	7	P4[30]/$\overline{CS0}$	8	P4[24]/$\overline{OE}$
9	P4[25]/$\overline{WE}$	10	P4[29]/BLS3/MAT2[1]/ LCDVD[7]/LCDVD[11]/ LCDVD[3]/RXD3	11	P1[6]/ENET_TX_CLK/ MCIDAT0/PWM0[4]	12	P0[4]/I2SRX_CLK/ LCDVD[0]/RD2/CAP2[0]
13	$V_{DD(3V3)}$	14	P3[19]/D19/ PWM0[4]/DCD1	15	P4[14]/A14	16	P4[13]/A13
17	P2[0]/PWM1[1]/TXD1/ TRACECLK/LCDPWR		-		-		-
Row C							
1	P3[13]/D13	2	TDI	3	RTCK	4	P0[2]/TXD0
5	P3[9]/D9	6	P3[22]/D22/ PCAP0[0]/RI1	7	P1[8]/ENET_CRS_DV/ ENET_CRS	8	P1[10]/ENET_RXD1
9	$V_{DD(3V3)}$	10	P3[21]/D21/ PWM0[6]/DTR1	11	P4[28]/BLS2/MAT2[0]/ LCDVD[6]/LCDVD[10]/ LCDVD[2]/TXD3	12	P0[5]/I2SRX_WS/ LCDVD[1]/TD2/CAP2[1]
13	P0[7]/I2STX_CLK/ LCDVD[9]/SCK1/ MAT2[1]	14	P0[9]/I2STX_SDA/ LCDVD[17]/MOSI1/ MAT2[3]	15	P3[18]/D18/ PWM0[3]/CTS1	16	P4[12]/A12
17	$V_{DD(3V3)}$		-		-		-
Row D							
1	$\overline{TRST}$	2	P3[28]/D28/ CAP1[1]/PWM1[5]	3	TDO	4	P3[12]/D12
5	P3[11]/D11	6	P0[3]/RXD0	7	$V_{DD(3V3)}$	8	P3[8]/D8
9	P1[2]/ENET_TXD2/ MCICLK/PWM0[1]	10	P1[16]/ENET_MDC	11	$V_{DD(DCDC)(3V3)}$	12	V_{SSCORE}
13	P0[6]/I2SRX_SDA/ LCDVD[8]/SSEL1/ MAT2[0]	14	P1[7]/ENET_COL/ MCIDAT1/PWM0[5]	15	P2[2]/PWM1[3]/CTS1/ PIPESTAT1/LCDDCLK	16	P1[13]/ENET_RX_DV
17	P2[4]/PWM1[5]/ DSR1/TRACESYNC/ LCDENAB/LCDM		-		-		-
Row E							
1	P0[26]/AD0[3]/ AOUT/RXD3	2	TCK	3	TMS	4	P3[3]/D3
14	P2[1]/PWM1[2]/RXD1/ PIPESTAT0/LCDLE	15	V_{SSIO}	16	P2[3]/PWM1[4]/DCD1/ PIPESTAT2/LCDFP	17	P2[6]/PCAP1[0]/RI1/ TRACEPKT1/ LCDVD[0]/LCDVD[4]
Row F							
1	P0[25]/AD0[2]/ I2SRX_SDA/TXD3	2	P3[4]/D4	3	P3[29]/D29/ MAT1[0]/PWM1[6]	4	DBGEN

Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
14	P4[11]/A11	15	P3[17]/D17/ PWM0[2]/RXD1	16	P2[5]/PWM1[6]/ DTR1/TRACEPKT0/ LCDLP	17	P3[16]/D16/ PWM0[1]/TXD1
Row G							
1	P3[5]/D5	2	P0[24]/AD0[1]/ I2SRX_WS/CAP3[1]	3	$V_{DD(3V3)}$	4	V_{DDA}
14	n.c.	15	P4[27]/BLS1	16	P2[7]/RD2/ RTS1/TRACEPKT2/ LCDVD[1]/LCDVD[5]	17	P4[10]/A10
Row H							
1	P0[23]/AD0[0]/ I2SRX_CLK/CAP3[0]	2	P3[14]/D14	3	P3[30]/D30/ MAT1[1]/RTS1	4	$V_{DD(DCDC)(3V3)}$
14	V_{SSIO}	15	P2[8]/TD2/TXD2/ TRACEPKT3/ LCDVD[2]/LCDVD[6]	16	P2[9]/ USB_CONNECT1/ RXD2/EXTIN0/ LCDVD[3]/LCDVD[7]	17	P4[9]/A9
Row J							
1	P3[6]/D6	2	V_{SSA}	3	P3[31]/D31/MAT1[2]	4	n.c.
14	P0[16]/RXD1/ SSEL0/SSEL	15	P4[23]/A23/ RXD2/MOSI1	16	P0[15]/TXD1/ SCK0/SCK	17	P4[8]/A8
Row K							
1	VREF	2	RTCX1	3	$\overline{\text{RSTOUT}}$	4	V_{SSCORE}
14	P4[22]/A22/ TXD2/MISO1	15	P0[18]/DCD1/ MOSI0/MOSI	16	$V_{DD(3V3)}$	17	P0[17]/CTS1/ MISO0/MISO
Row L							
1	P3[7]/D7	2	RTCX2	3	V_{SSIO}	4	P2[30]/DQMOUT2/ MAT3[2]/SDA2
14	n.c.	15	P4[26]/BLS0	16	P4[7]/A7	17	P0[19]/DSR1/ MCICLK/SDA1
Row M							
1	P3[15]/D15	2	$\overline{\text{RESET}}$	3	VBAT	4	XTAL1
14	P4[6]/A6	15	P4[21]/A21/ SCL2/SSEL1	16	P0[21]/RI1/ MCIPWR/RD1	17	P0[20]/DTR1/ MCICMD/SCL1
Row N							
1	ALARM	2	P2[31]/DQMOUT3/ MAT3[3]/SCL2	3	P2[29]/DQMOUT1	4	XTAL2
14	P2[12]/$\overline{\text{EINT2}}$/ LCDVD[4]/LCDVD[8]/ LCDVD[3]/LCDVD[18]/ MCIDAT2/I2STX_WS	15	P2[10]/$\overline{\text{EINT0}}$	16	V_{SSIO}	17	P0[22]/RTS1/ MCIDAT0/TD1
Row P							
1	P1[31]/$\overline{\text{USB\_OVRCR2}}$/ SCK1/AD0[5]	2	P1[30]/USB_PWRD2/ V_{BUS}/AD0[4]	3	P2[27]/CKEOUT3/ MAT3[1]/MOSI0	4	P2[28]/DQMOUT0
5	P2[24]/CKEOUT0	6	$V_{DD(3V3)}$	7	P1[18]/USB_UP_LED1/ PWM1[1]/CAP1[0]	8	$V_{DD(3V3)}$

Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
9	P1[23]/USB_RX_DP1/ LCDVD[9]/LCDVD[13]/ PWM1[4]/MISO0	10	V_{SSCORE}	11	$V_{DD(DCDC)(3V3)}$	12	V_{SSIO}
13	P2[15]/$\overline{CS3}$/ CAP2[1]/SCL1	14	P4[17]/A17	15	P4[18]/A18	16	P4[19]/A19
17	$V_{DD(3V3)}$		-		-		-
Row R							
1	P0[12]/$\overline{USB\_PPWR2}$/ MISO1/AD0[6]	2	P0[13]/USB_UP_LED2/ MOSI1/AD0[7]	3	P0[28]/SCL0	4	P2[25]/CKEOUT1
5	P3[24]/D24/ CAP0[1]/PWM1[1]	6	P0[30]/USB_D−1	7	P2[19]/CLKOUT1	8	P1[21]/USB_TX_DM1/ LCDVD[7]/LCDVD[11]/ PWM1[3]/SSEL0
9	V_{SSIO}	10	P1[26]/$\overline{USB\_SSPND1}$/ LCDVD[12]/LCDVD[20]/ PWM1[6]/CAP0[0]	11	P2[16]/$\overline{CAS}$	12	P2[14]/$\overline{CS2}$/CAP2[0]/ SDA1
13	P2[17]/$\overline{RAS}$	14	P0[11]/RXD2/SCL2/ MAT3[1]	15	P4[4]/A4	16	P4[5]/A5
17	P4[20]/A20/SDA2/SCK1		-		-		-
Row T							
1	P0[27]/SDA0	2	P0[31]/USB_D+2	3	P3[26]/D26/ MAT0[1]/PWM1[3]	4	P2[26]/CKEOUT2/ MAT3[0]/MISO0
5	V_{SSIO}	6	P3[23]/D23/ CAP0[0]/PCAP1[0]	7	P0[14]/$\overline{USB\_HSTEN2}$/ USB_CONNECT2/ SSEL1	8	P2[20]/$\overline{DYCS0}$
9	P1[24]/USB_RX_DM1/ LCDVD[10]/LCDVD[14]/ PWM1[5]/MOSI0	10	P1[25]/$\overline{USB\_LS1}$/ $\overline{LCDVD[11]}$/$\overline{LCDVD[15]}$/ $\overline{USB\_HSTEN1}$/MAT1[1]	11	P4[2]/A2	12	P1[27]/$\overline{USB\_INT1}$/ $\overline{LCDVD[13]}$/$\overline{LCDVD[21]}$/ $\overline{USB\_OVRCR1}$/CAP0[1]
13	P1[28]/USB_SCL1/ LCDVD[14]/LCDVD[22]/ PCAP1[0]/MAT0[0]	14	P0[1]/TD1/RXD3/SCL1	15	P0[10]/TXD2/SDA2/ MAT3[0]	16	P2[13]/$\overline{EINT3}$/ LCDVD[5]/LCDVD[9]/ LCDVD[19]/MCIDAT3/ I2STX_SDA
17	P2[11]/$\overline{EINT1}$/ LCDCLKIN/ MCIDAT1/I2STX_CLK		-		-		-
Row U							
1	USB_D−2	2	P3[25]/D25/ MAT0[0]/PWM1[2]	3	P2[18]/CLKOUT0	4	P0[29]/USB_D+1
5	P2[23]/$\overline{DYCS3}$/ CAP3[1]/SSEL0	6	$\overline{P1[19]}$/$\overline{USB\_TX\_E1}$/ $\overline{USB\_PPWR1}$/CAP1[1]	7	P1[20]/USB_TX_DP1/ LCDVD[6]/LCDVD[10]/ PWM1[2]/SCK0	8	P1[22]/USB_RCV1/ LCDVD[8]/LCDVD[12]/ USB_PWRD1/MAT1[0]
9	P4[0]/A0	10	P4[1]/A1	11	P2[21]/$\overline{DYCS1}$	12	P2[22]/$\overline{DYCS2}$/ CAP3[0]/SCK0
13	$V_{DD(3V3)}$	14	P1[29]/USB_SDA1/ LCDVD[15]/LCDVD[23]/ PCAP1[1]/MAT0[1]	15	P0[0]/RD1/TXD3/SDA1	16	P4[3]/A3
17	P4[16]/A16		-		-		-

6.2 Pin description

Table 4. Pin description

Symbol	Pin	Ball	Type	Description
P0[0] to P0[31]			I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the pin connect block.
P0[0]/RD1/TXD3/ SDA1	94[1]	U15[1]	I/O	**P0[0] —** General purpose digital input/output pin.
			I	**RD1 —** CAN1 receiver input.
			O	**TXD3 —** Transmitter output for UART3.
			I/O	**SDA1 —** I^2C1 data input/output (this is not an open-drain pin).
P0[1]/TD1/RXD3/ SCL1	96[1]	T14[1]	I/O	**P0[1] —** General purpose digital input/output pin.
			O	**TD1 —** CAN1 transmitter output.
			I	**RXD3 —** Receiver input for UART3.
			I/O	**SCL1 —** I^2C1 clock input/output (this is not an open-drain pin).
P0[2]/TXD0	202[1]	C4[1]	I/O	**P0[2] —** General purpose digital input/output pin.
			O	**TXD0 —** Transmitter output for UART0.
P0[3]/RXD0	204[1]	D6[1]	I/O	**P0[3] —** General purpose digital input/output pin.
			I	**RXD0 —** Receiver input for UART0.
P0[4]/I2SRX_CLK/ LCDVD[0]/RD2/ CAP2[0]	168[1]	B12[1]	I/O	**P0[4] —** General purpose digital input/output pin.
			I/O	**I2SRX_CLK —** I^2S Receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.[17]
			O	**LCDVD[0] —** LCD data.[17]
			I	**RD2 —** CAN2 receiver input.
			I	**CAP2[0] —** Capture input for Timer 2, channel 0.
P0[5]/I2SRX_WS/ LCDVD[1]/TD2/ CAP2[1]	166[1]	C12[1]	I/O	**P0[5] —** General purpose digital input/output pin.
			I/O	**I2SRX_WS —** I^2S Receive word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.[17]
			O	**LCDVD[1] —** LCD data.[17]
			O	**TD2 —** CAN2 transmitter output.
			I	**CAP2[1] —** Capture input for Timer 2, channel 1.
P0[6]/I2SRX_SDA/ LCDVD[8]/ SSEL1/MAT2[0]	164[1]	D13[1]	I/O	**P0[6] —** General purpose digital input/output pin.
			I/O	**I2SRX_SDA —** I^2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.[17]
			O	**LCDVD[8] —** LCD data.[17]
			I/O	**SSEL1 —** Slave Select for SSP1.
			O	**MAT2[0] —** Match output for Timer 2, channel 0.

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P0[7]/I2STX_CLK/ LCDVD[9]/SCK1/ MAT2[1]	162[1]	C13[1]	I/O	**P0[7] —** General purpose digital input/output pin.
			I/O	**I2STX_CLK —** I^2S transmit clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.[17]
			O	**LCDVD[9] —** LCD data.[17]
			I/O	**SCK1 —** Serial Clock for SSP1.
			O	**MAT2[1] —** Match output for Timer 2, channel 1.
P0[8]/I2STX_WS/ LCDVD[16]/ MISO1/MAT2[2]	160[1]	A15[1]	I/O	**P0[8] —** General purpose digital input/output pin.
			I/O	**I2STX_WS —** I^2S Transmit word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.[17]
			O	**LCDVD[16] —** LCD data.[17]
			I/O	**MISO1 —** Master In Slave Out for SSP1.
			O	**MAT2[2] —** Match output for Timer 2, channel 2.
P0[9]/I2STX_SDA/ LCDVD[17]/ MOSI1/MAT2[3]	158[1]	C14[1]	I/O	**P0[9] —** General purpose digital input/output pin.
			I/O	**I2STX_SDA —** I^2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.[17]
			O	**LCDVD[17] —** LCD data.[17]
			I/O	**MOSI1 —** Master Out Slave In for SSP1.
			O	**MAT2[3] —** Match output for Timer 2, channel 3.
P0[10]/TXD2/ SDA2/MAT3[0]	98[1]	T15[1]	I/O	**P0[10] —** General purpose digital input/output pin.
			O	**TXD2 —** Transmitter output for UART2.
			I/O	**SDA2 —** I^2C2 data input/output (this is not an open-drain pin).
			O	**MAT3[0] —** Match output for Timer 3, channel 0.
P0[11]/RXD2/ SCL2/MAT3[1]	100[1]	R14[1]	I/O	**P0[11] —** General purpose digital input/output pin.
			I	**RXD2 —** Receiver input for UART2.
			I/O	**SCL2 —** I^2C2 clock input/output (this is not an open-drain pin).
			O	**MAT3[1] —** Match output for Timer 3, channel 1.
P0[12]/ USB_PPWR2/ MISO1/AD0[6]	41[2]	R1[2]	I/O	**P0[12] —** General purpose digital input/output pin.
			O	**$\overline{\text{USB\_PPWR2}}$ —** Port Power enable signal for USB port 2.
			I/O	**MISO1 —** Master In Slave Out for SSP1.
			I	**AD0[6] —** A/D converter 0, input 6.
P0[13]/ USB_UP_LED2/ MOSI1/AD0[7]	45[2]	R2[2]	I/O	**P0[13] —** General purpose digital input/output pin.
			O	**USB_UP_LED2 —** USB port 2 GoodLink LED indicator. It is LOW when device is configured (non-control endpoints enabled), or when host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when host is enabled and detects activity on the bus.
			I/O	**MOSI1 —** Master Out Slave In for SSP1.
			I	**AD0[7] —** A/D converter 0, input 7.

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P0[14]/ USB_HSTEN2/ USB_CONNECT2/ SSEL1	69[1]	T7[1]	I/O	**P0[14]** — General purpose digital input/output pin.
			O	**USB_HSTEN2** — Host Enabled status for USB port 2.
			O	**USB_CONNECT2** — SoftConnect control for USB port 2. Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
			I/O	**SSEL1** — Slave Select for SSP1.
P0[15]/TXD1/ SCK0/SCK	128[1]	J16[1]	I/O	**P0[15]** — General purpose digital input/output pin.
			O	**TXD1** — Transmitter output for UART1.
			I/O	**SCK0** — Serial clock for SSP0.
			I/O	**SCK** — Serial clock for SPI.
P0[16]/RXD1/ SSEL0/SSEL	130[1]	J14[1]	I/O	**P0 [16]** — General purpose digital input/output pin.
			I	**RXD1** — Receiver input for UART1.
			I/O	**SSEL0** — Slave Select for SSP0.
			I/O	**SSEL** — Slave Select for SPI.
P0[17]/CTS1/ MISO0/MISO	126[1]	K17[1]	I/O	**P0[17]** — General purpose digital input/output pin.
			I	**CTS1** — Clear to Send input for UART1.
			I/O	**MISO0** — Master In Slave Out for SSP0.
			I/O	**MISO** — Master In Slave Out for SPI.
P0[18]/DCD1/ MOSI0/MOSI	124[1]	K15[1]	I/O	**P0[18]** — General purpose digital input/output pin.
			I	**DCD1** — Data Carrier Detect input for UART1.
			I/O	**MOSI0** — Master Out Slave In for SSP0.
			I/O	**MOSI** — Master Out Slave In for SPI.
P0[19]/DSR1/ MCICLK/SDA1	122[1]	L17[1]	I/O	**P0[19]** — General purpose digital input/output pin.
			I	**DSR1** — Data Set Ready input for UART1.
			O	**MCICLK** — Clock output line for SD/MMC interface.
			I/O	**SDA1** — I^2C1 data input/output (this is not an open-drain pin).
P0[20]/DTR1/ MCICMD/SCL1	120[1]	M17[1]	I/O	**P0[20]** — General purpose digital input/output pin.
			O	**DTR1** — Data Terminal Ready output for UART1.
			I/O	**MCICMD** — Command line for SD/MMC interface.
			I/O	**SCL1** — I^2C1 clock input/output (this is not an open-drain pin).
P0[21]/RI1/ MCIPWR/RD1	118[1]	M16[1]	I/O	**P0[21]** — General purpose digital input/output pin.
			I	**RI1** — Ring Indicator input for UART1.
			O	**MCIPWR** — Power Supply Enable for external SD/MMC power supply.
			I	**RD1** — CAN1 receiver input.
P0[22]/RTS1/ MCIDAT0/TD1	116[1]	N17[1]	I/O	**P0[22]** — General purpose digital input/output pin.
			O	**RTS1** — Request to Send output for UART1.
			I/O	**MCIDAT0** — Data line 0 for SD/MMC interface.
			O	**TD1** — CAN1 transmitter output.

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P0[23]/AD0[0]/ I2SRX_CLK/ CAP3[0]	18[2]	H1[2]	I/O	**P0[23] —** General purpose digital input/output pin.
			I	**AD0[0] —** A/D converter 0, input 0.
			I/O	**I2SRX_CLK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*.
			I	**CAP3[0] —** Capture input for Timer 3, channel 0.
P0[24]/AD0[1]/ I2SRX_WS/ CAP3[1]	16[2]	G2[2]	I/O	**P0[24] —** General purpose digital input/output pin.
			I	**AD0[1] —** A/D converter 0, input 1.
			I/O	**I2SRX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
			I	**CAP3[1] —** Capture input for Timer 3, channel 1.
P0[25]/AD0[2]/ I2SRX_SDA/ TXD3	14[2]	F1[2]	I/O	**P0[25] —** General purpose digital input/output pin.
			I	**AD0[2] —** A/D converter 0, input 2.
			I/O	**I2SRX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
			O	**TXD3 —** Transmitter output for UART3.
P0[26]/AD0[3]/ AOUT/RXD3	12[2][3]	E1[2][3]	I/O	**P0[26] —** General purpose digital input/output pin.
			I	**AD0[3] —** A/D converter 0, input 3.
			O	**AOUT —** D/A converter output.
			I	**RXD3 —** Receiver input for UART3.
P0[27]/SDA0	50[4]	T1[4]	I/O	**P0[27] —** General purpose digital input/output pin. Output is open-drain.
			I/O	**SDA0 —** I²C0 data input/output. Open-drain output (for I²C-bus compliance).
P0[28]/SCL0	48[4]	R3[4]	I/O	**P0[28] —** General purpose digital input/output pin. Output is open-drain.
			I/O	**SCL0 —** I²C0 clock input/output. Open-drain output (for I²C-bus compliance).
P0[29]/USB_D+1	61[5]	U4[5]	I/O	**P0[29] —** General purpose digital input/output pin.
			I/O	**USB_D+1 —** USB port 1 bidirectional D+ line.
P0[30]/USB_D−1	62[5]	R6[5]	I/O	**P0[30] —** General purpose digital input/output pin.
			I/O	**USB_D−1 —** USB port 1 bidirectional D− line.
P0[31]/USB_D+2	51[5]	T2[5]	I/O	**P0[31] —** General purpose digital input/output pin.
			I/O	**USB_D+2 —** USB port 2 bidirectional D+ line.
P1[0] to P1[31]			I/O	**Port 1:** Port 1 is a 32 bit I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block.
P1[0]/ ENET_TXD0	196[1]	A3[1]	I/O	**P1[0] —** General purpose digital input/output pin.
			O	**ENET_TXD0 —** Ethernet transmit data 0 (RMII/MII interface).
P1[1]/ ENET_TXD1	194[1]	B5[1]	I/O	**P1[1] —** General purpose digital input/output pin.
			O	**ENET_TXD1 —** Ethernet transmit data 1 (RMII/MII interface).
P1[2]/ ENET_TXD2/ MCICLK/ PWM0[1]	185[1]	D9[1]	I/O	**P1[2] —** General purpose digital input/output pin.
			O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
			O	**MCICLK —** Clock output line for SD/MMC interface.
			O	**PWM0[1] —** Pulse Width Modulator 0, output 1.

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P1[3]/ ENET_TXD3/ MCICMD/ PWM0[2]	177[1]	A10[1]	I/O	**P1[3] —** General purpose digital input/output pin.
			O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
			I/O	**MCICMD —** Command line for SD/MMC interface.
			O	**PWM0[2] —** Pulse Width Modulator 0, output 2.
P1[4]/ ENET_TX_EN	192[1]	A5[1]	I/O	**P1[4] —** General purpose digital input/output pin.
			O	**ENET_TX_EN —** Ethernet transmit data enable (RMII/MII interface).
P1[5]/ ENET_TX_ER/ MCIPWR/ PWM0[3]	156[1]	A17[1]	I/O	**P1[5] —** General purpose digital input/output pin.
			O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
			O	**MCIPWR —** Power Supply Enable for external SD/MMC power supply.
			O	**PWM0[3] —** Pulse Width Modulator 0, output 3.
P1[6]/ ENET_TX_CLK/ MCIDAT0/ PWM0[4]	171[1]	B11[1]	I/O	**P1[6] —** General purpose digital input/output pin.
			I	**ENET_TX_CLK —** Ethernet Transmit Clock (MII interface).
			I/O	**MCIDAT0 —** Data line 0 for SD/MMC interface.
			O	**PWM0[4] —** Pulse Width Modulator 0, output 4.
P1[7]/ ENET_COL/ MCIDAT1/ PWM0[5]	153[1]	D14[1]	I/O	**P1[7] —** General purpose digital input/output pin.
			I	**ENET_COL —** Ethernet Collision detect (MII interface).
			I/O	**MCIDAT1 —** Data line 1 for SD/MMC interface.
			O	**PWM0[5] —** Pulse Width Modulator 0, output 5.
P1[8]/ ENET_CRS_DV/ ENET_CRS	190[1]	C7[1]	I/O	**P1[8] —** General purpose digital input/output pin.
			I	**ENET_CRS_DV/ENET_CRS —** Ethernet Carrier Sense/Data Valid (RMII interface)/ Ethernet Carrier Sense (MII interface).
P1[9]/ ENET_RXD0	188[1]	A6[1]	I/O	**P1[9] —** General purpose digital input/output pin.
			I	**ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface).
P1[10]/ ENET_RXD1	186[1]	C8[1]	I/O	**P1[10] —** General purpose digital input/output pin.
			I	**ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface).
P1[11]/ ENET_RXD2/ MCIDAT2/ PWM0[6]	163[1]	A14[1]	I/O	**P1[11] —** General purpose digital input/output pin.
			I	**ENET_RXD2 —** Ethernet Receive Data 2 (MII interface).
			I/O	**MCIDAT2 —** Data line 2 for SD/MMC interface.
			O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
P1[12]/ ENET_RXD3/ MCIDAT3/ PCAP0[0]	157[1]	A16[1]	I/O	**P1[12] —** General purpose digital input/output pin.
			I	**ENET_RXD3 —** Ethernet Receive Data (MII interface).
			I/O	**MCIDAT3 —** Data line 3 for SD/MMC interface.
			I	**PCAP0[0] —** Capture input for PWM0, channel 0.
P1[13]/ ENET_RX_DV	147[1]	D16[1]	I/O	**P1[13] —** General purpose digital input/output pin.
			I	**ENET_RX_DV —** Ethernet Receive Data Valid (MII interface).
P1[14]/ ENET_RX_ER	184[1]	A7[1]	I/O	**P1[14] —** General purpose digital input/output pin.
			I	**ENET_RX_ER —** Ethernet receive error (RMII/MII interface).
P1[15]/ ENET_REF_CLK/ ENET_RX_CLK	182[1]	A8[1]	I/O	**P1[15] —** General purpose digital input/output pin.
			I	**ENET_REF_CLK/ENET_RX_CLK —** Ethernet Reference Clock (RMII interface)/ Ethernet Receive Clock (MII interface).

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P1[16]/ ENET_MDC	180[1]	D10[1]	I/O	**P1[16] —** General purpose digital input/output pin.
			O	**ENET_MDC —** Ethernet MIIM clock.
P1[17]/ ENET_MDIO	178[1]	A9[1]	I/O	**P1[17] —** General purpose digital input/output pin.
			I/O	**ENET_MDIO —** Ethernet MIIM data input and output.
P1[18]/ USB_UP_LED1/ PWM1[1]/CAP1[0]	66[1]	P7[1]	I/O	**P1[18] —** General purpose digital input/output pin.
			O	**USB_UP_LED1 —** USB port 1 GoodLink LED indicator. It is LOW when device is configured (non-control endpoints enabled), or when host is enabled and has detected a device on the bus. It is HIGH when the device is not configured or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when host is enabled and detects activity on the bus.
			O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
			I	**CAP1[0] —** Capture input for Timer 1, channel 0.
P1[19]/ $\overline{\text{USB\_TX\_E1}}$/ $\overline{\text{USB\_PPWR1}}$/ CAP1[1]	68[1]	U6[1]	I/O	**P1[19] —** General purpose digital input/output pin.
			O	**$\overline{\text{USB\_TX\_E1}}$ —** Transmit Enable signal for USB port 1 (OTG transceiver).
			O	**$\overline{\text{USB\_PPWR1}}$ —** Port Power enable signal for USB port 1.
			I	**CAP1[1] —** Capture input for Timer 1, channel 1.
P1[20]/ USB_TX_DP1/ LCDVD[6]/ LCDVD[10]/ PWM1[2]/SCK0	70[1]	U7[1]	I/O	**P1[20] —** General purpose digital input/output pin.
			O	**USB_TX_DP1 —** D+ transmit data for USB port 1 (OTG transceiver).[18]
			O	**LCDVD[6]/LCDVD[10] —** LCD data.[18]
			O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
			I/O	**SCK0 —** Serial clock for SSP0.
P1[21]/ USB_TX_DM1/ LCDVD[7]/ LCDVD[11]/ PWM1[3]/SSEL0	72[1]	R8[1]	I/O	**P1[21] —** General purpose digital input/output pin.
			O	**USB_TX_DM1 —** D− transmit data for USB port 1 (OTG transceiver).[18]
			O	**LCDVD[7]/LCDVD[11] —** LCD data.[18]
			O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
			I/O	**SSEL0 —** Slave Select for SSP0.
P1[22]/USB_RCV1/ LCDVD[8]/ LCDVD[12]/ USB_PWRD1/ MAT1[0]	74[1]	U8[1]	I/O	**P1[22] —** General purpose digital input/output pin.
			I	**USB_RCV1 —** Differential receive data for USB port 1 (OTG transceiver).[18]
			O	**LCDVD[8]/LCDVD[12] —** LCD data.[18]
			I	**USB_PWRD1 —** Power Status for USB port 1 (host power switch).
			O	**MAT1[0] —** Match output for Timer 1, channel 0.
P1[23]/ USB_RX_DP1/ LCDVD[9]/ LCDVD[13]/ PWM1[4]/MISO0	76[1]	P9[1]	I/O	**P1[23] —** General purpose digital input/output pin.
			I	**USB_RX_DP1 —** D+ receive data for USB port 1 (OTG transceiver).[18]
			O	**LCDVD[9]/LCDVD[13] —** LCD data.[18]
			O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
			I/O	**MISO0 —** Master In Slave Out for SSP0.

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P1[24]/ USB_RX_DM1/ LCDVD[10]/ LCDVD[14]/ PWM1[5]/MOSI0	78[1]	T9[1]	I/O	**P1[24]** — General purpose digital input/output pin.
			I	**USB_RX_DM1** — D− receive data for USB port 1 (OTG transceiver).[18]
			O	**LCDVD[10]/LCDVD[14]** — LCD data.[18]
			O	**PWM1[5]** — Pulse Width Modulator 1, channel 5 output.
			I/O	**MOSI0** — Master Out Slave in for SSP0.
P1[25]/$\overline{\text{USB\_LS1}}$/ LCDVD[11]/ LCDVD[15]/ $\overline{\text{USB\_HSTEN1}}$/ MAT1[1]	80[1]	T10[1]	I/O	**P1[25]** — General purpose digital input/output pin.
			O	**$\overline{\text{USB\_LS1}}$** — Low Speed status for USB port 1 (OTG transceiver).[18]
			O	**LCDVD[11]/LCDVD[15]** — LCD data.[18]
			O	**$\overline{\text{USB\_HSTEN1}}$** — Host Enabled status for USB port 1.
			O	**MAT1[1]** — Match output for Timer 1, channel 1.
P1[26]/ $\overline{\text{USB\_SSPND1}}$/ LCDVD[12]/ LCDVD[20]/ PWM1[6]/CAP0[0]	82[1]	R10[1]	I/O	**P1[26]** — General purpose digital input/output pin.
			O	**$\overline{\text{USB\_SSPND1}}$** — USB port 1 Bus Suspend status (OTG transceiver).[18]
			O	**LCDVD[12]/LCDVD[20]** — LCD data.[18]
			O	**PWM1[6]** — Pulse Width Modulator 1, channel 6 output.
			I	**CAP0[0]** — Capture input for Timer 0, channel 0.
P1[27]/$\overline{\text{USB\_INT1}}$/ LCDVD[13]/ LCDVD[21]/ $\overline{\text{USB\_OVRCR1}}$/ CAP0[1]	88[1]	T12[1]	I/O	**P1[27]** — General purpose digital input/output pin.
			I	**$\overline{\text{USB\_INT1}}$** — USB port 1 OTG transceiver interrupt (OTG transceiver).[18]
			O	**LCDVD[13]/LCDVD[21]** — LCD data.[18]
			I	**$\overline{\text{USB\_OVRCR1}}$** — USB port 1 Over-Current status.
			I	**CAP0[1]** — Capture input for Timer 0, channel 1.
P1[28]/USB_SCL1/ LCDVD[14]/ LCDVD[22]/ PCAP1[0]/MAT0[0]	90[1]	T13[1]	I/O	**P1[28]** — General purpose digital input/output pin.
			I/O	**USB_SCL1** — USB port 1 I^2C-bus serial clock (OTG transceiver).[18]
			O	**LCDVD[14]/LCDVD[22]** — LCD data.[18]
			I	**PCAP1[0]** — Capture input for PWM1, channel 0.
			O	**MAT0[0]** — Match output for Timer 0, channel 0.
P1[29]/USB_SDA1/ LCDVD[15]/ LCDVD[23]/ PCAP1[1]/MAT0[1]	92[1]	U14[1]	I/O	**P1[29]** — General purpose digital input/output pin.
			I/O	**USB_SDA1** — USB port 1 I^2C-bus serial data (OTG transceiver).[18]
			O	**LCDVD[15]/LCDVD[23]** — LCD data.[18]
			I	**PCAP1[1]** — Capture input for PWM1, channel 1.
			O	**MAT0[1]** — Match output for Timer 0, channel 0.
P1[30]/ USB_PWRD2/ V_{BUS}/AD0[4]	42[2]	P2[2]	I/O	**P1[30]** — General purpose digital input/output pin.
			I	**USB_PWRD2** — Power Status for USB port 2.
			I	**V_{BUS}** — Monitors the presence of USB bus power. **Note:** This signal must be HIGH for USB reset to occur.
			I	**AD0[4]** — A/D converter 0, input 4.
P1[31]/ $\overline{\text{USB\_OVRCR2}}$/ SCK1/AD0[5]	40[2]	P1[2]	I/O	**P1[31]** — General purpose digital input/output pin.
			I	**$\overline{\text{USB\_OVRCR2}}$** — Over-Current status for USB port 2.
			I/O	**SCK1** — Serial Clock for SSP1.
			I	**AD0[5]** — A/D converter 0, input 5.

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P2[0] to P2[31]			I/O	**Port 2:** Port 2 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the pin connect block.

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P2[0]/PWM1[1]/ TXD1/TRACECLK/ LCDPWR	154[1]	B17[1]	I/O	**P2[0] —** General purpose digital input/output pin.
			O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
			O	**TXD1 —** Transmitter output for UART1.
			O	**TRACECLK —** Trace clock.[19]
			O	**LCDPWR —** LCD panel power enable.[19]
P2[1]/PWM1[2]/ RXD1/PIPESTAT0/ LCDLE	152[1]	E14[1]	I/O	**P2[1] —** General purpose digital input/output pin.
			O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
			I	**RXD1 —** Receiver input for UART1.
			O	**PIPESTAT0 —** Pipeline status, bit 0.[19]
			O	**LCDLE —** Line end signal.[19]
P2[2]/PWM1[3]/ CTS1/PIPESTAT1/ LCDDCLK	150[1]	D15[1]	I/O	**P2[2] —** General purpose digital input/output pin.
			O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
			I	**CTS1 —** Clear to Send input for UART1.
			O	**PIPESTAT1 —** Pipeline status, bit 1.[19]
			O	**LCDDCLK —** LCD panel clock.[19]
P2[3]/PWM1[4]/ DCD1/PIPESTAT2/ LCDFP	144[1]	E16[1]	I/O	**P2[3] —** General purpose digital input/output pin.
			O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
			I	**DCD1 —** Data Carrier Detect input for UART1.
			O	**PIPESTAT2 —** Pipeline status, bit 2.[19]
			O	**LCDFP —** Frame pulse (STN). Vertical synchronization pulse (TFT).[19]
P2[4]/PWM1[5]/ DSR1/ TRACESYNC/ LCDENAB/LCDM	142[1]	D17[1]	I/O	**P2[4] —** General purpose digital input/output pin.
			O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
			I	**DSR1 —** Data Set Ready input for UART1.
			O	**TRACESYNC —** Trace Synchronization.[19]
			O	**LCDENAB/LCDM —** STN AC bias drive or TFT data enable output.[19]
P2[5]/PWM1[6]/ DTR1/ TRACEPKT0/ LCDLP	140[1]	F16[1]	I/O	**P2[5] —** General purpose digital input/output pin.
			O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
			O	**DTR1 —** Data Terminal Ready output for UART1.
			O	**TRACEPKT0 —** Trace Packet, bit 0.[19]
			O	**LCDLP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).[19]
P2[6]/PCAP1[0]/ RI1/ TRACEPKT1/ LCDVD[0]/ LCDVD[4]	138[1]	E17[1]	I/O	**P2[6] —** General purpose digital input/output pin.
			I	**PCAP1[0] —** Capture input for PWM1, channel 0.
			I	**RI1 —** Ring Indicator input for UART1.
			O	**TRACEPKT1 —** Trace Packet, bit 1.[19]
			O	**LCDVD[0]/LCDVD[4] —** LCD data.[19]
P2[7]/RD2/ RTS1/ TRACEPKT2/ LCDVD[1]/ LCDVD[5]	136[1]	G16[1]	I/O	**P2[7] —** General purpose digital input/output pin.
			I	**RD2 —** CAN2 receiver input.
			O	**RTS1 —** Request to Send output for UART1.
			O	**TRACEPKT2 —** Trace Packet, bit 2.[19]
			O	**LCDVD[1]/LCDVD[5] —** LCD data.[19]

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P2[8]/TD2/TXD2/ TRACEPKT3/ LCDVD[2]/ LCDVD[6]	134[1]	H15[1]	I/O	**P2[8] —** General purpose digital input/output pin.
			O	**TD2 —** CAN2 transmitter output.
			O	**TXD2 —** Transmitter output for UART2.
			O	**TRACEPKT3 —** Trace packet, bit 3.[19]
			O	**LCDVD[2]/LCDVD[6] —** LCD data.[19]
P2[9]/ USB_CONNECT1/ RXD2/EXTIN0/ LCDVD[3]/ LCDVD[7]	132[1]	H16[1]	I/O	**P2[9] —** General purpose digital input/output pin.
			O	**USB_CONNECT1 —** USB1 SoftConnect control. Signal used to switch an external 1.5 kΩ resistor under the software control. Used with the SoftConnect USB feature.
			I	**RXD2 —** Receiver input for UART2.
			I	**EXTIN0 —** External Trigger Input.[19]
			O	**LCDVD[3]/LCDVD[7] —** LCD data.[19]
P2[10]/$\overline{\text{EINT0}}$	110[6]	N15[6]	I/O	**P2[10] —** General purpose digital input/output pin. **Note:** LOW on this pin while RESET is LOW forces on-chip bootloader to take over control of the part after a reset.
			I	**$\overline{\text{EINT0}}$ —** External interrupt 0 input.
P2[11]/$\overline{\text{EINT1}}$/ LCDCLKIN/ MCIDAT1/ I2STX_CLK	108[6]	T17[6]	I/O	**P2[11] —** General purpose digital input/output pin.
			I	**$\overline{\text{EINT1}}$ —** External interrupt 1 input.[20]
			O	**LCDCLKIN —** LCD clock.[20]
			I/O	**MCIDAT1 —** Data line 1 for SD/MMC interface.
			I/O	**I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
P2[12]/$\overline{\text{EINT2}}$/ LCDVD[4]/ LCDVD[3]/ LCDVD[8]/ LCDVD[18]/ MCIDAT2/ I2STX_WS	106[6]	N14[6]	I/O	**P2[12] —** General purpose digital input/output pin.
			I	**$\overline{\text{EINT2}}$ —** External interrupt 2 input.[20]
			O	**LCDVD[4]/LCDVD[3]/LCDVD[8]/LCDVD[18] —** LCD data.[20]
			I/O	**MCIDAT2 —** Data line 2 for SD/MMC interface.
			I/O	**I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
P2[13]/$\overline{\text{EINT3}}$/ LCDVD[5]/ LCDVD[9]/ LCDVD[19]/ MCIDAT3/ I2STX_SDA	102[6]	T16[6]	I/O	**P2[13] —** General purpose digital input/output pin.
			I	**$\overline{\text{EINT3}}$ —** External interrupt 3 input.[20]
			O	**LCDVD[5]/LCDVD[9]/LCDVD[19] —** LCD data.[20]
			I/O	**MCIDAT3 —** Data line 3 for SD/MMC interface.
			I/O	**I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
P2[14]/$\overline{\text{CS2}}$/ CAP2[0]/SDA1	91[6]	R12[6]	I/O	**P2[14] —** General purpose digital input/output pin.
			O	**$\overline{\text{CS2}}$ —** LOW active Chip Select 2 signal.
			I	**CAP2[0] —** Capture input for Timer 2, channel 0.
			I/O	**SDA1 —** I^2C1 data input/output (this is not an open-drain pin).
P2[15]/$\overline{\text{CS3}}$/ CAP2[1]/SCL1	99[6]	P13[6]	I/O	**P2[15] —** General purpose digital input/output pin.
			O	**$\overline{\text{CS3}}$ —** LOW active Chip Select 3 signal.
			I	**CAP2[1] —** Capture input for Timer 2, channel 1.
			I/O	**SCL1 —** I^2C1 clock input/output (this is not an open-drain pin).

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P2[16]/$\overline{\text{CAS}}$	87[1]	R11[1]	I/O	**P2[16]** — General purpose digital input/output pin.
			O	**$\overline{\text{CAS}}$** — LOW active SDRAM Column Address Strobe.
P2[17]/$\overline{\text{RAS}}$	95[1]	R13[1]	I/O	**P2[17]** — General purpose digital input/output pin.
			O	**$\overline{\text{RAS}}$** — LOW active SDRAM Row Address Strobe.
P2[18]/ CLKOUT0	59[1]	U3[1]	I/O	**P2[18]** — General purpose digital input/output pin.
			O	**CLKOUT0** — SDRAM clock 0.
P2[19]/ CLKOUT1	67[1]	R7[1]	I/O	**P2[19]** — General purpose digital input/output pin.
			O	**CLKOUT1** — SDRAM clock 1.
P2[20]/$\overline{\text{DYCS0}}$	73[1]	T8[1]	I/O	**P2[20]** — General purpose digital input/output pin.
			O	**$\overline{\text{DYCS0}}$** — SDRAM chip select 0.
P2[21]/$\overline{\text{DYCS1}}$	81[1]	U11[1]	I/O	**P2[21]** — General purpose digital input/output pin.
			O	**$\overline{\text{DYCS1}}$** — SDRAM chip select 1.
P2[22]/$\overline{\text{DYCS2}}$/ CAP3[0]/SCK0	85[1]	U12[1]	I/O	**P2[22]** — General purpose digital input/output pin.
			O	**$\overline{\text{DYCS2}}$** — SDRAM chip select 2.
			I	**CAP3[0]** — Capture input for Timer 3, channel 0.
			I/O	**SCK0** — Serial clock for SSP0.
P2[23]/$\overline{\text{DYCS3}}$/ CAP3[1]/SSEL0	64[1]	U5[1]	I/O	**P2[23]** — General purpose digital input/output pin.
			O	**$\overline{\text{DYCS3}}$** — SDRAM chip select 3.
			I	**CAP3[1]** — Capture input for Timer 3, channel 1.
			I/O	**SSEL0** — Slave Select for SSP0.
P2[24]/ CKEOUT0	53[1]	P5[1]	I/O	**P2[24]** — General purpose digital input/output pin.
			O	**CKEOUT0** — SDRAM clock enable 0.
P2[25]/ CKEOUT1	54[1]	R4[1]	I/O	**P2[25]** — General purpose digital input/output pin.
			O	**CKEOUT1** — SDRAM clock enable 1.
P2[26]/ CKEOUT2/ MAT3[0]/MISO0	57[1]	T4[1]	I/O	**P2[26]** — General purpose digital input/output pin.
			O	**CKEOUT2** — SDRAM clock enable 2.
			O	**MAT3[0]** — Match output for Timer 3, channel 0.
			I/O	**MISO0** — Master In Slave Out for SSP0.
P2[27]/ CKEOUT3/ MAT3[1]/MOSI0	47[1]	P3[1]	I/O	**P2[27]** — General purpose digital input/output pin.
			O	**CKEOUT3** — SDRAM clock enable 3.
			O	**MAT3[1]** — Match output for Timer 3, channel 1.
			I/O	**MOSI0** — Master Out Slave In for SSP0.
P2[28]/ DQMOUT0	49[1]	P4[1]	I/O	**P2[28]** — General purpose digital input/output pin.
			O	**DQMOUT0** — Data mask 0 used with SDRAM and static devices.
P2[29]/ DQMOUT1	43[1]	N3[1]	I/O	**P2[29]** — General purpose digital input/output pin.
			O	**DQMOUT1** — Data mask 1 used with SDRAM and static devices.
P2[30]/ DQMOUT2/ MAT3[2]/SDA2	31[1]	L4[1]	I/O	**P2[30]** — General purpose digital input/output pin.
			O	**DQMOUT2** — Data mask 2 used with SDRAM and static devices.
			O	**MAT3[2]** — Match output for Timer 3, channel 2.
			I/O	**SDA2** — I^2C2 data input/output (this is not an open-drain pin).

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P2[31]/ DQMOUT3/ MAT3[3]/SCL2	39[1]	N2[1]	I/O	**P2[31] —** General purpose digital input/output pin.
			O	**DQMOUT3 —** Data mask 3 used with SDRAM and static devices.
			O	**MAT3[3] —** Match output for Timer 3, channel 3.
			I/O	**SCL2 —** I^2C2 clock input/output (this is not an open-drain pin).
P3[0] to P3[31]			I/O	**Port 3:** Port 3 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the pin connect block.
P3[0]/D0	197[1]	B4[1]	I/O	**P3[0] —** General purpose digital input/output pin.
			I/O	**D0 —** External memory data line 0.
P3[1]/D1	201[1]	B3[1]	I/O	**P3[1] —** General purpose digital input/output pin.
			I/O	**D1 —** External memory data line 1.
P3[2]/D2	207[1]	B1[1]	I/O	**P3[2] —** General purpose digital input/output pin.
			I/O	**D2 —** External memory data line 2.
P3[3]/D3	3[1]	E4[1]	I/O	**P3[3] —** General purpose digital input/output pin.
			I/O	**D3 —** External memory data line 3.
P3[4]/D4	13[1]	F2[1]	I/O	**P3[4] —** General purpose digital input/output pin.
			I/O	**D4 —** External memory data line 4.
P3[5]/D5	17[1]	G1[1]	I/O	**P3[5] —** General purpose digital input/output pin.
			I/O	**D5 —** External memory data line 5.
P3[6]/D6	23[1]	J1[1]	I/O	**P3[6] —** General purpose digital input/output pin.
			I/O	**D6 —** External memory data line 6.
P3[7]/D7	27[1]	L1[1]	I/O	**P3[7] —** General purpose digital input/output pin.
			I/O	**D7 —** External memory data line 7.
P3[8]/D8	191[1]	D8[1]	I/O	**P3[8] —** General purpose digital input/output pin.
			I/O	**D8 —** External memory data line 8.
P3[9]/D9	199[1]	C5[1]	I/O	**P3[9] —** General purpose digital input/output pin.
			I/O	**D9 —** External memory data line 9.
P3[10]/D10	205[1]	B2[1]	I/O	**P3[10] —** General purpose digital input/output pin.
			I/O	**D10 —** External memory data line 10.
P3[11]/D11	208[1]	D5[1]	I/O	**P3[11] —** General purpose digital input/output pin.
			I/O	**D11 —** External memory data line 11.
P3[12]/D12	1[1]	D4[1]	I/O	**P3[12] —** General purpose digital input/output pin.
			I/O	**D12 —** External memory data line 12.
P3[13]/D13	7[1]	C1[1]	I/O	**P3[13] —** General purpose digital input/output pin.
			I/O	**D13 —** External memory data line 13.
P3[14]/D14	21[1]	H2[1]	I/O	**P3[14] —** General purpose digital input/output pin.
			I/O	**D14 —** External memory data line 14.
P3[15]/D15	28[1]	M1[1]	I/O	**P3[15] —** General purpose digital input/output pin.
			I/O	**D15 —** External memory data line 15.

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P3[16]/D16/ PWM0[1]/TXD1	137[1]	F17[1]	I/O	**P3[16]** — General purpose digital input/output pin.
			I/O	**D16** — External memory data line 16.
			O	**PWM0[1]** — Pulse Width Modulator 0, output 1.
			O	**TXD1** — Transmitter output for UART1.
P3[17]/D17/ PWM0[2]/RXD1	143[1]	F15[1]	I/O	**P3[17]** — General purpose digital input/output pin.
			I/O	**D17** — External memory data line 17.
			O	**PWM0[2]** — Pulse Width Modulator 0, output 2.
			I	**RXD1** — Receiver input for UART1.
P3[18]/D18/ PWM0[3]/CTS1	151[1]	C15[1]	I/O	**P3[18]** — General purpose digital input/output pin.
			I/O	**D18** — External memory data line 18.
			O	**PWM0[3]** — Pulse Width Modulator 0, output 3.
			I	**CTS1** — Clear to Send input for UART1.
P3[19]/D19/ PWM0[4]/DCD1	161[1]	B14[1]	I/O	**P3[19]** — General purpose digital input/output pin.
			I/O	**D19** — External memory data line 19.
			O	**PWM0[4]** — Pulse Width Modulator 0, output 4.
			I	**DCD1** — Data Carrier Detect input for UART1.
P3[20]/D20/ PWM0[5]/DSR1	167[1]	A13[1]	I/O	**P3[20]** — General purpose digital input/output pin.
			I/O	**D20** — External memory data line 20.
			O	**PWM0[5]** — Pulse Width Modulator 0, output 5.
			I	**DSR1** — Data Set Ready input for UART1.
P3[21]/D21/ PWM0[6]/DTR1	175[1]	C10[1]	I/O	**P3[21]** — General purpose digital input/output pin.
			I/O	**D21** — External memory data line 21.
			O	**PWM0[6]** — Pulse Width Modulator 0, output 6.
			O	**DTR1** — Data Terminal Ready output for UART1.
P3[22]/D22/ PCAP0[0]/RI1	195[1]	C6[1]	I/O	**P3[22]** — General purpose digital input/output pin.
			I/O	**D22** — External memory data line 22.
			I	**PCAP0[0]** — Capture input for PWM0, channel 0.
			I	**RI1** — Ring Indicator input for UART1.
P3[23]/D23/ CAP0[0]/ PCAP1[0]	65[1]	T6[1]	I/O	**P3[23]** — General purpose digital input/output pin.
			I/O	**D23** — External memory data line 23.
			I	**CAP0[0]** — Capture input for Timer 0, channel 0.
			I	**PCAP1[0]** — Capture input for PWM1, channel 0.
P3[24]/D24/ CAP0[1]/ PWM1[1]	58[1]	R5[1]	I/O	**P3[24]** — General purpose digital input/output pin.
			I/O	**D24** — External memory data line 24.
			I	**CAP0[1]** — Capture input for Timer 0, channel 1.
			O	**PWM1[1]** — Pulse Width Modulator 1, output 1.
P3[25]/D25/ MAT0[0]/ PWM1[2]	56[1]	U2[1]	I/O	**P3[25]** — General purpose digital input/output pin.
			I/O	**D25** — External memory data line 25.
			O	**MAT0[0]** — Match output for Timer 0, channel 0.
			O	**PWM1[2]** — Pulse Width Modulator 1, output 2.

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P3[26]/D26/ MAT0[1]/ PWM1[3]	55[1]	T3[1]	I/O	**P3[26] —** General purpose digital input/output pin.
			I/O	**D26 —** External memory data line 26.
			O	**MAT0[1] —** Match output for Timer 0, channel 1.
			O	**PWM1[3] —** Pulse Width Modulator 1, output 3.
P3[27]/D27/ CAP1[0]/ PWM1[4]	203[1]	A1[1]	I/O	**P3[27] —** General purpose digital input/output pin.
			I/O	**D27 —** External memory data line 27.
			I	**CAP1[0] —** Capture input for Timer 1, channel 0.
			O	**PWM1[4] —** Pulse Width Modulator 1, output 4.
P3[28]/D28/ CAP1[1]/ PWM1[5]	5[1]	D2[1]	I/O	**P3[28] —** General purpose digital input/output pin.
			I/O	**D28 —** External memory data line 28.
			I	**CAP1[1] —** Capture input for Timer 1, channel 1.
			O	**PWM1[5] —** Pulse Width Modulator 1, output 5.
P3[29]/D29/ MAT1[0]/ PWM1[6]	11[1]	F3[1]	I/O	**P3[29] —** General purpose digital input/output pin.
			I/O	**D29 —** External memory data line 29.
			O	**MAT1[0] —** Match output for Timer 1, channel 0.
			O	**PWM1[6] —** Pulse Width Modulator 1, output 6.
P3[30]/D30/ MAT1[1]/ RTS1	19[1]	H3[1]	I/O	**P3[30] —** General purpose digital input/output pin.
			I/O	**D30 —** External memory data line 30.
			O	**MAT1[1] —** Match output for Timer 1, channel 1.
			O	**RTS1 —** Request to Send output for UART1.
P3[31]/D31/ MAT1[2]	25[1]	J3[1]	I/O	**P3[31] —** General purpose digital input/output pin.
			I/O	**D31 —** External memory data line 31.
			O	**MAT1[2] —** Match output for Timer 1, channel 2.
P4[0] to P4[31]			I/O	**Port 4:** Port 4 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 4 pins depends upon the pin function selected via the pin connect block.
P4[0]/A0	75[1]	U9[1]	I/O	**P4[0] —** General purpose digital input/output pin.
			I/O	**A0 —** External memory address line 0.
P4[1]/A1	79[1]	U10[1]	I/O	**P4[1] —** General purpose digital input/output pin.
			I/O	**A1 —** External memory address line 1.
P4[2]/A2	83[1]	T11[1]	I/O	**P4[2] —** General purpose digital input/output pin.
			I/O	**A2 —** External memory address line 2.
P4[3]/A3	97[1]	U16[1]	I/O	**P4[3] —** General purpose digital input/output pin.
			I/O	**A3 —** External memory address line 3.
P4[4]/A4	103[1]	R15[1]	I/O	**P4[4] —** General purpose digital input/output pin.
			I/O	**A4 —** External memory address line 4.
P4[5]/A5	107[1]	R16[1]	I/O	**P4[5] —** General purpose digital input/output pin.
			I/O	**A5 —** External memory address line 5.
P4[6]/A6	113[1]	M14[1]	I/O	**P4[6] —** General purpose digital input/output pin.
			I/O	**A6 —** External memory address line 6.

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P4[7]/A7	121[1]	L16[1]	I/O	**P4[7]** — General purpose digital input/output pin.
			I/O	**A7** — External memory address line 7.
P4[8]/A8	127[1]	J17[1]	I/O	**P4[8]** — General purpose digital input/output pin.
			I/O	**A8** — External memory address line 8.
P4[9]/A9	131[1]	H17[1]	I/O	**P4[9]** — General purpose digital input/output pin.
			I/O	**A9** — External memory address line 9.
P4[10]/A10	135[1]	G17[1]	I/O	**P4[10]** — General purpose digital input/output pin.
			I/O	**A10** — External memory address line 10.
P4[11]/A11	145[1]	F14[1]	I/O	**P4[11]** — General purpose digital input/output pin.
			I/O	**A11** — External memory address line 11.
P4[12]/A12	149[1]	C16[1]	I/O	**P4[12]** — General purpose digital input/output pin.
			I/O	**A12** — External memory address line 12.
P4[13]/A13	155[1]	B16[1]	I/O	**P4[13]** — General purpose digital input/output pin.
			I/O	**A13** — External memory address line 13.
P4[14]/A14	159[1]	B15[1]	I/O	**P4[14]** — General purpose digital input/output pin.
			I/O	**A14** — External memory address line 14.
P4[15]/A15	173[1]	A11[1]	I/O	**P4[15]** — General purpose digital input/output pin.
			I/O	**A15** — External memory address line 15.
P4[16]/A16	101[1]	U17[1]	I/O	**P4[16]** — General purpose digital input/output pin.
			I/O	**A16** — External memory address line 16.
P4[17]/A17	104[1]	P14[1]	I/O	**P4[17]** — General purpose digital input/output pin.
			I/O	**A17** — External memory address line 17.
P4[18]/A18	105[1]	P15[1]	I/O	**P4[18]** — General purpose digital input/output pin.
			I/O	**A18** — External memory address line 18.
P4[19]/A19	111[1]	P16[1]	I/O	**P4[19]** — General purpose digital input/output pin.
			I/O	**A19** — External memory address line 19.
P4[20]/A20/ SDA2/SCK1	109[1]	R17[1]	I/O	**P4[20]** — General purpose digital input/output pin.
			I/O	**A20** — External memory address line 20.
			I/O	**SDA2** — I^2C2 data input/output (this is not an open-drain pin).
			I/O	**SCK1** — Serial Clock for SSP1.
P4[21]/A21/ SCL2/SSEL1	115[1]	M15[1]	I/O	**P4[21]** — General purpose digital input/output pin.
			I/O	**A21** — External memory address line 21.
			I/O	**SCL2** — I^2C2 clock input/output (this is not an open-drain pin).
			I/O	**SSEL1** — Slave Select for SSP1.
P4[22]/A22/ TXD2/MISO1	123[1]	K14[1]	I/O	**P4[22]** — General purpose digital input/output pin.
			I/O	**A22** — External memory address line 22.
			O	**TXD2** — Transmitter output for UART2.
			I/O	**MISO1** — Master In Slave Out for SSP1.

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P4[23]/A23/ RXD2/MOSI1	129[1]	J15[1]	I/O	**P4[23] —** General purpose digital input/output pin.
			I/O	**A23 —** External memory address line 23.
			I	**RXD2 —** Receiver input for UART2.
			I/O	**MOSI1 —** Master Out Slave In for SSP1.
P4[24]/$\overline{OE}$	183[1]	B8[1]	I/O	**P4[24] —** General purpose digital input/output pin.
			O	**$\overline{OE}$ —** LOW active Output Enable signal.
P4[25]/$\overline{WE}$	179[1]	B9[1]	I/O	**P4[25] —** General purpose digital input/output pin.
			O	**$\overline{WE}$ —** LOW active Write Enable signal.
P4[26]/BLS0	119[1]	L15[1]	I/O	**P4[26] —** General purpose digital input/output pin.
			O	**BLS0 —** LOW active Byte Lane select signal 0.
P4[27]/BLS1	139[1]	G15[1]	I/O	**P4[27] —** General purpose digital input/output pin.
			O	**BLS1 —** LOW active Byte Lane select signal 1.
P4[28]/BLS2/ MAT2[0]/LCDVD[6]/ LCDVD[10]/ LCDVD[2]/ TXD3	170[1]	C11[1]	I/O	**P4 [28] —** General purpose digital input/output pin.
			O	**BLS2 —** LOW active Byte Lane select signal 2.
			O	**MAT2[0] —** Match output for Timer 2, channel 0.[21]
			O	**LCDVD[6]/LCDVD[10]/LCDVD[2] —** LCD data.[21]
			O	**TXD3 —** Transmitter output for UART3.
P4[29]/BLS3/ MAT2[1] LCDVD[7]/ LCDVD[11]/ LCDVD[3]/RXD3	176[1]	B10[1]	I/O	**P4[29] —** General purpose digital input/output pin.
			O	**BLS3 —** LOW active Byte Lane select signal 3.
			O	**MAT2[1] —** Match output for Timer 2, channel 1.[21]
			O	**LCDVD[7]/LCDVD[11]/LCDVD[3] —** LCD data.[21]
			I	**RXD3 —** Receiver input for UART3.
P4[30]/$\overline{CS0}$	187[1]	B7[1]	I/O	**P4[30] —** General purpose digital input/output pin.
			O	**$\overline{CS0}$ —** LOW active Chip Select 0 signal.
P4[31]/$\overline{CS1}$	193[1]	A4[1]	I/O	**P4[31] —** General purpose digital input/output pin.
			O	**$\overline{CS1}$ —** LOW active Chip Select 1 signal.
ALARM	37[8]	N1[8]	O	**ALARM —** RTC controlled output. This is a 1.8 V pin. It goes HIGH when a RTC alarm is generated.
USB_D−2	52	U1	I/O	**USB_D−2 —** USB port 2 bidirectional D− line.
DBGEN	9[1][22]	F4[1][22]	I	**DBGEN —** JTAG interface control signal. Also used for boundary scanning.
TDO	2[1][23]	D3[1][23]	O	**TDO —** Test Data Out for JTAG interface.
TDI	4[1][22]	C2[1][22]	I	**TDI —** Test Data In for JTAG interface.
TMS	6[1][22]	E3[1][22]	I	**TMS —** Test Mode Select for JTAG interface.
$\overline{TRST}$	8[1][22]	D1[1][22]	I	**$\overline{TRST}$ —** Test Reset for JTAG interface.
TCK	10[1][23]	E2[1][23]	I	**TCK —** Test Clock for JTAG interface. This clock must be slower than $1/6$ of the CPU clock (CCLK) for the JTAG interface to operate.
RTCK	206[1][22]	C3[1][22]	I/O	**RTCK —** JTAG interface control signal. **Note:** LOW on this pin while $\overline{RESET}$ is LOW enables ETM pins (P2[9:0]) to operate as Trace port after reset.
$\overline{RSTOUT}$	29	K3	O	**$\overline{RSTOUT}$ —** This is a 3.3 V pin. LOW on this pin indicates LPC2478 being in Reset state.