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LPC1769/68/67/66/65/64/63

32-bit Arm Cortex®-M3 microcontroller; up to 512 kB flash and 64 kB SRAM with Ethernet, USB 2.0 Host/Device/OTG, CAN

Rev. 9.8 — 4 May 2018 Product data sheet

1. General description

The LPC1769/68/67/66/65/64/63 are ARM Cortex-M3 based microcontrollers for embedded applications featuring a high level of integration and low power consumption. The Arm Cortex-M3 is a next generation core that offers system enhancements such as enhanced debug features and a higher level of support block integration.

The LPC1768/67/66/65/64/63 operate at CPU frequencies of up to 100 MHz. The LPC1769 operates at CPU frequencies of up to 120 MHz. The Arm Cortex-M3 CPU incorporates a 3-stage pipeline and uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals. The Arm Cortex-M3 CPU also includes an internal prefetch unit that supports speculative branching.

The peripheral complement of the LPC1769/68/67/66/65/64/63 includes up to 512 kB of flash memory, up to 64 kB of data memory, Ethernet MAC, USB Device/Host/OTG interface, 8-channel general purpose DMA controller, 4 UARTs, 2 CAN channels, 2 SSP controllers, SPI interface, 3 I^2C-bus interfaces, 2-input plus 2-output I^2S-bus interface, 8-channel 12-bit ADC, 10-bit DAC, motor control PWM, Quadrature Encoder interface, four general purpose timers, 6-output general purpose PWM, ultra-low power Real-Time Clock (RTC) with separate battery supply, and up to 70 general purpose I/O pins.

The LPC1769/68/67/66/65/64/63 are pin-compatible to the 100-pin LPC236x Arm7-based microcontroller series.

For additional documentation, see Section 19 “References”.

2. Features and benefits

- Arm Cortex-M3 processor, running at frequencies of up to 100 MHz (LPC1768/67/66/65/64/63) or of up to 120 MHz (LPC1769). A Memory Protection Unit (MPU) supporting eight regions is included.
- Arm Cortex-M3 built-in Nested Vectored Interrupt Controller (NVIC).
- Up to 512 kB on-chip flash programming memory. Enhanced flash memory accelerator enables high-speed 120 MHz operation with zero wait states.
- In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
- On-chip SRAM includes:
  - 32/16 kB of SRAM on the CPU with local code/data bus for high-performance CPU access.

- Two/one 16 kB SRAM blocks with separate access paths for higher throughput. These SRAM blocks may be used for Ethernet, USB, and DMA memory, as well as for general purpose CPU instruction and data storage.

- Eight channel General Purpose DMA controller (GPDMA) on the AHB multilayer matrix that can be used with SSP, I^2S-bus, UART, Analog-to-Digital and Digital-to-Analog converter peripherals, timer match signals, and for memory-to-memory transfers.
- Multilayer AHB matrix interconnect provides a separate bus for each AHB master. AHB masters include the CPU, General Purpose DMA controller, Ethernet MAC, and the USB interface. This interconnect provides communication with no arbitration delays.
- Split APB bus allows high throughput with few stalls between the CPU and DMA.
- Serial interfaces:
  - Ethernet MAC with RMII interface and dedicated DMA controller. (Not available on all parts, see Table 2.)
  - USB 2.0 full-speed device/Host/OTG controller with dedicated DMA controller and on-chip PHY for device, Host, and OTG functions. (Not available on all parts, see Table 2.)
  - Four UARTs with fractional baud rate generation, internal FIFO, and DMA support. One UART has modem control I/O and RS-485/EIA-485 support, and one UART has IrDA support.
  - CAN 2.0B controller with two channels. (Not available on all parts, see Table 2.)
  - SPI controller with synchronous, serial, full duplex communication and programmable data length.
  - Two SSP controllers with FIFO and multi-protocol capabilities. The SSP interfaces can be used with the GPDMA controller.
  - Three enhanced I^2C bus interfaces, one with an open-drain output supporting full I^2C specification and Fast mode plus with data rates of 1 Mbit/s, two with standard port pins. Enhancements include multiple address recognition and monitor mode.
  - I^2S (Inter-IC Sound) interface for digital audio input or output, with fractional rate control. The I^2S-bus interface can be used with the GPDMA. The I^2S-bus interface supports 3-wire and 4-wire data transmit and receive as well as master clock input/output. (Not available on all parts, see Table 2.)
- Other peripherals:
  - 70 (100 pin package) General Purpose I/O (GPIO) pins with configurable pull-up/down resistors. All GPIOs support a new, configurable open-drain operating mode. The GPIO block is accessed through the AHB multilayer bus for fast access and located in memory such that it supports Cortex-M3 bit banding and use by the General Purpose DMA Controller.
  - 12-bit Analog-to-Digital Converter (ADC) with input multiplexing among eight pins, conversion rates up to 200 kHz, and multiple result registers. The 12-bit ADC can be used with the GPDMA controller.
  - 10-bit Digital-to-Analog Converter (DAC) with dedicated conversion timer and DMA support. (Not available on all parts, see Table 2)
  - Four general purpose timers/counters, with a total of eight capture inputs and ten compare outputs. Each timer block has an external count input. Specific timer events can be selected to generate DMA requests.
  - One motor control PWM with support for three-phase motor control.

- Quadrature encoder interface that can monitor one external quadrature encoder.
- One standard PWM/timer block with external count input.
- RTC with a separate power domain and dedicated RTC oscillator. The RTC block includes 20 bytes of battery-powered backup registers.
- WatchDog Timer (WDT). The WDT can be clocked from the internal RC oscillator, the RTC oscillator, or the APB clock.
- Arm Cortex-M3 system tick timer, including an external clock input option.
- Repetitive interrupt timer provides programmable and repeating timed interrupts.
- Each peripheral has its own clock divider for further power savings.

- Standard JTAG debug interface for compatibility with existing tools. Serial Wire Debug and Serial Wire Trace Port options. Boundary Scan Description Language (BSDL) is not available for this device.
- Emulation trace module enables non-intrusive, high-speed real-time tracing of instruction execution.
- Integrated PMU (Power Management Unit) automatically adjusts internal regulators to minimize power consumption during Sleep, Deep sleep, Power-down, and Deep power-down modes.
- Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
- Single 3.3 V power supply (2.4 V to 3.6 V).
- Four external interrupt inputs configurable as edge/level sensitive. All pins on Port 0 and Port 2 can be used as edge sensitive interrupt sources.
- Non-maskable Interrupt (NMI) input.
- Clock output function that can reflect the main oscillator clock, IRC clock, RTC clock, CPU clock, and the USB clock.
- The Wake-up Interrupt Controller (WIC) allows the CPU to automatically wake up from any priority interrupt that can occur while the clocks are stopped in deep sleep, Power-down, and Deep power-down modes.
- Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, USB activity, Ethernet wake-up interrupt, CAN bus activity, Port 0/2 pin interrupt, and NMI).
- Brownout detect with separate threshold for interrupt and forced reset.
- Power-On Reset (POR).
- Crystal oscillator with an operating range of 1 MHz to 25 MHz.
- 4 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
- PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the RTC oscillator.
- USB PLL for added flexibility.
- Code Read Protection (CRP) with different security levels.
- Unique device serial number for identification purposes.
- Available as LQFP100 (14 mm × 14 mm × 1.4 mm), TFBGA100[1] (9 mm × 9 mm × 0.7 mm), and WLCSP100 (5.07 × 5.07 × 0.53 mm) package.

1. LPC1768/65 only.

3. Applications

- eMetering
- Lighting
- Industrial networking
- Alarm systems
- White goods
- Motor control

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1769FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1768FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1768FET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1768UK	WLCSP100	wafer level chip-scale package; 100 balls; 5.07 × 5.07 × 0.53 mm	-
LPC1767FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1766FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1765FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1765FET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1764FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1763FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

4.1 Ordering options

Table 2. Ordering options

Type number	Device order part number	Flash (kB)	SRAM in kB				Ethernet	USB	CAN	I^2S	DAC	GPIO	Maximum CPU operating frequency (MHz)
			CPU	AHB SRAM0	AHB SRAM1	Total							
LPC1769FBD100	LPC1769FBD100,551	512	32	16	16	64	yes	Device/Host/OTG	2	yes	yes	70	120
LPC1768FBD100	LPC1768FBD100/CP32	512	32	16	16	64	yes	Device/Host/OTG	2	yes	yes	70	100
LPC1768FET100	LPC1768FET100Z	512	32	16	16	64	yes	Device/Host/OTG	2	yes	yes	70	100
LPC1768UK	LPC1768UKZ	512	32	16	16	64	yes	Device/Host/OTG	2	yes	yes	70	100
LPC1767FBD100	LPC1767FBD100,551	512	32	16	16	64	yes	no	no	yes	yes	70	100
LPC1766FBD100	LPC1766FBD100,551	256	32	16	16	64	yes	Device/Host/OTG	2	yes	yes	70	100
LPC1765FBD100	LPC1765FBD100/3271	256	32	16	16	64	no	Device/Host/OTG	2	yes	yes	70	100
LPC1765FET100	LPC1765FET100,551	256	32	16	16	64	no	Device/Host/OTG	2	yes	yes	70	100
LPC1764FBD100	LPC1764FBD100,551	128	16	16	-	32	yes	Device only	2	no	no	70	100
LPC1763FBD100	LPC1763FBD100K	256	32	16	16	64	no	no	no	yes	yes	70	100

5. Marking

The LPC176x devices typically have the following top-side marking:

LPC176xxxx

xxxxxxx

xxYYWWR[x]

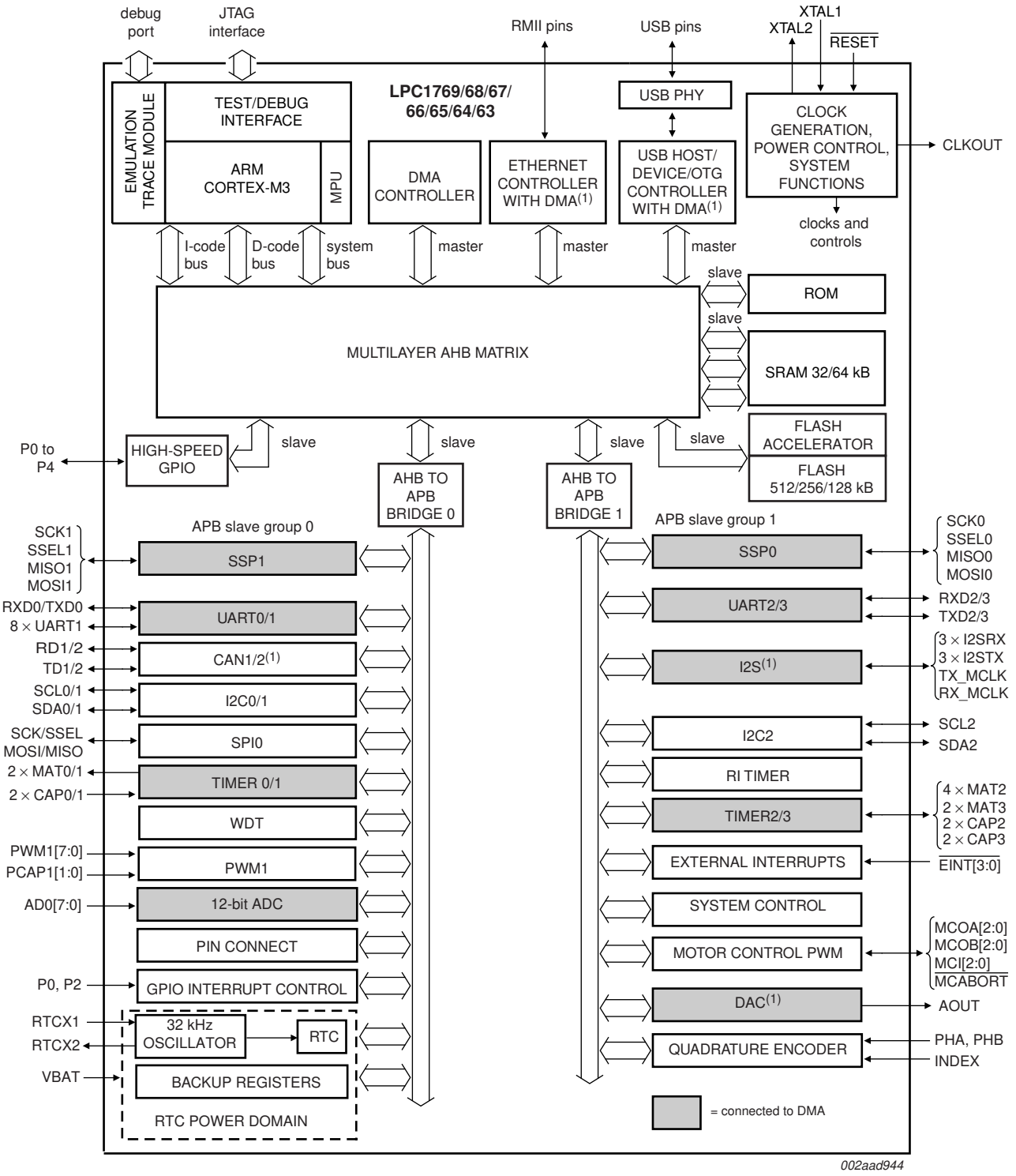
The last/second to last letter in the third line (field 'R') will identify the device revision. This data sheet covers the following revisions of the LPC176x:

Table 3. Device revision table

Revision identifier (R)	Revision description
'-'	Initial device revision
'A'	Second device revision
'B'	Third device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

6. Block diagram



(1) Not available on all parts. See Table 2.

Fig 1. Block diagram

7. Pinning information

7.1 Pinning

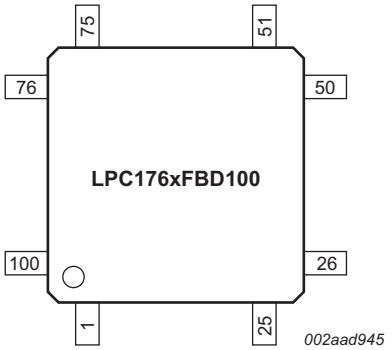


Fig 2. Pin configuration LQFP100 package

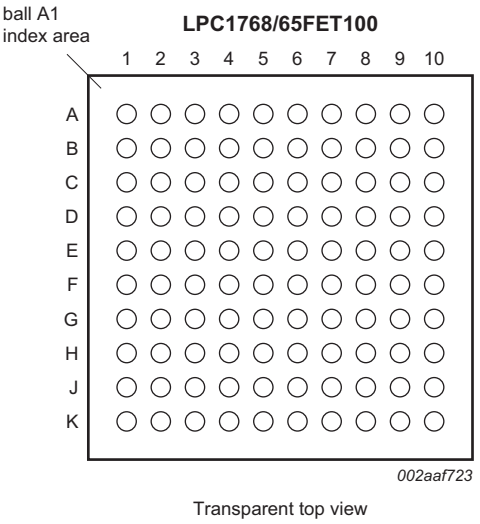


Fig 3. Pin configuration TFBGA100 package

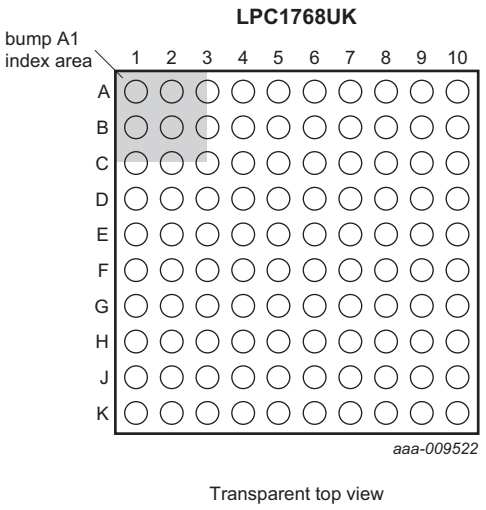


Fig 4. Pin configuration WLCSP100 package

Table 4. Pin allocation table TFBGA100

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
1	TDO/SWO	2	P0[3]/RXD0/AD0[6]	3	$V_{DD(3V3)}$	4	P1[4]/ENET_TX_EN
5	P1[10]/ENET_RXD1	6	P1[16]/ENET_MDC	7	$V_{DD(REG)(3V3)}$	8	P0[4]/I2SRX_CLK/ RD2/CAP2[0]
9	P0[7]/I2STX_CLK/ SCK1/MAT2[1]	10	P0[9]/I2STX_SDA/ MOSI1/MAT2[3]	11	-	12	-
Row B							
1	TMS/SWDIO	2	RTCK	3	V_{SS}	4	P1[1]/ENET_TXD1
5	P1[9]/ENET_RXD0	6	P1[17]/ ENET_MDIO	7	V_{SS}	8	P0[6]/I2SRX_SDA/ SSEL1/MAT2[0]
9	P2[0]/PWM1[1]/TXD1	10	P2[1]/PWM1[2]/RXD1	11	-	12	-
Row C							
1	TCK/SWDCLK	2	$\overline{\text{TRST}}$	3	TDI	4	P0[2]/TXD0/AD0[7]
5	P1[8]/ENET_CRS	6	P1[15]/ ENET_REF_CLK	7	P4[28]/RX_MCLK/ MAT2[0]/TXD3	8	P0[8]/I2STX_WS/ MISO1/MAT2[2]
9	V_{SS}	10	$V_{DD(3V3)}$	11	-	12	-
Row D							
1	P0[24]/AD0[1]/ I2SRX_WS/CAP3[1]	2	P0[25]/AD0[2]/ I2SRX_SDA/TXD3	3	P0[26]/AD0[3]/ AOUT/RXD3	4	n.c.
5	P1[0]/ENET_TXD0	6	P1[14]/ENET_RX_ER	7	P0[5]/I2SRX_WS/ TD2/CAP2[1]	8	P2[2]/PWM1[3]/ CTS1/TRACEDATA[3]
9	P2[4]/PWM1[5]/ DSR1/TRACEDATA[1]	10	P2[5]/PWM1[6]/ DTR1/TRACEDATA[0]	11	-	12	-
Row E							
1	V_{SSA}	2	V_{DDA}	3	VREFP	4	n.c.
5	P0[23]/AD0[0]/ I2SRX_CLK/CAP3[0]	6	P4[29]/TX_MCLK/ MAT2[1]/RXD3	7	P2[3]/PWM1[4]/ DCD1/TRACEDATA[2]	8	P2[6]/PCAP1[0]/ RI1/TRACECLK

Table 4. Pin allocation table TFBGA100 *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
9	P2[7]/RD2/RTS1	10	P2[8]/TD2/TXD2	11	-	12	-
Row F							
1	VREFN	2	RTCX1	3	$\overline{\text{RESET}}$	4	P1[31]/SCK1/ AD0[5]
5	P1[21]/$\overline{\text{MCABORT}}$/ PWM1[3]/SSEL0	6	P0[18]/DCD1/ MOSI0/MOSI	7	P2[9]/USB_CONNECT/ RXD2	8	P0[16]/RXD1/ SSEL0/SSEL
9	P0[17]/CTS1/ MISO0/MISO	10	P0[15]/TXD1/ SCK0/SCK	11	-	12	-
Row G							
1	RTCX2	2	VBAT	3	XTAL2	4	P0[30]/USB_D–
5	P1[25]/MCOA1/ MAT1[1]	6	P1[29]/MCOB2/ PCAP1[1]/MAT0[1]	7	V_{SS}	8	P0[21]/RI1/RD1
9	P0[20]/DTR1/SCL1	10	P0[19]/DSR1/SDA1	11	-	12	-
Row H							
1	P1[30]/V_{BUS}/ AD0[4]	2	XTAL1	3	P3[25]/MAT0[0]/ PWM1[2]	4	P1[18]/USB_UP_LED/ PWM1[1]/CAP1[0]
5	P1[24]/MCI2/ PWM1[5]/MOSI0	6	$V_{DD(REG)(3V3)}$	7	P0[10]/TXD2/ SDA2/MAT3[0]	8	P2[11]/$\overline{\text{EINT1}}$/ I2STX_CLK
9	$V_{DD(3V3)}$	10	P0[22]/RTS1/TD1	11	-	12	-

Table 4. Pin allocation table TFBGA100 *...continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row J							
1	P0[28]/SCL0/ USB_SCL	2	P0[27]/SDA0/ USB_SDA	3	P0[29]/USB_D+	4	P1[19]/MCOA0/ USB_PPWR/ CAP1[1]
5	P1[22]/MCOB0/ USB_PWRD/ MAT1[0]	6	V_{SS}	7	P1[28]/MCOA2/ PCAP1[0]/ MAT0[0]	8	P0[1]/TD1/RXD3/SCL1
9	P2[13]/EINT3/ I2STX_SDA	10	P2[10]/EINT0/NMI	11	-	12	-
Row K							
1	P3[26]/STCLK/ MAT0[1]/PWM1[3]	2	$V_{DD(3V3)}$	3	V_{SS}	4	P1[20]/MCI0/ PWM1[2]/SCK0
5	P1[23]/MCI1/ PWM1[4]/MISO0	6	P1[26]/MCOB1/ PWM1[6]/CAP0[0]	7	P1[27]/CLKOUT /USB_OVRCR/ CAP0[1]	8	P0[0]/RD1/TXD3/SDA1
9	P0[11]/RXD2/ SCL2/MAT3[1]	10	P2[12]/EINT2/ I2STX_WS	11	-	12	-

7.2 Pin description

Table 5. Pin description

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P0[0] to P0[31]					I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the pin connect block. Pins 12, 13, 14, and 31 of this port are not available.
P0[0]/RD1/TXD3/ SDA1	46	K8	H10	[1]	I/O	**P0[0] —** General purpose digital input/output pin.
					I	**RD1 —** CAN1 receiver input. (LPC1769/68/66/65/64 only).
					O	**TXD3 —** Transmitter output for UART3.
					I/O	**SDA1 —** I^2C1 data input/output. (This is not an I^2C-bus compliant open-drain pin).
P0[1]/TD1/RXD3/ SCL1	47	J8	H9	[1]	I/O	**P0[1] —** General purpose digital input/output pin.
					O	**TD1 —** CAN1 transmitter output. (LPC1769/68/66/65/64 only).
					I	**RXD3 —** Receiver input for UART3.
					I/O	**SCL1 —** I^2C1 clock input/output. (This is not an I^2C-bus compliant open-drain pin).
P0[2]/TXD0/AD0[7]	98	C4	B1	[2]	I/O	**P0[2] —** General purpose digital input/output pin.
					O	**TXD0 —** Transmitter output for UART0.
					I	**AD0[7] —** A/D converter 0, input 7.
P0[3]/RXD0/AD0[6]	99	A2	C3	[2]	I/O	**P0[3] —** General purpose digital input/output pin.
					I	**RXD0 —** Receiver input for UART0.
					I	**AD0[6] —** A/D converter 0, input 6.

Table 5. Pin description *…continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P0[4]/ I2SRX_CLK/ RD2/CAP2[0]	81	A8	G2	[1]	I/O	**P0[4] —** General purpose digital input/output pin.
					I/O	**I2SRX_CLK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I	**RD2 —** CAN2 receiver input. (LPC1769/68/66/65/64 only).
					I	**CAP2[0] —** Capture input for Timer 2, channel 0.
P0[5]/ I2SRX_WS/ TD2/CAP2[1]	80	D7	H1	[1]	I/O	**P0[5] —** General purpose digital input/output pin.
					I/O	**I2SRX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					O	**TD2 —** CAN2 transmitter output. (LPC1769/68/66/65/64 only).
					I	**CAP2[1] —** Capture input for Timer 2, channel 1.
P0[6]/ I2SRX_SDA/ SSEL1/MAT2[0]	79	B8	G3	[1]	I/O	**P0[6] —** General purpose digital input/output pin.
					I/O	**I2SRX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I/O	**SSEL1 —** Slave Select for SSP1.
					O	**MAT2[0] —** Match output for Timer 2, channel 0.
P0[7]/ I2STX_CLK/ SCK1/MAT2[1]	78	A9	J1	[1]	I/O	**P0[7] —** General purpose digital input/output pin.
					I/O	**I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I/O	**SCK1 —** Serial Clock for SSP1.
					O	**MAT2[1] —** Match output for Timer 2, channel 1.
P0[8]/ I2STX_WS/ MISO1/MAT2[2]	77	C8	H2	[1]	I/O	**P0[8] —** General purpose digital input/output pin.
					I/O	**I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I/O	**MISO1 —** Master In Slave Out for SSP1.
					O	**MAT2[2] —** Match output for Timer 2, channel 2.
P0[9]/ I2STX_SDA/ MOSI1/MAT2[3]	76	A10	H3	[1]	I/O	**P0[9] —** General purpose digital input/output pin.
					I/O	**I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I/O	**MOSI1 —** Master Out Slave In for SSP1.
					O	**MAT2[3] —** Match output for Timer 2, channel 3.
P0[10]/TXD2/ SDA2/MAT3[0]	48	H7	H8	[1]	I/O	**P0[10] —** General purpose digital input/output pin.
					O	**TXD2 —** Transmitter output for UART2.
					I/O	**SDA2 —** I²C2 data input/output (this is not an open-drain pin).
					O	**MAT3[0] —** Match output for Timer 3, channel 0.

Table 5. Pin description *…continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P0[11]/RXD2/ SCL2/MAT3[1]	49	K9	J10	[1]	I/O	**P0[11]** — General purpose digital input/output pin.
					I	**RXD2** — Receiver input for UART2.
					I/O	**SCL2** — I^2C2 clock input/output (this is not an open-drain pin).
					O	**MAT3[1]** — Match output for Timer 3, channel 1.
P0[15]/TXD1/ SCK0/SCK	62	F10	H6	[1]	I/O	**P0[15]** — General purpose digital input/output pin.
					O	**TXD1** — Transmitter output for UART1.
					I/O	**SCK0** — Serial clock for SSP0.
					I/O	**SCK** — Serial clock for SPI.
P0[16]/RXD1/ SSEL0/SSEL	63	F8	J5	[1]	I/O	**P0[16]** — General purpose digital input/output pin.
					I	**RXD1** — Receiver input for UART1.
					I/O	**SSEL0** — Slave Select for SSP0.
					I/O	**SSEL** — Slave Select for SPI.
P0[17]/CTS1/ MISO0/MISO	61	F9	K6	[1]	I/O	**P0[17]** — General purpose digital input/output pin.
					I	**CTS1** — Clear to Send input for UART1.
					I/O	**MISO0** — Master In Slave Out for SSP0.
					I/O	**MISO** — Master In Slave Out for SPI.
P0[18]/DCD1/ MOSI0/MOSI	60	F6	J6	[1]	I/O	**P0[18]** — General purpose digital input/output pin.
					I	**DCD1** — Data Carrier Detect input for UART1.
					I/O	**MOSI0** — Master Out Slave In for SSP0.
					I/O	**MOSI** — Master Out Slave In for SPI.
P0[19]/DSR1/ SDA1	59	G10	K7	[1]	I/O	**P0[19]** — General purpose digital input/output pin.
					I	**DSR1** — Data Set Ready input for UART1.
					I/O	**SDA1** — I^2C1 data input/output (this is not an I^2C-bus compliant open-drain pin).
P0[20]/DTR1/SCL1	58	G9	J7	[1]	I/O	**P0[20]** — General purpose digital input/output pin.
					O	**DTR1** — Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal.
					I/O	**SCL1** — I^2C1 clock input/output (this is not an I^2C-bus compliant open-drain pin).
P0[21]/RI1/RD1	57	G8	H7	[1]	I/O	**P0[21]** — General purpose digital input/output pin.
					I	**RI1** — Ring Indicator input for UART1.
					I	**RD1** — CAN1 receiver input. (LPC1769/68/66/65/64 only).
P0[22]/RTS1/TD1	56	H10	K8	[1]	I/O	**P0[22]** — General purpose digital input/output pin.
					O	**RTS1** — Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal.
					O	**TD1** — CAN1 transmitter output. (LPC1769/68/66/65/64 only).

Table 5. Pin description *…continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P0[23]/AD0[0]/ I2SRX_CLK/ CAP3[0]	9	E5	D5	[2]	I/O	**P0[23] —** General purpose digital input/output pin.
					I	**AD0[0] —** A/D converter 0, input 0.
					I/O	**I2SRX_CLK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I	**CAP3[0] —** Capture input for Timer 3, channel 0.
P0[24]/AD0[1]/ I2SRX_WS/ CAP3[1]	8	D1	B4	[2]	I/O	**P0[24] —** General purpose digital input/output pin.
					I	**AD0[1] —** A/D converter 0, input 1.
					I/O	**I2SRX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I	**CAP3[1] —** Capture input for Timer 3, channel 1.
P0[25]/AD0[2]/ I2SRX_SDA/ TXD3	7	D2	A3	[2]	I/O	**P0[25] —** General purpose digital input/output pin.
					I	**AD0[2] —** A/D converter 0, input 2.
					I/O	**I2SRX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					O	**TXD3 —** Transmitter output for UART3.
P0[26]/AD0[3]/ AOUT/RXD3	6	D3	C5	[3]	I/O	**P0[26] —** General purpose digital input/output pin.
					I	**AD0[3] —** A/D converter 0, input 3.
					O	**AOUT —** DAC output (LPC1769/68/67/66/65/63 only).
					I	**RXD3 —** Receiver input for UART3.
P0[27]/SDA0/ USB_SDA	25	J2	C8	[4]	I/O	**P0[27] —** General purpose digital input/output pin. Output is open-drain.
					I/O	**SDA0 —** I²C0 data input/output. Open-drain output (for I²C-bus compliance).
					I/O	**USB_SDA —** USB port I²C serial data (OTG transceiver, LPC1769/68/66/65 only).
P0[28]/SCL0/ USB_SCL	24	J1	B9	[4]	I/O	**P0[28] —** General purpose digital input/output pin. Output is open-drain.
					I/O	**SCL0 —** I²C0 clock input/output. Open-drain output (for I²C-bus compliance).
					I/O	**USB_SCL —** USB port I²C serial clock (OTG transceiver, LPC1769/68/66/65 only).
P0[29]/USB_D+	29	J3	B10	[5]	I/O	**P0[29] —** General purpose digital input/output pin.
					I/O	**USB_D+ —** USB bidirectional D+ line. (LPC1769/68/66/65/64 only).
P0[30]/USB_D−	30	G4	C9	[5]	I/O	**P0[30] —** General purpose digital input/output pin.
					I/O	**USB_D− —** USB bidirectional D− line. (LPC1769/68/66/65/64 only).

Table 5. Pin description *...continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P1[0] to P1[31]					I/O	**Port 1:** Port 1 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block. Pins 2, 3, 5, 6, 7, 11, 12, and 13 of this port are not available.
P1[0]/ ENET_TXD0	95	D5	C1	[1]	I/O	**P1[0] —** General purpose digital input/output pin.
					O	**ENET_TXD0 —** Ethernet transmit data 0. (LPC1769/68/67/66/64 only).
P1[1]/ ENET_TXD1	94	B4	C2	[1]	I/O	**P1[1] —** General purpose digital input/output pin.
					O	**ENET_TXD1 —** Ethernet transmit data 1. (LPC1769/68/67/66/64 only).
P1[4]/ ENET_TX_EN	93	A4	D2	[1]	I/O	**P1[4] —** General purpose digital input/output pin.
					O	**ENET_TX_EN —** Ethernet transmit data enable. (LPC1769/68/67/66/64 only).
P1[8]/ ENET_CRS	92	C5	D1	[1]	I/O	**P1[8] —** General purpose digital input/output pin.
					I	**ENET_CRS —** Ethernet carrier sense. (LPC1769/68/67/66/64 only).
P1[9]/ ENET_RXD0	91	B5	D3	[1]	I/O	**P1[9] —** General purpose digital input/output pin.
					I	**ENET_RXD0 —** Ethernet receive data. (LPC1769/68/67/66/64 only).
P1[10]/ ENET_RXD1	90	A5	E3	[1]	I/O	**P1[10] —** General purpose digital input/output pin.
					I	**ENET_RXD1 —** Ethernet receive data. (LPC1769/68/67/66/64 only).
P1[14]/ ENET_RX_ER	89	D6	E2	[1]	I/O	**P1[14] —** General purpose digital input/output pin.
					I	**ENET_RX_ER —** Ethernet receive error. (LPC1769/68/67/66/64 only).
P1[15]/ ENET_REF_CLK	88	C6	E1	[1]	I/O	**P1[15] —** General purpose digital input/output pin.
					I	**ENET_REF_CLK —** Ethernet reference clock. (LPC1769/68/67/66/64 only).
P1[16]/ ENET_MDC	87	A6	F3	[1]	I/O	**P1[16] —** General purpose digital input/output pin.
					O	**ENET_MDC —** Ethernet MIIM clock (LPC1769/68/67/66/64 only).
P1[17]/ ENET_MDIO	86	B6	F2	[1]	I/O	**P1[17] —** General purpose digital input/output pin.
					I/O	**ENET_MDIO —** Ethernet MIIM data input and output. (LPC1769/68/67/66/64 only).

Table 5. Pin description *...continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P1[18]/ USB_UP_LED/ PWM1[1]/ CAP1[0]	32	H4	D9	[1]	I/O	**P1[18]** — General purpose digital input/output pin.
					O	**USB_UP_LED** — USB GoodLink LED indicator. It is LOW when the device is configured (non-control endpoints enabled), or when the host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when the host is enabled and detects activity on the bus. (LPC1769/68/66/65/64 only).
					O	**PWM1[1]** — Pulse Width Modulator 1, channel 1 output.
					I	**CAP1[0]** — Capture input for Timer 1, channel 0.
P1[19]/MCOA0/ USB_PPWR/ CAP1[1]	33	J4	C10	[1]	I/O	**P1[19]** — General purpose digital input/output pin.
					O	**MCOA0** — Motor control PWM channel 0, output A.
					O	**USB_PPWR** — Port Power enable signal for USB port. (LPC1769/68/66/65 only).
					I	**CAP1[1]** — Capture input for Timer 1, channel 1.
P1[20]/MCI0/ PWM1[2]/SCK0	34	K4	E8	[1]	I/O	**P1[20]** — General purpose digital input/output pin.
					I	**MCI0** — Motor control PWM channel 0, input. Also Quadrature Encoder Interface PHA input.
					O	**PWM1[2]** — Pulse Width Modulator 1, channel 2 output.
					I/O	**SCK0** — Serial clock for SSP0.
P1[21]/MCABORT/ PWM1[3]/ SSEL0	35	F5	E9	[1]	I/O	**P1[21]** — General purpose digital input/output pin.
					O	**MCABORT** — Motor control PWM, LOW-active fast abort.
					O	**PWM1[3]** — Pulse Width Modulator 1, channel 3 output.
					I/O	**SSEL0** — Slave Select for SSP0.
P1[22]/MCOB0/ USB_PWRD/ MAT1[0]	36	J5	D10	[1]	I/O	**P1[22]** — General purpose digital input/output pin.
					O	**MCOB0** — Motor control PWM channel 0, output B.
					I	**USB_PWRD** — Power Status for USB port (host power switch, LPC1769/68/66/65 only).
					O	**MAT1[0]** — Match output for Timer 1, channel 0.
P1[23]/MCI1/ PWM1[4]/MISO0	37	K5	E7	[1]	I/O	**P1[23]** — General purpose digital input/output pin.
					I	**MCI1** — Motor control PWM channel 1, input. Also Quadrature Encoder Interface PHB input.
					O	**PWM1[4]** — Pulse Width Modulator 1, channel 4 output.
					I/O	**MISO0** — Master In Slave Out for SSP0.
P1[24]/MCI2/ PWM1[5]/MOSI0	38	H5	F8	[1]	I/O	**P1[24]** — General purpose digital input/output pin.
					I	**MCI2** — Motor control PWM channel 2, input. Also Quadrature Encoder Interface INDEX input.
					O	**PWM1[5]** — Pulse Width Modulator 1, channel 5 output.
					I/O	**MOSI0** — Master Out Slave in for SSP0.

Table 5. Pin description *…continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P1[25]/MCOA1/ MAT1[1]	39	G5	F9	[1]	I/O	**P1[25]** — General purpose digital input/output pin.
					O	**MCOA1** — Motor control PWM channel 1, output A.
					O	**MAT1[1]** — Match output for Timer 1, channel 1.
P1[26]/MCOB1/ PWM1[6]/CAP0[0]	40	K6	E10	[1]	I/O	**P1[26]** — General purpose digital input/output pin.
					O	**MCOB1** — Motor control PWM channel 1, output B.
					O	**PWM1[6]** — Pulse Width Modulator 1, channel 6 output.
					I	**CAP0[0]** — Capture input for Timer 0, channel 0.
P1[27]/CLKOUT /USB_OVRCR/ CAP0[1]	43	K7	G9	[1]	I/O	**P1[27]** — General purpose digital input/output pin.
					O	**CLKOUT** — Clock output pin.
					I	**USB_OVRCR** — USB port Over-Current status. (LPC1769/68/66/65 only).
					I	**CAP0[1]** — Capture input for Timer 0, channel 1.
P1[28]/MCOA2/ PCAP1[0]/ MAT0[0]	44	J7	G10	[1]	I/O	**P1[28]** — General purpose digital input/output pin.
					O	**MCOA2** — Motor control PWM channel 2, output A.
					I	**PCAP1[0]** — Capture input for PWM1, channel 0.
					O	**MAT0[0]** — Match output for Timer 0, channel 0.
P1[29]/MCOB2/ PCAP1[1]/ MAT0[1]	45	G6	G8	[1]	I/O	**P1[29]** — General purpose digital input/output pin.
					O	**MCOB2** — Motor control PWM channel 2, output B.
					I	**PCAP1[1]** — Capture input for PWM1, channel 1.
					O	**MAT0[1]** — Match output for Timer 0, channel 1.
P1[30]/V_{BUS}/ AD0[4]	21	H1	B8	[2]	I/O	**P1[30]** — General purpose digital input/output pin.
					I	**V_{BUS}** — Monitors the presence of USB bus power. (LPC1769/68/66/65/64 only). **Note:** This signal must be HIGH for USB reset to occur.
					I	**AD0[4]** — A/D converter 0, input 4.
P1[31]/SCK1/ AD0[5]	20	F4	C7	[2]	I/O	**P1[31]** — General purpose digital input/output pin.
					I/O	**SCK1** — Serial Clock for SSP1.
					I	**AD0[5]** — A/D converter 0, input 5.
P2[0] to P2[31]					I/O	**Port 2:** Port 2 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the pin connect block. Pins 14 through 31 of this port are not available.
P2[0]/PWM1[1]/ TXD1	75	B9	K1	[1]	I/O	**P2[0]** — General purpose digital input/output pin.
					O	**PWM1[1]** — Pulse Width Modulator 1, channel 1 output.
					O	**TXD1** — Transmitter output for UART1.
P2[1]/PWM1[2]/ RXD1	74	B10	J2	[1]	I/O	**P2[1]** — General purpose digital input/output pin.
					O	**PWM1[2]** — Pulse Width Modulator 1, channel 2 output.
					I	**RXD1** — Receiver input for UART1.

Table 5. Pin description *...continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P2[2]/PWM1[3]/ CTS1/ TRACEDATA[3]	73	D8	K2	[1]	I/O	**P2[2]** — General purpose digital input/output pin.
					O	**PWM1[3]** — Pulse Width Modulator 1, channel 3 output.
					I	**CTS1** — Clear to Send input for UART1.
					O	**TRACEDATA[3]** — Trace data, bit 3.
P2[3]/PWM1[4]/ DCD1/ TRACEDATA[2]	70	E7	K3	[1]	I/O	**P2[3]** — General purpose digital input/output pin.
					O	**PWM1[4]** — Pulse Width Modulator 1, channel 4 output.
					I	**DCD1** — Data Carrier Detect input for UART1.
					O	**TRACEDATA[2]** — Trace data, bit 2.
P2[4]/PWM1[5]/ DSR1/ TRACEDATA[1]	69	D9	J3	[1]	I/O	**P2[4]** — General purpose digital input/output pin.
					O	**PWM1[5]** — Pulse Width Modulator 1, channel 5 output.
					I	**DSR1** — Data Set Ready input for UART1.
					O	**TRACEDATA[1]** — Trace data, bit 1.
P2[5]/PWM1[6]/ DTR1/ TRACEDATA[0]	68	D10	H4	[1]	I/O	**P2[5]** — General purpose digital input/output pin.
					O	**PWM1[6]** — Pulse Width Modulator 1, channel 6 output.
					O	**DTR1** — Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal.
					O	**TRACEDATA[0]** — Trace data, bit 0.
P2[6]/PCAP1[0]/ RI1/TRACECLK	67	E8	K4	[1]	I/O	**P2[6]** — General purpose digital input/output pin.
					I	**PCAP1[0]** — Capture input for PWM1, channel 0.
					I	**RI1** — Ring Indicator input for UART1.
					O	**TRACECLK** — Trace Clock.
P2[7]/RD2/ RTS1	66	E9	J4	[1]	I/O	**P2[7]** — General purpose digital input/output pin.
					I	**RD2** — CAN2 receiver input. (LPC1769/68/66/65/64 only).
					O	**RTS1** — Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal.
P2[8]/TD2/ TXD2	65	E10	H5	[1]	I/O	**P2[8]** — General purpose digital input/output pin.
					O	**TD2** — CAN2 transmitter output. (LPC1769/68/66/65/64 only).
					O	**TXD2** — Transmitter output for UART2.
P2[9]/ USB_CONNECT/ RXD2	64	F7	K5	[1]	I/O	**P2[9]** — General purpose digital input/output pin.
					O	**USB_CONNECT** — Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature. (LPC1769/68/66/65/64 only).
					I	**RXD2** — Receiver input for UART2.
P2[10]/$\overline{\text{EINT0}}$/NMI	53	J10	K9	[6]	I/O	**P2[10]** — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
					I	**$\overline{\text{EINT0}}$** — External interrupt 0 input.
					I	**NMI** — Non-maskable interrupt input.

Table 5. Pin description *...continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P2[11]/EINT1/ I2STX_CLK	52	H8	J8	[6]	I/O	**P2[11]** — General purpose digital input/output pin.
					I	**EINT1** — External interrupt 1 input.
					I/O	**I2STX_CLK** — Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
P2[12]/EINT2/ I2STX_WS	51	K10	K10	[6]	I/O	**P2[12]** — General purpose digital input/output pin.
					I	**EINT2** — External interrupt 2 input.
					I/O	**I2STX_WS** — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
P2[13]/EINT3/ I2STX_SDA	50	J9	J9	[6]	I/O	**P2[13]** — General purpose digital input/output pin.
					I	**EINT3** — External interrupt 3 input.
					I/O	**I2STX_SDA** — Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
P3[0] to P3[31]					I/O	**Port 3:** Port 3 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the pin connect block. Pins 0 through 24, and 27 through 31 of this port are not available.
P3[25]/MAT0[0]/ PWM1[2]	27	H3	D8	[1]	I/O	**P3[25]** — General purpose digital input/output pin.
					O	**MAT0[0]** — Match output for Timer 0, channel 0.
					O	**PWM1[2]** — Pulse Width Modulator 1, output 2.
P3[26]/STCLK/ MAT0[1]/PWM1[3]	26	K1	A10	[1]	I/O	**P3[26]** — General purpose digital input/output pin.
					I	**STCLK** — System tick timer clock input. The maximum STCLK frequency is 1/4 of the Arm processor clock frequency CCLK.
					O	**MAT0[1]** — Match output for Timer 0, channel 1.
					O	**PWM1[3]** — Pulse Width Modulator 1, output 3.
P4[0] to P4[31]					I/O	**Port 4:** Port 4 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 4 pins depends upon the pin function selected via the pin connect block. Pins 0 through 27, 30, and 31 of this port are not available.
P4[28]/RX_MCLK/ MAT2[0]/TXD3	82	C7	G1	[1]	I/O	**P4[28]** — General purpose digital input/output pin.
					O	**RX_MCLK** — I²S receive master clock. (LPC1769/68/67/66/65 only).
					O	**MAT2[0]** — Match output for Timer 2, channel 0.
					O	**TXD3** — Transmitter output for UART3.
P4[29]/TX_MCLK/ MAT2[1]/RXD3	85	E6	F1	[1]	I/O	**P4[29]** — General purpose digital input/output pin.
					O	**TX_MCLK** — I²S transmit master clock. (LPC1769/68/67/66/65 only).
					O	**MAT2[1]** — Match output for Timer 2, channel 1.
					I	**RXD3** — Receiver input for UART3.

Table 5. Pin description *...continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
TDO/SWO	1	A1	A1	[7]	O	**TDO —** Test Data out for JTAG interface.
					O	**SWO —** Serial wire trace output.
TDI	2	C3	C4	[1][8]	I	**TDI —** Test Data in for JTAG interface.
TMS/SWDIO	3	B1	B3	[1][8]	I	**TMS —** Test Mode Select for JTAG interface.
					I/O	**SWDIO —** Serial wire debug data input/output.
$\overline{\text{TRST}}$	4	C2	A2	[1][8]	I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
TCK/SWDCLK	5	C1	D4	[7]	I	**TCK —** Test Clock for JTAG interface.
					I	**SWDCLK —** Serial wire clock.
RTCK	100	B2	B2	[7]	O	**RTCK —** JTAG interface control signal.
$\overline{\text{RSTOUT}}$	14	-	-	-	O	**$\overline{\text{RSTOUT}}$ —** This is a 3.3 V pin. LOW on this pin indicates the microcontroller being in Reset state.
$\overline{\text{RESET}}$	17	F3	C6	[9]	I	**External reset input:** A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	22	H2	D7	[10][11]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	23	G3	A9	[10][11]	O	Output from the oscillator amplifier.
RTCX1	16	F2	A7	[10][11]	I	Input to the RTC oscillator circuit.
RTCX2	18	G1	B7	[10]	O	Output from the RTC oscillator circuit.
V_{SS}	31, 41, 55, 72, 83, 97	B3, B7, C9, G7, J6, K3	E5, F5, F6, G5, G6, G7	[10]	I	**ground:** 0 V reference.
V_{SSA}	11	E1	B5	[10]	I	**analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{DD(3V3)}$	28, 54, 71, 96	K2, H9, C10, A3	E4, E6, F7, G4	[10]	I	**3.3 V supply voltage:** This is the power supply voltage for the I/O ports.
$V_{DD(REG)(3V3)}$	42, 84	H6, A7	F4, F10	[10]	I	**3.3 V voltage regulator supply voltage:** This is the supply voltage for the on-chip voltage regulator only.
V_{DDA}	10	E2	A4	[10]	I	**analog 3.3 V pad supply voltage:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. This voltage is used to power the ADC and DAC. This pin should be tied to 3.3 V if the ADC and DAC are not used.
VREFP	12	E3	A5	[10]	I	**ADC positive reference voltage:** This should be nominally the same voltage as V_{DDA} but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC and DAC. This pin should be tied to 3.3 V if the ADC and DAC are not used.

Table 5. Pin description *…continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
VREFN	15	F1	A6		I	**ADC negative reference voltage:** This should be nominally the same voltage as V_{SS} but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC and DAC.
VBAT	19	G2	A8	[10][12]	I	**RTC pin power supply:** 3.3 V on this pin supplies the power to the RTC peripheral.
n.c.	13	D4, E4	B6, D6		-	not connected.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis. This pin is pulled up to a voltage level of 2.3 V to 2.6 V.

[2] 5 V tolerant pad providing digital I/O functions (with TTL levels and hysteresis) and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant. This pin is pulled up to a voltage level of 2.3 V to 2.6 V.

[3] 5 V tolerant pad providing digital I/O with TTL levels and hysteresis and analog output function. When configured as the DAC output, digital section of the pad is disabled. This pin is pulled up to a voltage level of 2.3 V to 2.6 V.

[4] Open-drain 5 V tolerant digital I/O pad, compatible with I^2C-bus 400 kHz specification. This pad requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I^2C-bus is floating and does not disturb the I^2C lines. Open-drain configuration applies to all functions on this pin.

[5] Pad provides digital I/O and USB functions. It is designed in accordance with the *USB specification, revision 2.0* (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[6] 5 V tolerant pad with 10 ns glitch filter providing digital I/O functions with TTL levels and hysteresis. This pin is pulled up to a voltage level of 2.3 V to 2.6 V.

[7] 5 V tolerant pad with TTL levels and hysteresis. Internal pull-up and pull-down resistors disabled.

[8] 5 V tolerant pad with TTL levels and hysteresis and internal pull-up resistor.

[9] 5 V tolerant pad with 20 ns glitch filter providing digital I/O function with TTL levels and hysteresis.

[10] Pad provides special analog functionality. A 32 kHz crystal oscillator must be used with the RTC.

[11] When the system oscillator is not used, connect XTAL1 and XTAL2 as follows: XTAL1 can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTAL2 should be left floating.

[12] When the RTC is not used, connect VBAT to $V_{DD(REG)(3V3)}$ and leave RTCX1 floating.

8. Functional description

8.1 Architectural overview

Remark: In the following, the notation LPC17xx refers to all parts: LPC1769/68/67/66/65/64/63.

The Arm Cortex-M3 includes three AHB-Lite buses: the system bus, the I-code bus, and the D-code bus (see Figure 1). The I-code and D-code core buses are faster than the system bus and are used similarly to TCM interfaces: one bus dedicated for instruction fetch (I-code) and one bus for data access (D-code). The use of two core buses allows for simultaneous operations if concurrent operations target different devices.

The LPC17xx use a multi-layer AHB matrix to connect the Arm Cortex-M3 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slaves ports of the matrix to be accessed simultaneously by different bus masters.

8.2 Arm Cortex-M3 processor

The Arm Cortex-M3 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The Arm Cortex-M3 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware divide, interruptible/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The Arm Cortex-M3 processor is described in detail in the *Cortex-M3 Technical Reference Manual* that can be found on official Arm website.

8.3 On-chip flash program memory

The LPC17xx contain up to 512 kB of on-chip flash memory. A new two-port flash accelerator maximizes performance for use with the two fast AHB-Lite buses.

8.4 On-chip SRAM

The LPC17xx contain a total of 64 kB on-chip static RAM memory. This includes the main 32 kB SRAM, accessible by the CPU and DMA controller on a higher-speed bus, and two additional 16 kB each SRAM blocks situated on a separate slave port on the AHB multilayer matrix.

This architecture allows CPU and DMA accesses to be spread over three separate RAMs that can be accessed simultaneously.

8.5 Memory Protection Unit (MPU)

The LPC17xx have a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application.

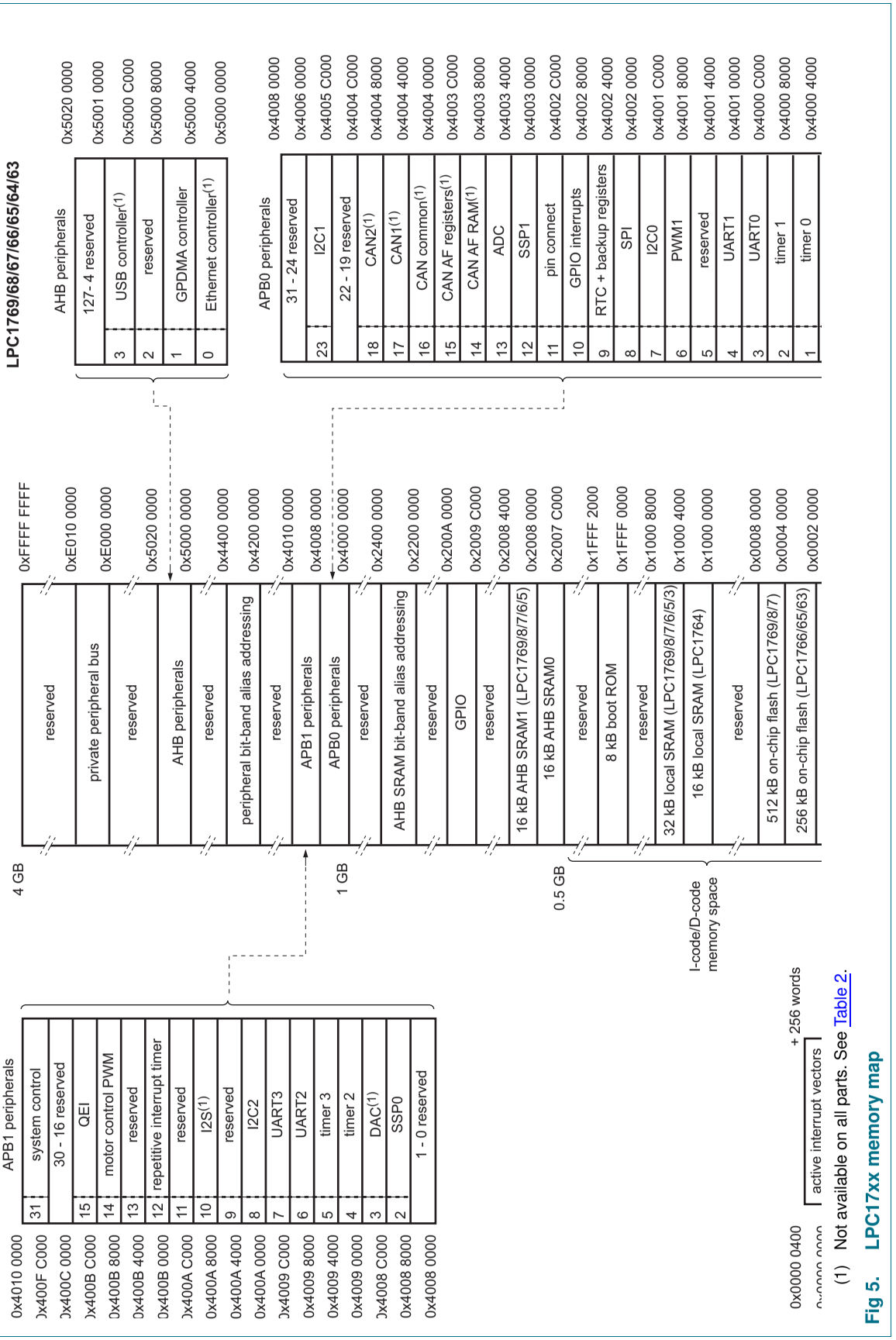
The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to 8 regions each of which can be divided into 8 subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

8.6 Memory map

The LPC17xx incorporates several distinct memory regions, shown in the following figures. Figure 5 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB peripheral area is 1 MB in size and is divided to allow for up to 64 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.



(1) Not available on all parts. See Table 2.

Fig 5. LPC17xx memory map

8.7 Nested Vectored Interrupt Controller (NVIC)

The NVIC is an integral part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.7.1 Features

- Controls system exceptions and peripheral interrupts
- In the LPC17xx, the NVIC supports 33 vectored interrupts
- 32 programmable interrupt priority levels, with hardware priority level masking
- Relocatable vector table
- Non-Maskable Interrupt (NMI)
- Software interrupt generation

8.7.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any pin on Port 0 and Port 2 (total of 42 pins) regardless of the selected function, can be programmed to generate an interrupt on a rising edge, a falling edge, or both.

8.8 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

Most pins can also be configured as open-drain outputs or to have a pull-up, pull-down, or no resistor enabled.

8.9 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the AHB master. The GPDMA controller allows data transfers between the USB and Ethernet controllers and the various on-chip SRAM areas. The supported APB peripherals are SSP0/1, all UARTs, the I^2S-bus interface, the ADC, and the DAC. Two match signals for each timer can be used to trigger DMA transfers.

Remark: The Ethernet controller is available on parts LPC1769/68/67/66/64. The USB controller is available on parts LPC1769/68/66/65/64. The I^2S-bus interface is available on parts LPC1769/68/67/66/65. The DAC is available on parts LPC1769/68/67/66/65/63.

8.9.1 Features

- Eight DMA channels. Each channel can support an unidirectional transfer.
- 16 DMA request lines.
- Single DMA and burst DMA request signals. Each peripheral connected to the DMA Controller can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the DMA Controller.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers are supported.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority.
- AHB slave DMA programming interface. The DMA Controller is programmed by writing to the DMA control registers over the AHB slave interface.
- One AHB bus master for transferring data. The interface transfers data when a DMA request goes active.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data.
- Internal four-word FIFO per channel.
- Supports 8, 16, and 32-bit wide transactions.
- Big-endian and little-endian support. The DMA Controller defaults to little-endian mode on reset.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

8.10 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

LPC17xx use accelerated GPIO functions:

- GPIO registers are accessed through the AHB multilayer bus so that the fastest possible I/O timing can be achieved.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte and half-word addressable.
- Entire port value can be written in one instruction.
- Support for Cortex-M3 bit banding.
- Support for use with the GPDMA controller.