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EM773 User manual

Rev. 2 — 7 December 2011 User manual

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2	20111207	• Section 3.6 “Start-up behavior” added. • Section 3.4.34 “Device ID register”: Added device ID for EM773FHN33/302. • Section 19.4.11 “Read Part Identification number (UART ISP)”: Added device ID for EM773FHN33/302. • Table 76; added “Pin is 5 V tolerant” to Table note 2. • Table 129 “Master Transmitter mode”; for 0x10, changed “SLA+W” to “SLA+R”. • Chapter 16 “EM773 System tick timer”; description of system tick timer updated. • Chapter 16 “EM773 Metrology engine”; corrected Equation 14. • Chapter 18 “EM773 Flash memory programming firmware”; changed format of command code throughout. • Single-cycle hardware multiply specified in Table 265. • Added Chapter 15 “EM773 Power profiles”. • Updated Chapter 14 “EM773 WatchDog Timer (WDT)”. • Updated Chapter 6 “EM773 I/O Configuration”.
1	20100910	Initial version

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1.1 Introduction

The EM773 is an ARM Cortex-M0 based, low-cost 32-bit energy metering IC, designed for 8/16-bit smart metering applications. The EM773 offers programmability and on-chip metrology functionality combined with a low power, simple instruction set and memory addressing with reduced code size compared to existing 8/16-bit architectures.

The EM773 operates at CPU frequencies of up to 48 MHz.

The peripheral complement of the EM773 includes up to 32 kB of flash memory, up to 8 kB of data memory, one Fast-mode Plus I^2C-bus interface, one RS-485/EIA-485 UART, one SPI interface with SSP features, three general purpose timers, a metrology engine, and up to 25 general purpose I/O pins.

1.2 Features

- System:
  - ARM Cortex-M0 processor, running at frequencies of up to 48 MHz.
  - ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
  - Serial Wire Debug.
  - System tick timer.
- Memory:
  - 32 kB on-chip flash programming memory.
  - 8 kB SRAM.
  - In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
- Digital peripherals:
  - Up to 25 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors.
  - GPIO pins can be used as edge and level sensitive interrupt sources.
  - High-current output driver (20 mA) on one pin.
  - High-current sink drivers (20 mA) on two I^2C-bus pins in Fast-mode Plus.
  - Three general purpose timers/counters with a total of two capture inputs and 10 match outputs.
  - Programmable WatchDog Timer (WDT).
- Analog peripherals:
  - Metrology Engine for Smart Metering with two current inputs and a voltage input.

- Serial interfaces:
  - UART with fractional baud rate generation, internal FIFO, and RS-485 support.
  - One SPI controller with SSP features and with FIFO and multi-protocol capabilities.
  - I^2C-bus interface supporting full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Programmable watchdog oscillator with a frequency range of 7.8 kHz to 1.8 MHz.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
  - Clock output function with divider that can reflect the system oscillator clock, IRC clock, CPU clock, and the Watchdog clock.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, and Deep power-down modes.
  - Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.
  - Processor wake-up from Deep-sleep mode via a dedicated start logic using up to 11 of the functional pins.
  - Power-On Reset (POR).
  - Brownout detect with four separate thresholds for interrupt and forced reset.
- Unique device serial number for identification.
- Single 3.3 V power supply (1.8 V to 3.6 V).
- Available as 33-pin HVQFN package.

1.3 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
EM773FHN33	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm	n/a

1.4 Block diagram

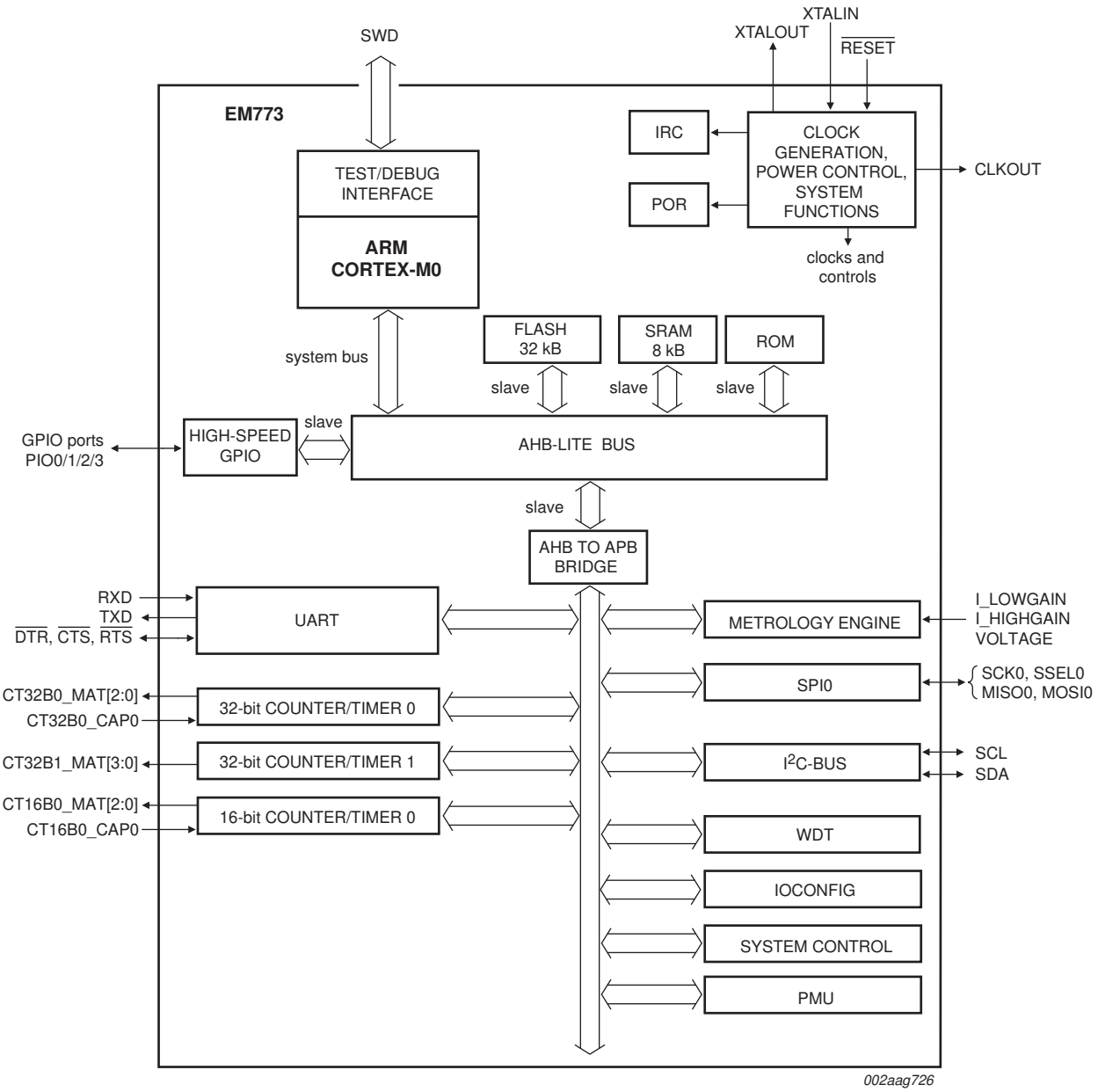

Fig 1. EM773 block diagram

1.5 ARM Cortex-M0 processor

The ARM Cortex-M0 processor is described in detail in Section 21.2 “About the Cortex-M0 processor and core peripherals”. For the EM773, the ARM Cortex-M0 processor core is configured as follows:

- System options:
  - The Nested Vectored Interrupt Controller (NVIC) is included and supports up to 32 interrupts.
  - The system tick timer is included.
- Debug options: Serial Wire Debug is included with two watchpoints and four breakpoints.

2.1 Memory map

Figure 2 shows the memory and peripheral address space of the EM773.

The AHB peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. On the EM773, the GPIO ports are the only AHB peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

All peripheral register addresses are 32-bit word aligned regardless of their size. An implication of this is that word and half-word registers must be accessed all at once. For example, it is not possible to read or write the upper byte of a word register separately.

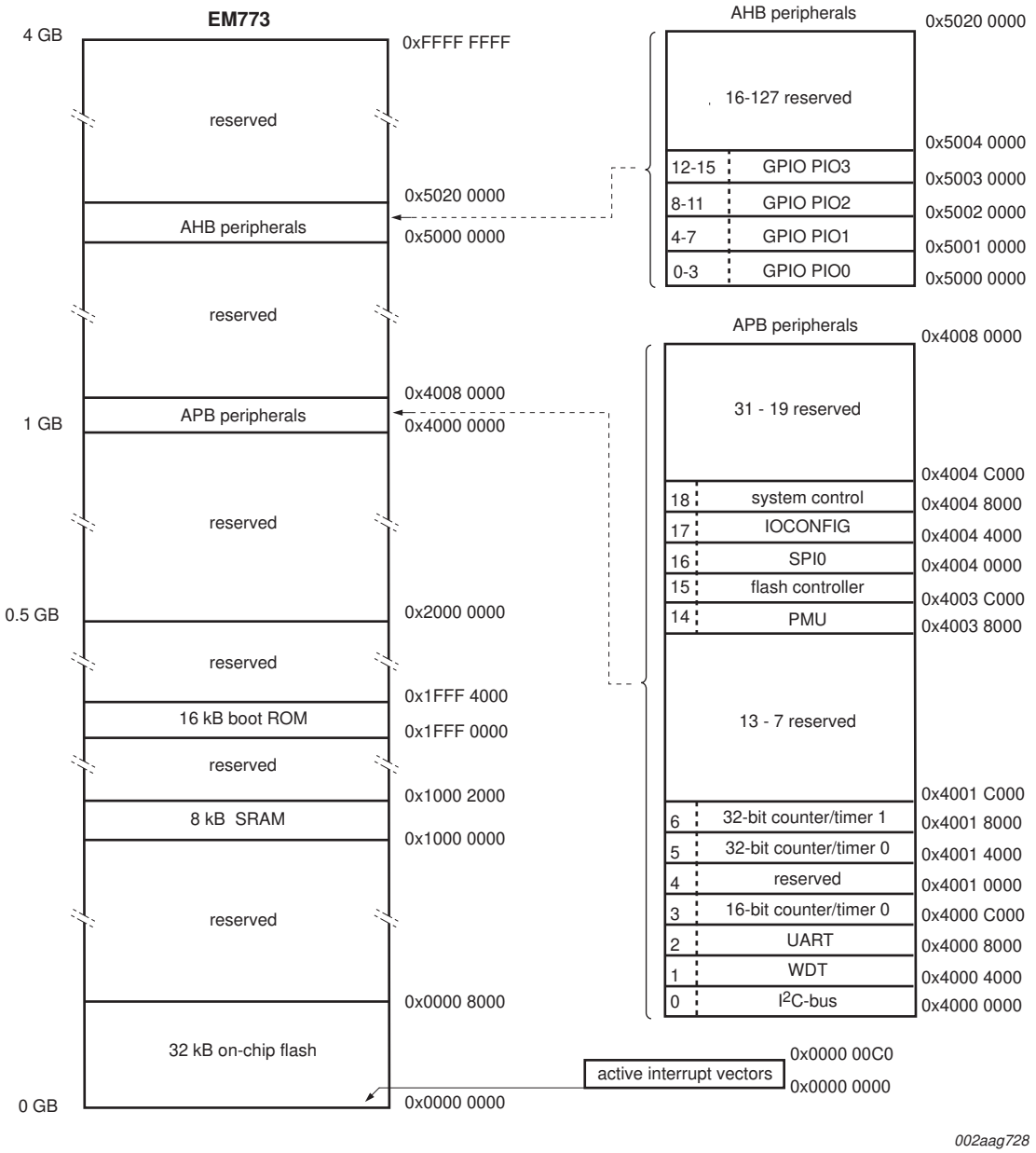

Fig 2. EM773 memory map

3.1 Introduction

The system configuration block controls oscillators, start logic, and clock generation of the EM773. Also included in this block are registers for setting the priority for AHB access and a register for remapping flash, SRAM, and ROM memory areas.

3.2 Pin description

Table 2 shows pins that are associated with system control block functions.

Table 2. Pin summary

Pin name	Pin direction	Pin description
CLKOUT	O	Clockout pin
PIO0_0 to PIO0_10	I	Start logic wake-up pins port 0

3.3 Clocking and power control

See Figure 3 for an overview of the EM773 Clock Generation Unit (CGU).

The EM773 includes three independent oscillators. These are the system oscillator, the Internal RC oscillator (IRC), and the watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the EM773 will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

The SYSAHBCLKCTRL register gates the system clock to the various peripherals and memories. UART, the WDT, and SPI0 have individual clock dividers to derive peripheral clocks from the main clock.

The main clock and the clock outputs from the IRC, the system oscillator, and the watchdog oscillator can be observed directly on the CLKOUT pin.

For details on power control see Section 3.8.

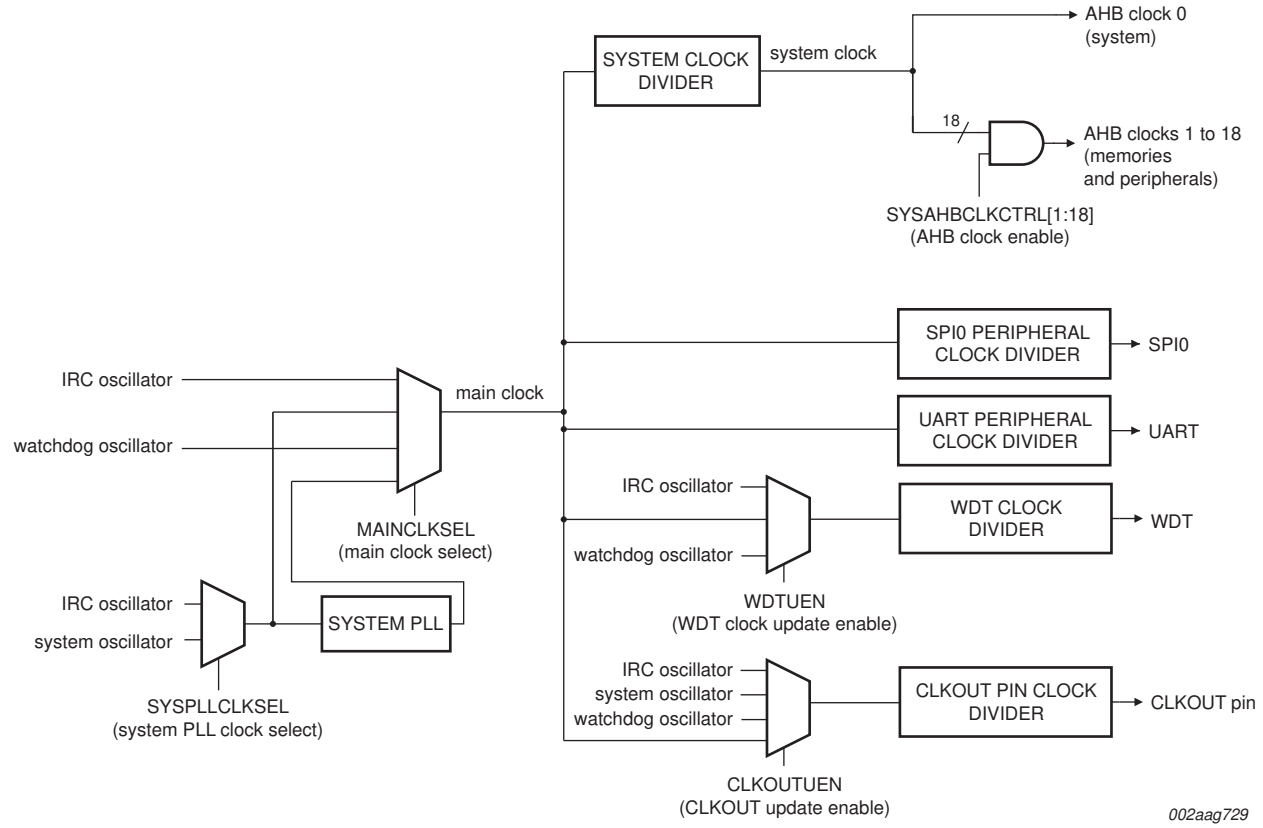

Fig 3. EM773 CGU block diagram

3.4 Register description

All registers, regardless of size, are on word address boundaries. Details of the registers appear in the description of each function.

See Section 3.11 for the flash access timing register, which can be re-configured as part the system setup. This register is not part of the system configuration block.

Table 3. Register overview: system control block (base address 0x4004 8000)

Name	Access	Address offset	Description	Reset value	Reference
SYSMEMREMAP	R/W	0x000	System memory remap	0x002	Table 4
PRESETCTRL	R/W	0x004	Peripheral reset control	0x000	Table 5
SYSPLLCTRL	R/W	0x008	System PLL control	0x000	Table 6
SYSPLLSTAT	R	0x00C	System PLL status	0x000	Table 7
-	-	0x010 - 0x01C	Reserved	-	-
SYSOSCCTRL	R/W	0x020	System oscillator control	0x000	Table 8
WDTOSCCTRL	R/W	0x024	Watchdog oscillator control	0x000	Table 9
IRCCTRL	R/W	0x028	IRC control	0x080	Table 10
-	-	0x02C	Reserved	-	-

Table 3. Register overview: system control block (base address 0x4004 8000) *...continued*

Name	Access	Address offset	Description	Reset value	Reference
SYSRSTSTAT	R	0x030	System reset status register	0x000	Table 11
-	-	0x034 - 0x03C	Reserved	-	-
SYSPLLCLKSEL	R/W	0x040	System PLL clock source select	0x000	Table 12
SYSPLLCLKUEN	R/W	0x044	System PLL clock source update enable	0x000	Table 13
-	-	0x048 - 0x06C	Reserved	-	-
MAINCLKSEL	R/W	0x070	Main clock source select	0x000	Table 14
MAINCLKUEN	R/W	0x074	Main clock source update enable	0x000	Table 15
SYSAHBCLKDIV	R/W	0x078	System AHB clock divider	0x001	Table 16
-	-	0x07C	Reserved	-	-
SYSAHBCLKCTRL	R/W	0x080	System AHB clock control	0x85F	Table 17
-	-	0x084 - 0x090	Reserved	-	-
SSP0CLKDIV	R/W	0x094	SPI0 clock divider	0x000	Table 18
UARTCLKDIV	R/W	0x098	UART clock divider	0x000	Table 19
-	-	0x0A0-0x0CC	Reserved	-	-
WDTCLKSEL	R/W	0x0D0	WDT clock source select	0x000	Table 20
WDTCLKUEN	R/W	0x0D4	WDT clock source update enable	0x000	Table 21
WDTCLKDIV	R/W	0x0D8	WDT clock divider	0x000	Table 22
-	-	0x0DC	Reserved	-	-
CLKOUTCLKSEL	R/W	0x0E0	CLKOUT clock source select	0x000	Table 23
CLKOUTUEN	R/W	0x0E4	CLKOUT clock source update enable	0x000	Table 24
CLKOUTDIV	R/W	0x0E8	CLKOUT clock divider	0x000	Table 25
-	-	0x0EC - 0x0FC	Reserved	-	-
PIOPORCAP0	R	0x100	POR captured PIO status 0	user dependent	Table 26
PIOPORCAP1	R	0x104	POR captured PIO status 1	user dependent	Table 27
-	R	0x108 - 0x14C	Reserved	-	-
BODCTRL	R/W	0x150	BOD control	0x000	Table 28
-	-	0x154	Reserved	-	-
SYSTCKCAL	R/W	0x158	System tick counter calibration	0x004	Table 29
-	-	0x15C - 0x1FC	Reserved	-	-
STARTAPRP0	R/W	0x200	Start logic edge control register 0		Table 30
STARTERP0	R/W	0x204	Start logic signal enable register 0		Table 31
STARTRSRP0CLR	W	0x208	Start logic reset register 0	n/a	Table 32
STARTSRP0	R	0x20C	Start logic status register 0	n/a	Table 33
-	-	0x210 - 0x22C	Reserved	-	-
PDSLEEPCFG	R/W	0x230	Power-down states in Deep-sleep mode	0x0000 0000	Table 35
PDAWAKECFG	R/W	0x234	Power-down states after wake-up from Deep-sleep mode	0x0000 EDF0	Table 36

Table 3. Register overview: system control block (base address 0x4004 8000) *...continued*

Name	Access	Address offset	Description	Reset value	Reference
PDRUNCFG	R/W	0x238	Power-down configuration register	0x0000 EDF0	Table 37
-	-	0x23C - 0x3F0	Reserved	-	-
DEVICE_ID	R	0x3F4	Device ID	part dependent	Table 38

3.4.1 System memory remap register

The system memory remap register selects whether the ARM interrupt vectors are read from the boot ROM, the flash, or the SRAM. By default, the flash memory is mapped to address 0x0000 0000. When the MAP bits in the SYSMEMREMAP register are set to 0x0 or 0x1, the boot ROM or RAM respectively are mapped to the bottom 512 bytes of the memory map (addresses 0x0000 0000 to 0x0000 0200).

Table 4. System memory remap register (SYSMEMREMAP, address 0x4004 8000) bit description

Bit	Symbol	Value	Description	Reset value
1:0	MAP		System memory remap	0x02
		00	Boot Loader Mode. Interrupt vectors are re-mapped to Boot ROM.	
		01	User RAM Mode. Interrupt vectors are re-mapped to Static RAM.	
		10 or 11	User Flash Mode. Interrupt vectors are not re-mapped and reside in Flash.	
31:2	-	-	Reserved	0x00

3.4.2 Peripheral reset control register

This register allows software to reset the SPI and I2C peripherals. Writing a 0 to the SSP0_RST_N or I2C_RST_N bits resets the SPI0 or I2C peripheral. Writing a 1 de-asserts the reset.

Remark: Before accessing the SPI and I2C peripherals, write a 1 to this register to ensure that the reset signals to the SPI and I2C are de-asserted.

Table 5. Peripheral reset control register (PRESETCTRL, address 0x4004 8004) bit description

Bit	Symbol	Value	Description	Reset value
0	SSP0_RST_N		SPI0 reset control	0
		0	Resets the SPI0 peripheral.	
		1	SPI0 reset de-asserted.	
1	I2C_RST_N		I2C reset control	0
		0	Resets the I2C peripheral.	
		1	I2C reset de-asserted.	
31:2	-	-	Reserved	0x00

3.4.3 System PLL control register

This register connects and enables the system PLL and configures the PLL multiplier and divider values. The PLL accepts an input frequency from 10 MHz to 25 MHz from various clock sources. The input frequency is multiplied up to a high frequency, then divided down to provide the actual clock used by the CPU, peripherals, and memories. The PLL can produce a clock up to the maximum allowed for the CPU.

Table 6. System PLL control register (SYSPLLCTRL, address 0x4004 8008) bit description

Bit	Symbol	Value	Description	Reset value
4:0	MSEL		Feedback divider value. The division value M is the programmed MSEL value + 1.	0x000
		00000	Division ratio M = 1	
		...		
		11111	Division ration M = 32	
6:5	PSEL		Post divider ratio P. The division ratio is 2 × P.	0x00
		00	P = 1	
		01	P = 2	
		10	P = 4	
		11	P = 8	
31:7	-	-	Reserved. Do not write ones to reserved bits.	0x0

3.4.4 System PLL status register

This register is a Read-only register and supplies the PLL lock status (see Section 3.10.1).

Table 7. System PLL status register (SYSPLLSTAT, address 0x4004 800C) bit description

Bit	Symbol	Value	Description	Reset value
0	LOCK		PLL lock status	0x0
		0	PLL not locked	
		1	PLL locked	
31:1	-	-	Reserved	0x00

3.4.5 System oscillator control register

This register configures the frequency range for the system oscillator.

Table 8. System oscillator control register (SYSOSCCTRL, address 0x4004 8020) bit description

Bit	Symbol	Value	Description	Reset value
0	BYPASS		Bypass system oscillator	0x0
		0	Oscillator is not bypassed.	
		1	Bypass enabled. PLL input (sys_osc_clk) is fed directly from the XTALIN and XTALOUT pins.	

Table 8. System oscillator control register (SYSOSCCTRL, address 0x4004 8020) bit description *…continued*

Bit	Symbol	Value	Description	Reset value
1	FREQRANGE		Determines frequency range for Low-power oscillator.	0x0
		0	1 - 20 MHz frequency range.	
		1	15 - 25 MHz frequency range	
31:2	-	-	Reserved	0x00

3.4.6 Watchdog oscillator control register

This register configures the watchdog oscillator. The oscillator consists of an analog and a digital part. The analog part contains the oscillator function and generates an analog clock (Fclkana). With the digital part, the analog output clock (Fclkana) can be divided to the required output clock frequency wdt_osc_clk. The analog output frequency (Fclkana) can be adjusted with the FREQSEL bits between 500 kHz and 3.4 MHz. With the digital part Fclkana will be divided (divider ratios = 2, 4,...,64) to wdt_osc_clk using the DIVSEL bits.

The output clock frequency of the watchdog oscillator can be calculated as wdt_osc_clk = Fclkana/(2 × (1 + DIVSEL)) = 7.8 kHz to 1.7 MHz (nominal values).

Remark: Any setting of the FREQSEL bits will yield a Fclkana value within ±40% of the listed frequency value. The watchdog oscillator is the clock source with the lowest power consumption. If accurate timing is required, use the IRC or system oscillator.

Remark: The frequency of the watchdog oscillator is undefined after reset. The watchdog oscillator frequency must be programmed by writing to the WDTOSCCTRL register before using the watchdog oscillator.

Table 9. Watchdog oscillator control register (WDTOSCCTRL, address 0x4004 8024) bit description

Bit	Symbol	Value	Description	Reset value
4:0	DIVSEL		Select divider for Fclkana. wdt_osc_clk = Fclkana/(2 × (1 + DIVSEL))	0x00
		00000	2 × (1 + DIVSEL) = 2	
		00001	2 × (1 + DIVSEL) = 4	
		00010	2 × (1 + DIVSEL) = 6	
		...	...	
		11111	2 × (1 + DIVSEL) = 64	
8:5	FREQSEL		Select watchdog oscillator analog output frequency (Fclkana).	0x00
		0001	0.5 MHz	
		0010	0.8 MHz	
		0011	1.1 MHz	
		0100	1.4 MHz	
		0101	1.6 MHz	
		0110	1.8 MHz	

Table 9. Watchdog oscillator control register (WDTOSCCTRL, address 0x4004 8024) bit description *…continued*

Bit	Symbol	Value	Description	Reset value
		0111	2.0 MHz	
		1000	2.2 MHz	
		1001	2.4 MHz	
		1010	2.6 MHz	
		1011	2.7 MHz	
		1100	2.9 MHz	
		1101	3.1 MHz	
		1110	3.2 MHz	
		1111	3.4 MHz	
31:9	-	-	Reserved	0x00

3.4.7 Internal resonant crystal control register

This register is used to trim the on-chip 12 MHz oscillator. The trim value is factory-preset and written by the boot code on start-up.

Table 10. Internal resonant crystal control register (IRCCTRL, address 0x4004 8028) bit description

Bit	Symbol	Value	Description	Reset value
7:0	TRIM		Trim value	0x1000 0000, then flash will reprogram
31:9	-	-	Reserved	0x00

3.4.8 System reset status register

The SYSRSTSTAT register shows the source of the latest reset event. The bits are cleared by writing a one to any of the bits. The POR event clears all other bits in this register, but if another reset signal - for example EXTRST - remains asserted after the POR signal is negated, then its bit is set to detected.

Table 11. System reset status register (SYSRSTSTAT, address 0x4004 8030) bit description

Bit	Symbol	Value	Description	Reset value
0	POR		POR reset status	0x0
		0	no POR detected	
		1	POR detected	
1	EXTRST		Status of the external $\overline{\text{RESET}}$ pin	0x0
		0	no $\overline{\text{RESET}}$ event detected	
		1	$\overline{\text{RESET}}$ detected	
2	WDT		Status of the Watchdog reset	0x0
		0	no WDT reset detected	
		1	WDT reset detected	
3	BOD		Status of the Brown-out detect reset	0x0
		0	no BOD reset detected	
		1	BOD reset detected	
4	SYSRST		Status of the software system reset	0x0
		0	no System reset detected	
		1	System reset detected	
31:5	-	-	Reserved	0x00

3.4.9 System PLL clock source select register

This register selects the clock source for the system PLL. The SYSPLLCLKUEN register (see Section 3.4.10) must be toggled from LOW to HIGH for the update to take effect.

Remark: When switching clock sources, both clocks must be running before the clock source can be updated.

Table 12. System PLL clock source select register (SYSPLLCLKSEL, address 0x4004 8040) bit description

Bit	Symbol	Value	Description	Reset value
1:0	SEL		System PLL clock source	0x00
		00	IRC oscillator	
		01	System oscillator	
		10	Reserved	
		11	Reserved	
31:2	-	-	Reserved	0x00

3.4.10 System PLL clock source update enable register

This register updates the clock source of the system PLL with the new input clock after the SYSPLLCLKSEL register has been written to. In order for the update to take effect, first write a zero to the SYSPLLUEN register and then write a one to SYSPLLUEN.

To successfully change clock sources, both clock sources must be running before updating this register.

Table 13. System PLL clock source update enable register (SYSPLLUEN, address 0x4004 8044) bit description

Bit	Symbol	Value	Description	Reset value
0	ENA		Enable system PLL clock source update	0x0
		0	No change	
		1	Update clock source	
31:1	-	-	Reserved	0x00

3.4.11 Main clock source select register

This register selects the main system clock which can be either any input to the system PLL, the output from the system PLL (sys_pllclkout), or the watchdog or IRC oscillators directly. The main system clock clocks the core, the peripherals, and the memories.

The MAINCLKUEN register (see Section 3.4.12) must be toggled from LOW to HIGH for the update to take effect.

Remark: When switching clock sources, both clocks must be running before the clock source can be updated.

Table 14. Main clock source select register (MAINCLKSEL, address 0x4004 8070) bit description

Bit	Symbol	Value	Description	Reset value
1:0	SEL		Cock source for main clock	0x00
		00	IRC oscillator	
		01	Input clock to system PLL	
		10	WDT oscillator	
		11	System PLL clock out	
31:2	-	-	Reserved	0x00

3.4.12 Main clock source update enable register

This register updates the clock source of the main clock with the new input clock after the MAINCLKSEL register has been written to. In order for the update to take effect, first write a zero to the MAINCLKUEN register and then write a one to MAINCLKUEN.

To successfully change clock sources, both clock sources must be running before updating this register.

Table 15. Main clock source update enable register (MAINCLKUEN, address 0x4004 8074) bit description

Bit	Symbol	Value	Description	Reset value
0	ENA		Enable main clock source update	0x0
		0	No change	
		1	Update clock source	
31:1	-	-	Reserved	0x00

3.4.13 System AHB clock divider register

This register divides the main clock to provide the system clock to the core, memories, and the peripherals. The system clock can be shut down completely by setting the DIV bits to 0x0.

Table 16. System AHB clock divider register (SYSAHBCLKDIV, address 0x4004 8078) bit description

Bit	Symbol	Value	Description	Reset value
7:0	DIV		System AHB clock divider values	0x01
		0	System clock disabled.	
		1	Divide by 1	
		to	...	
		255	Divide by 255	
31:8	-	-	Reserved	0x00

3.4.14 System AHB clock control register

The AHBCLKCTRL register enables the clocks to individual system and peripheral blocks. The system clock (sys_ahb_clk[0], bit 0 in the AHBCLKCTRL register) provides the clock for the AHB to APB bridge, the AHB matrix, the ARM Cortex-M0, the Syscon block, and the PMU. This clock cannot be disabled.

Table 17. System AHB clock control register (SYSAHBCLKCTRL, address 0x4004 8080) bit description

Bit	Symbol	Value	Description	Reset value
0	SYS		Enables clock for AHB to APB bridge, to the AHB matrix, to the Cortex-M0 FCLK and HCLK, to the SysCon, and to the PMU. This bit is read only.	1
		0	Reserved	
		1	Enable	
1	ROM		Enables clock for ROM.	1
		0	Disable	
		1	Enable	
2	RAM		Enables clock for RAM.	1
		0	Disable	
		1	Enable	

Table 17. System AHB clock control register (SYSAHBCLKCTRL, address 0x4004 8080) bit description *…continued*

Bit	Symbol	Value	Description	Reset value
3	FLASHREG		Enables clock for flash register interface.	1
		0	Disabled	
		1	Enabled	
4	FLASHARRAY		Enables clock for flash array access.	1
		0	Disabled	
		1	Enabled	
5	I2C		Enables clock for I2C.	0
		0	Disable	
		1	Enable	
6	GPIO		Enables clock for GPIO.	1
		0	Disable	
		1	Enable	
7	CT16B0		Enables clock for 16-bit counter/timer 0.	0
		0	Disable	
		1	Enable	
8	Metrology engine clock		Automatically set by the metrology engine software.	0
		0	Disable	
		1	Enable	
9	CT32B0		Enables clock for 32-bit counter/timer 0.	0
		0	Disable	
		1	Enable	
10	CT32B1		Enables clock for 32-bit counter/timer 1.	0
		0	Disable	
		1	Enable	
11	SSP0		Enables clock for SPI0.	1
		0	Disable	
		1	Enable	
12	UART		Enables clock for UART.	0
		0	Disable	
		1	Enable	
13	Metrology engine clock		Automatically set by the metrology engine software.	0
		0	Disable	
		1	Enable	
14	-	-	Reserved	0
15	WDT		Enables clock for WDT.	0
		0	Disable	
		1	Enable	

Table 17. System AHB clock control register (SYSAHBCLKCTRL, address 0x4004 8080) bit description *…continued*

Bit	Symbol	Value	Description	Reset value
16	IOCON		Enables clock for I/O configuration block.	0
		0	Disable	
		1	Enable	
17	-	-	Reserved	0
18	-	-	Reserved	0
31:19	-	-	Reserved	0x00

3.4.15 SPI0 clock divider register

This register configures the SPI0 peripheral clock SPI0_PCLK. The SPI0_PCLK can be shut down by setting the DIV bits to 0x0.

Table 18. SPI0 clock divider register (SSP0CLKDIV, address 0x4004 8094) bit description

Bit	Symbol	Value	Description	Reset value
7:0	DIV		SPI0_PCLK clock divider values	0x00
		0	Disable SPI0_PCLK.	
		1	Divide by 1.	
		to	...	
		255	Divide by 255.	
31:8	-	-	Reserved	0x00

3.4.16 UART clock divider register

This register configures the UART peripheral clock UART_PCLK. The UART_PCLK can be shut down by setting the DIV bits to 0x0.

Table 19. UART clock divider register (UARTCLKDIV, address 0x4004 8098) bit description

Bit	Symbol	Value	Description	Reset value
7:0	DIV		UART_PCLK clock divider values	0x00
		0	Disable UART_PCLK.	
		1	Divide by 1.	
		to	...	
		255	Divide by 255.	
31:8	-	-	Reserved	0x00

3.4.17 WDT clock source select register

This register selects the clock source for the watchdog timer. The WDTCLKUEN register (see Section 3.4.18) must be toggled from LOW to HIGH for the update to take effect.

Table 20. WDT clock source select register (WDTCLKSEL, address 0x4004 80D0) bit description

Bit	Symbol	Value	Description	Reset value
1:0	SEL		WDT clock source	0x00
		00	IRC oscillator	
		01	Main clock	
		10	Watchdog oscillator	
		11	Reserved	
31:2	-	-	Reserved	0x00

3.4.18 WDT clock source update enable register

This register updates the clock source of the watchdog timer with the new input clock after the WDTCLKSEL register has been written to. In order for the update to take effect at the input of the watchdog timer, first write a zero to the WDTCLKUEN register and then write a one to WDTCLKUEN.

Table 21. WDT clock source update enable register (WDTCLKUEN, address 0x4004 80D4) bit description

Bit	Symbol	Value	Description	Reset value
0	ENA		Enable WDT clock source update	0x0
		0	No change	
		1	Update clock source	
31:1	-	-	Reserved	0x00

3.4.19 WDT clock divider register

This register determines the divider values for the watchdog clock wdt_clk.

Table 22. WDT clock divider register (WDTCLKDIV, address 0x4004 80D8) bit description

Bit	Symbol	Value	Description	Reset value
7:0	DIV		WDT clock divider values	0x00
		0	Disable	
		1	Divide by 1	
		to	...	
		255	Divide by 255	
31:8	-	-	Reserved	0x00

3.4.20 CLKOUT clock source select register

This register configures the clkout_clk signal to be output on the CLKOUT pin. All three oscillators and the main clock can be selected for the clkout_clk clock.

The CLKOUTCLKUEN register (see Section 3.4.21) must be toggled from LOW to HIGH for the update to take effect.

Table 23. CLKOUT clock source select register (CLKOUTCLKSEL, address 0x4004 80E0) bit description

Bit	Symbol	Value	Description	Reset value
1:0	SEL		CLKOUT clock source	0x00
		00	IRC oscillator	
		01	System oscillator	
		10	Watchdog oscillator	
		11	Main clock	
31:2	-	-	Reserved	0x00

3.4.21 CLKOUT clock source update enable register

This register updates the clock source of the CLKOUT pin with the new clock after the CLKOUTCLKSEL register has been written to. In order for the update to take effect at the input of the CLKOUT pin, first write a zero to the CLKCLKUEN register and then write a one to CLKCLKUEN.

Table 24. CLKOUT clock source update enable register (CLKOUTUEN, address 0x4004 80E4) bit description

Bit	Symbol	Value	Description	Reset value
0	ENA		Enable CLKOUT clock source update	0x0
		0	No change	
		1	Update clock source	
31:1	-	-	Reserved	0x00

3.4.22 CLKOUT clock divider register

This register determines the divider value for the clock output signal on the CLKOUT pin.

Table 25. CLKOUT clock divider registers (CLKOUTCLKDIV, address 0x4004 80E8) bit description

Bit	Symbol	Value	Description	Reset value
7:0	DIV		Clock divider values	0x00
		0	Disable	
		1	Divide by 1	
		to	...	
		255	Divide by 255	
31:8	-	-	Reserved	0x00

3.4.23 POR captured PIO status register 0

The PIOPORCAP0 register captures the state (HIGH or LOW) of the PIO pins of ports 0,1, and 2 (pins PIO2_0 to PIO2_7) at power-on-reset. Each bit represents the reset state of one GPIO pin. This register is a read-only status register.

Table 26. POR captured PIO status registers 0 (PIOPORCAP0, address 0x4004 8100) bit description

Bit	Symbol	Description	Reset value
11:0	CAPPIO0_11 to CAPPIO0_0	Raw reset status input PIO0_11 to PIO0_0	User implementation dependent
23:12	CAPPIO1_11 to CAPPIO1_0	Raw reset status input PIO1_11 to PIO1_0	User implementation dependent
31:24	CAPPIO2_7 to CAPPIO2_0	Raw reset status input PIO2_7 to PIO2_0	User implementation dependent

3.4.24 POR captured PIO status register 1

The PIOPORCAP1 register captures the state (HIGH or LOW) of the PIO pins of port 2 (PIO2_8 to PIO2_11) and port 3 at power-on-reset. Each bit represents the reset state of one PIO pin. This register is a read-only status register.

Table 27. POR captured PIO status registers 1 (PIOPORCAP1, address 0x4004 8104) bit description

Bit	Symbol	Description	Reset value
0	CAPPIO2_8	Raw reset status input PIO2_8	User implementation dependent
1	CAPPIO2_9	Raw reset status input PIO2_9	User implementation dependent
2	CAPPIO2_10	Raw reset status input PIO2_10	User implementation dependent
3	CAPPIO2_11	Raw reset status input PIO2_11	User implementation dependent
4	CAPPIO3_0	Raw reset status input PIO3_0	User implementation dependent
5	CAPPIO3_1	Raw reset status input PIO3_1	User implementation dependent
6	CAPPIO3_2	Raw reset status input PIO3_2	User implementation dependent
7	CAPPIO3_3	Raw reset status input PIO3_3	User implementation dependent
8	CAPPIO3_4	Raw reset status input PIO3_4	User implementation dependent
9	CAPPIO3_5	Raw reset status input PIO3_5	User implementation dependent
31:10	-	Reserved	-

3.4.25 BOD control register

The BOD control register selects four separate threshold values for sending a BOD interrupt to the NVIC and for forced reset. Reset and interrupt threshold values listed in Table 28 are typical values.

Table 28. BOD control register (BODCTRL, address 0x4004 8150) bit description

Bit	Symbol	Value	Description	Reset value
1:0	BODRSTLEV		BOD reset level	00
		00	Level 0: The reset assertion threshold voltage is 1.46 V; the reset de-assertion threshold voltage is 1.63 V.	
		01	Level 1: The reset assertion threshold voltage is 2.06 V; the reset de-assertion threshold voltage is 2.15 V.	
		10	Level 2: The reset assertion threshold voltage is 2.35 V; the reset de-assertion threshold voltage is 2.43 V.	
		11	Level 3: The reset assertion threshold voltage is 2.63 V; the reset de-assertion threshold voltage is 2.71 V.	

Table 28. BOD control register (BODCTRL, address 0x4004 8150) bit description

Bit	Symbol	Value	Description	Reset value
3:2	BODINTVAL		BOD interrupt level	00
		00	Level 0: The interrupt assertion threshold voltage is 1.65 V; the interrupt de-assertion threshold voltage is 1.80 V.	
		01	Level 1:The interrupt assertion threshold voltage is 2.22 V; the interrupt de-assertion threshold voltage is 2.35 V.	
		10	Level 2: The interrupt assertion threshold voltage is 2.52 V; the interrupt de-assertion threshold voltage is 2.66 V.	
		11	Level 3: The interrupt assertion threshold voltage is 2.80 V; the interrupt de-assertion threshold voltage is 2.90 V.	
4	BODRSTENA		BOD reset enable	0
		0	Disable reset function.	
		1	Enable reset function.	
31:5	-	-	Reserved	0x00

3.4.26 System tick counter calibration register

Table 29. System tick timer calibration register (SYSTCKCAL, address 0x4004 8158) bit description

Bit	Symbol	Value	Description	Reset value
25:0	CAL		System tick timer calibration value	0x04
31:26	-	-	Reserved	0x00

3.4.27 Start logic edge control register 0

The STARTAPRP0 register controls the start logic inputs of port 0 (PIO0_0 to PIO0_10). This register selects a falling or rising edge on the corresponding PIO input to produce a falling or rising clock edge, respectively, for the start logic (see Section 3.9.2).

Every bit in the STARTAPRP0 register controls one port input and is connected to one wake-up interrupt in the NVIC. Bit 0 in the STARTAPRP0 register corresponds to interrupt 0, bit 1 to interrupt 1, etc. (see Table 46), up to a total of 11 interrupts.

Remark: Each interrupt connected to a start logic input must be enabled in the NVIC if the corresponding PIO pin is used to wake up the chip from Deep-sleep mode.

Table 30. Start logic edge control register 0 (STARTAPRP0, address 0x4004 8200) bit description

Bit	Symbol	Value	Description	Reset value
10:0	APRPIO0_10 to APRPIO0_0		Edge select for start logic input PIO0_10 to PIO0_0	0x0
		0	Falling edge	
		1	Rising edge	
31:11	-	-	Reserved. Do not write a 1 to reserved bits in this register.	0x0

3.4.28 Start logic signal enable register 0

This STARTERP0 register enables or disables the start signal bits in the start logic. The bit assignment is identical to Table 30.

Table 31. Start logic signal enable register 0 (STARTERP0, address 0x4004 8204) bit description

Bit	Symbol	Value	Description	Reset value
10:0	ERPIO0_10 to ERPIO0_0		Enable start signal for start logic input PIO0_10 to PIO0_0	0x0
		0	Disabled	
		1	Enabled	
31:11	-		Reserved. Do not write a 1 to reserved bits in this register.	0x0

3.4.29 Start logic reset register 0

Writing a one to a bit in the STARTRSRP0CLR register resets the start logic state. The bit assignment is identical to Table 30. The start-up logic uses the input signals to generate a clock edge for registering a start signal. This clock edge (falling or rising) sets the interrupt for waking up from Deep-sleep mode. Therefore, the start-up logic states must be cleared before being used.

Table 32. Start logic reset register 0 (STARTRSRP0CLR, address 0x4004 8208) bit description

Bit	Symbol	Value	Description	Reset value
10:0	RSRPIO0_10 to RSRPIO0_0		Start signal reset for start logic input PIO0_10 to PIO0_0	n/a
		0	-	
		1	Write: reset start signal	
31:11	-	-	Reserved. Do not write a 1 to reserved bits in this register.	n/a

3.4.30 Start logic status register 0

This register reflects the status of the enabled start signal bits. The bit assignment is identical to Table 30. Each bit (if enabled) reflects the state of the start logic, i.e. whether or not a wake-up signal has been received for a given pin.

Table 33. Start logic status register 0 (STARTSRP0, address 0x4004 820C) bit description

Bit	Symbol	Value	Description	Reset value
10:0	SRPIO0_10 to SRPIO0_0		Start signal status for start logic input PIO0_10 to PIO0_0	n/a
		0	No start signal received	
		1	Start signal pending	
31:11	-	-	Reserved. Do not write a 1 to reserved bits in this register.	n/a