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LPC11U6x

32-bit ARM Cortex-M0+ microcontroller; up to 256 KB flash and 36 KB SRAM; 4 KB EEPROM; USB; 12-bit ADC

Rev. 1.3 — 7 September 2016 Product data sheet

1. General description

The LPC11U6x are an ARM Cortex-M0+ based, low-cost 32-bit MCU family operating at CPU frequencies of up to 50 MHz. The LPC11U6x support up to 256 KB of flash memory, a 4 KB EEPROM, and 36 KB of SRAM.

The ARM Cortex-M0+ is an easy-to-use, energy-efficient core using a two-stage pipeline and fast single-cycle I/O access.

The peripheral complement of the LPC11U6x includes a DMA controller, a CRC engine, one full-speed USB device controller with XTAL-less low-speed mode, two I^2C-bus interfaces, up to five USARTs, two SSP interfaces, PWM/timer subsystem with six configurable multi-purpose timers, a Real-Time Clock, one 12-bit ADC, temperature sensor, function-configurable I/O ports, and up to 80 general-purpose I/O pins.

For additional documentation related to the LPC11U6x parts, see Section 17 “References”.

2. Features and benefits

- System:
  - ARM Cortex-M0+ processor (version r0p1), running at frequencies of up to 50 MHz with single-cycle multiplier and fast single-cycle I/O port.
  - ARM Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC).
  - AHB Multilayer matrix.
  - System tick timer.
  - Serial Wire Debug (SWD) and JTAG boundary scan modes supported.
  - Micro Trace Buffer (MTB) supported.
- Memory:
  - Up to 256 KB on-chip flash programming memory with page erase.
  - Up to 32 KB main SRAM.
  - Up to two additional SRAM blocks of 2 KB each.
  - Up to 4 KB EEPROM.
- ROM API support:
  - Boot loader.
  - USART drivers.
  - I2C drivers.
  - USB drivers.
  - DMA drivers.

- Power profiles.
- Flash In-Application Programming (IAP) and In-System Programming (ISP).
- 32-bit integer division routines.

- Digital peripherals:
  - Simple DMA engine with 16 channels and programmable input triggers.
  - High-speed GPIO interface connected to the ARM Cortex-M0+ IO bus with up to 80 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, programmable open-drain mode, input inverter, and programmable glitch filter and digital filter.
  - Pin interrupt and pattern match engine using eight selectable GPIO pins.
  - Two GPIO group interrupt generators.
  - CRC engine.
- Configurable PWM/timer subsystem (two 16-bit and two 32-bit standard counter/timers, two State-Configurable Timers (SCTimer/PWM)) that provides:
  - Up to four 32-bit and two 16-bit counter/timers or two 32-bit and six 16-bit counter/timers.
  - Up to 21 match outputs and 16 capture inputs.
  - Up to 19 PWM outputs with 6 independent time bases.
- Windowed WatchDog timer (WWDT).
- Real-time Clock (RTC) in the always-on power domain with separate battery supply pin and 32 kHz oscillator.
- Analog peripherals:
  - One 12-bit ADC with up to 12 input channels with multiple internal and external trigger inputs and with sample rates of up to 2 Msamples/s. The ADC supports two independent conversion sequences.
  - Temperature sensor.
- Serial interfaces:
  - Up to five USART interfaces, all with DMA, synchronous mode, and RS-485 mode support. Four USARTs use a shared fractional baud generator.
  - Two SSP controllers with DMA support.
  - Two I^2C-bus interfaces. One I^2C-bus interface with specialized open-drain pins supports I2C Fast-mode plus.
  - USB 2.0 full-speed device controller with on-chip PHY. XTAL-less low-speed mode supported.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy for $-25\ °C \leq T_{amb} \leq +85\ °C$ that can optionally be used as a system clock.
  - On-chip 32 kHz oscillator for RTC.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz. Oscillator pins are shared with the GPIO pins.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal.
  - A second, dedicated PLL is provided for USB.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.

- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode.
  - Wake-up from Deep-sleep and Power-down modes on external pin inputs and USART activity.
  - Power-On Reset (POR).
  - Brownout detect.
- Unique device serial number for identification.
- Single power supply (2.4 V to 3.6 V).
- Separate VBAT supply for RTC.
- Operating temperature range −40 °C to 105 °C.
- Available as LQFP48, LQFP64, and LQFP100 packages.

3. Applications

- Three-phase e-meter
- GPS tracker
- Gaming accessories
- Car radio
- Medical monitor
- PC peripherals

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC11U66JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U67JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U67JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11U67JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC11U68JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U68JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11U68JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash/ KB	EEPROM/ KB	SRAM/ KB	USB	USART0	USART1	USART2	USART3	USART4	I^2C	SSP	Timers with PWM	12-bit ADC channels	GPIO
LPC11U66JBD48	64	4	12	1	Y	Y	Y	N	N	2	2	6	8	34
LPC11U67JBD48	128	4	20	1	Y	Y	Y	N	N	2	2	6	8	34
LPC11U67JBD64	128	4	20	1	Y	Y	Y	N	N	2	2	6	10	48
LPC11U67JBD100	128	4	20	1	Y	Y	Y	Y	Y	2	2	6	12	80
LPC11U68JBD48	256	4	36	1	Y	Y	Y	N	N	2	2	6	8	34
LPC11U68JBD64	256	4	36	1	Y	Y	Y	N	N	2	2	6	10	48
LPC11U68JBD100	256	4	36	1	Y	Y	Y	Y	Y	2	2	6	12	80

5. Marking

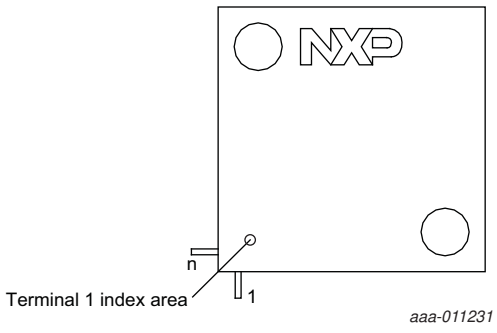


Fig 1. LQFP64/100 package marking

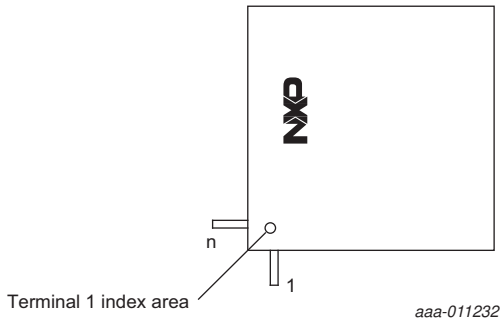


Fig 2. LQFP48 package marking

The LPC11U6x devices typically have the following top-side marking for LQFP100 packages:

LPC11U6xJBD100

xxxxxx xx

xxxyywwxR[x]

The LPC11U6x devices typically have the following top-side marking for LQFP64 packages:

LPC11U6xJ

xxxxxx xx

xxxyywwxR[x]

The LPC11U6x devices typically have the following top-side marking for LQFP48 packages:

LPC11U6xJ

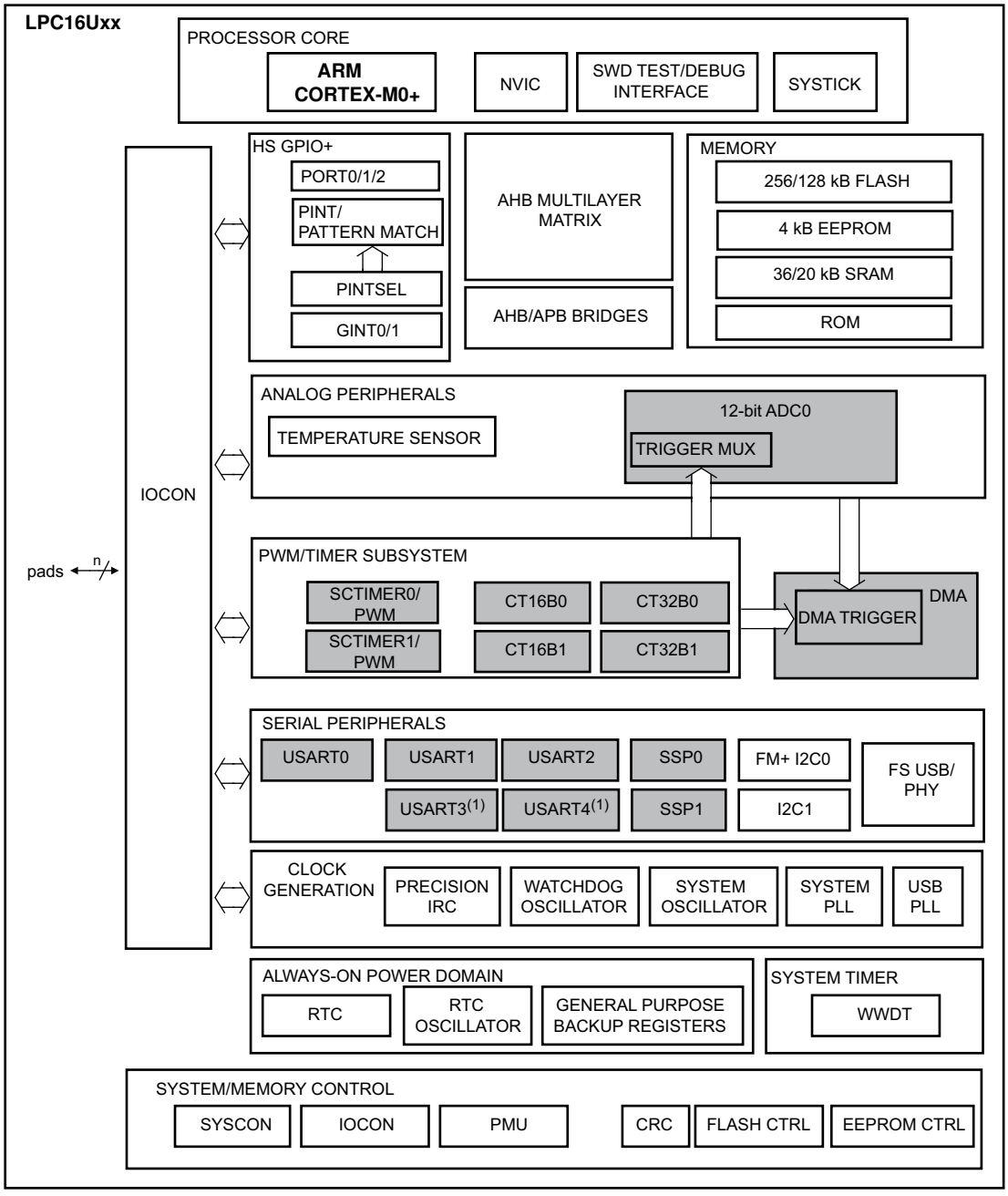
xx xx

xxxyy

wwxR[x]

Field ‘yy’ states the year the device was manufactured. Field ‘ww’ states the week the device was manufactured during that year. Field ‘R’ states the chip revision.

6. Block diagram



Gray-shaded blocks show peripherals that can provide hardware triggers for DMA transfers or have DMA request lines.

(1) Available on LQFP100 packages only.

Fig 3. LPC11U6x block diagram

7. Pinning information

7.1 Pinning

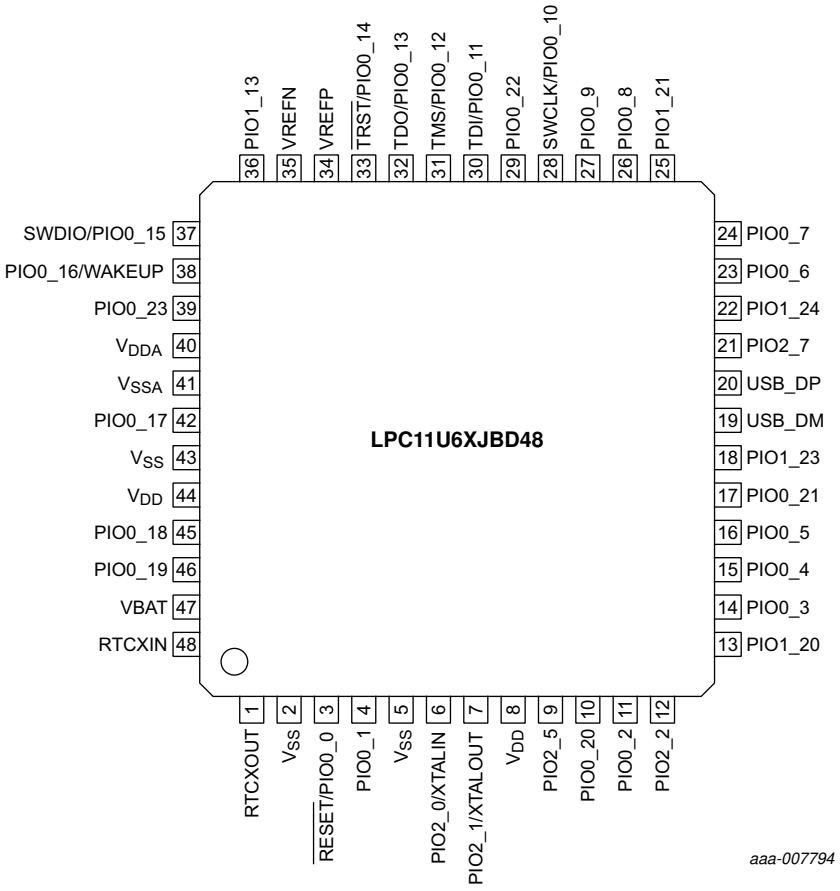


Fig 4. LQFP48 pinning

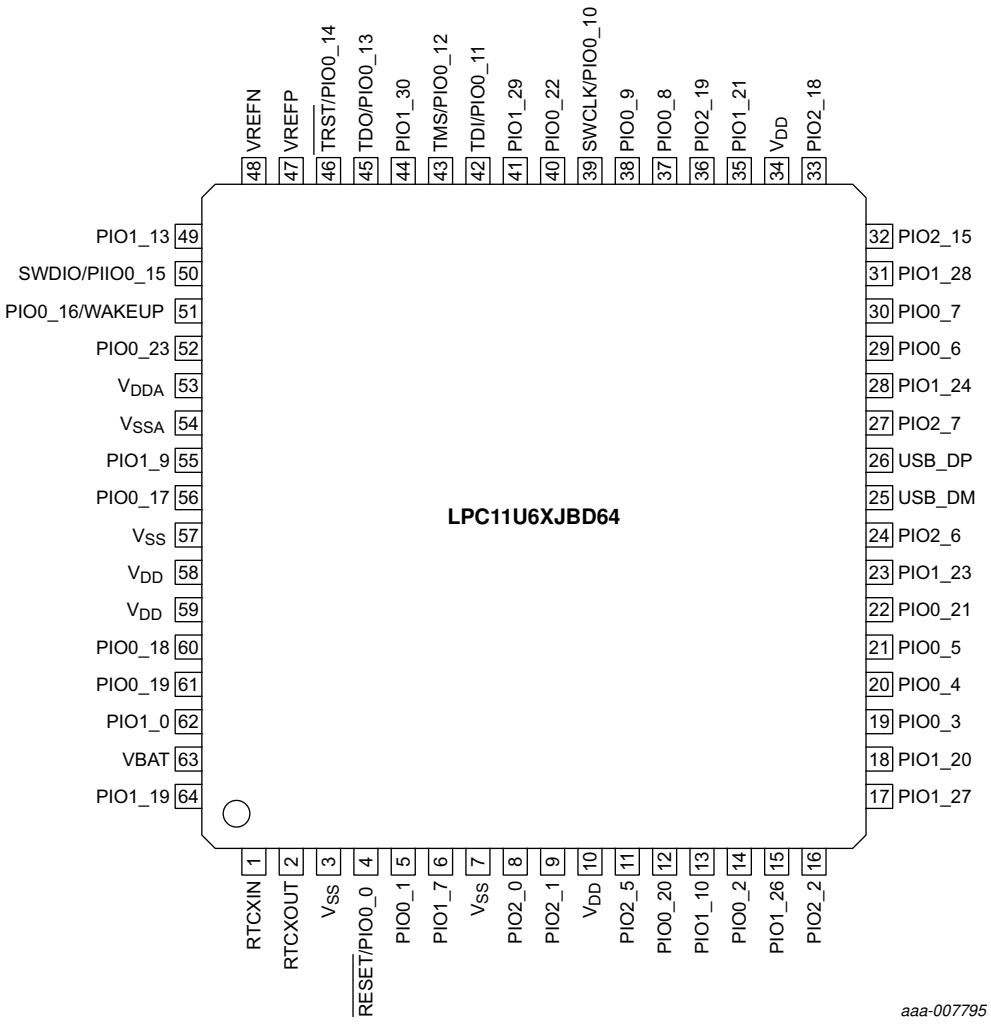


Fig 5. LQFP64 pinning

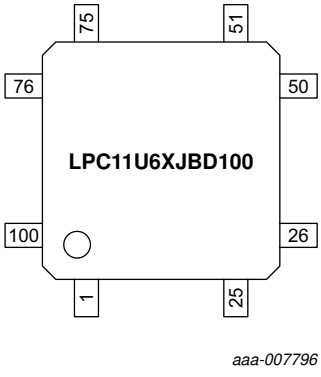


Fig 6. LQFP100 pinning

7.2 Pin description

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
$\overline{\text{RESET}}$/PIO0_0	3	4	8	[8]	I; PU	I	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed and Deep power-down mode is not used.
						IO	**PIO0_0 —** General-purpose digital input/output pin.
PIO0_1	4	5	9	[6]	I; PU	IO	**PIO0_1 —** General-purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler or the USB device enumeration.
						O	**CLKOUT —** Clockout pin.
						O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
						O	**USB_FTOGGLE —** USB 1 ms Start-of-Frame signal.
PIO0_2	11	14	19	[6]	I; PU	IO	**PIO0_2 —** General-purpose port 0 input/output 2.
						IO	**SSP0_SSEL —** Slave select for SSP0.
						I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
						-	**R_0 —** Reserved.
PIO0_3	14	19	30	[6]	I; PU	IO	**PIO0_3 —** General-purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler. A HIGH level during reset starts the USB device enumeration.
						I	**USB_VBUS —** Monitors the presence of USB bus power.
						-	**R_1 —** Reserved.
PIO0_4	15	20	31	[7]	IA	IO	**PIO0_4 —** General-purpose port 0 input/output 4 (open-drain).
						IO	**I2C0_SCL —** I^2C-bus clock input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
						-	**R_2 —** Reserved.
PIO0_5	16	21	32	[7]	IA	IO	**PIO0_5 —** General-purpose port 0 input/output 5 (open-drain).
						IO	**I2C0_SDA —** I^2C-bus data input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
						-	**R_3 —** Reserved.

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO0_6	23	29	44	[6]	I; PU	IO	**PIO0_6 —** General-purpose port 0 input/output 6.
						-	**R —** Reserved.
						IO	**SSP0_SCK —** Serial clock for SSP0.
						-	**R_4 —** Reserved.
PIO0_7	24	30	45	[5]	I; PU	IO	**PIO0_7 —** General-purpose port 0 input/output 7 (high-current output driver).
						I	**$\overline{\text{U0\_CTS}}$ —** Clear To Send input for USART.
						-	**R_5 —** Reserved.
						IO	**I2C1_SCL —** I^2C-bus clock input/output. This pin is not open-drain.
PIO0_8	26	37	58	[6]	I; PU	IO	**PIO0_8 —** General-purpose port 0 input/output 8.
						IO	**SSP0_MISO —** Master In Slave Out for SSP0.
						O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
						-	**R_6 —** Reserved.
PIO0_9	27	38	59	[6]	I; PU	IO	**PIO0_9 —** General-purpose port 0 input/output 9.
						IO	**SSP0_MOSI —** Master Out Slave In for SSP0.
						O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
						-	**R_7 —** Reserved.
SWCLK/PIO0_10	28	39	60	[6]	I; PU	IO	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
						IO	**PIO0_10 —** General-purpose digital input/output pin.
						IO	**SSP0_SCK —** Serial clock for SSP0.
						O	**CT16B0_MAT2 —** 16-bit timer0 MAT2
TDI/PIO0_11	30	42	64	[3]	I; PU	IO	**TDI —** Test Data In for JTAG interface. In boundary scan mode only.
						IO	**PIO0_11 —** General-purpose digital input/output pin.
						AI	**ADC_9 —** A/D converter, input channel 9.
						O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
						O	**$\overline{\text{U1\_RTS}}$ —** Request To Send output for USART1.
						IO	**U1_SCLK —** Serial clock input/output for USART1 in synchronous mode.
TMS/PIO0_12	31	43	66	[3]	I; PU	IO	**TMS —** Test Mode Select for JTAG interface. In boundary scan mode only.
						IO	**PIO0_12 —** General-purpose digital input/output pin.
						AI	**ADC_8 —** A/D converter, input channel 8.
						I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
						I	**$\overline{\text{U1\_CTS}}$ —** Clear To Send input for USART1.

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
TDO/PIO0_13	32	45	68	[3]	I; PU	IO	**TDO —** Test Data Out for JTAG interface. In boundary scan mode only.
						IO	**PIO0_13 —** General-purpose digital input/output pin.
						AI	**ADC_7 —** A/D converter, input channel 7.
						O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
						I	**U1_RXD —** Receiver input for USART1.
$\overline{\text{TRST}}$/PIO0_14	33	46	69	[3]	I; PU	IO	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface. In boundary scan mode only.
						IO	**PIO0_14 —** General-purpose digital input/output pin.
						AI	**ADC_6 —** A/D converter, input channel 6.
						O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
						O	**U1_TXD —** Transmitter output for USART1.
SWDIO/PIO0_15	37	50	81	[3]	I; PU	IO	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
						IO	**PIO0_15 —** General-purpose digital input/output pin.
						AI	**ADC_3 —** A/D converter, input channel 3.
						O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO0_16/WAKEUP	38	51	82	[4]	I; PU	IO	**PIO0_16 —** General-purpose digital input/output pin. This pin also serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
						AI	**ADC_2 —** A/D converter, input channel 2.
						O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
						-	**R_8 —** Reserved.
PIO0_17	42	56	90	[6]	I; PU	IO	**PIO0_17 —** General-purpose digital input/output pin.
						O	**$\overline{\text{U0\_RTS}}$ —** Request To Send output for USART0.
						I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
						IO	**U0_SCLK —** Serial clock input/output for USART0 in synchronous mode.
PIO0_18	45	60	94	[6]	I; PU	IO	**PIO0_18 —** General-purpose digital input/output pin.
						I	**U0_RXD —** Receiver input for USART0. Used in UART ISP mode.
						O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO0_19	46	61	95	[6]	I; PU	IO	**PIO0_19 —** General-purpose digital input/output pin.
						O	**U0_TXD —** Transmitter output for USART0. Used in UART ISP mode.
						O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO0_20	10	12	17	[6]	I; PU	IO	**PIO0_20** — General-purpose digital input/output pin.
						I	**CT16B1_CAP0** — Capture input 0 for 16-bit timer 1.
						I	**U2_RXD** — Receiver input for USART2.
PIO0_21	17	22	33	[6]	I; PU	IO	**PIO0_21** — General-purpose digital input/output pin.
						O	**CT16B1_MAT0** — Match output 0 for 16-bit timer 1.
						IO	**SSP1_MOSI** — Master Out Slave In for SSP1.
PIO0_22	29	40	62	[3]	I; PU	IO	**PIO0_22** — General-purpose digital input/output pin.
						AI	**ADC_11** — A/D converter, input channel 11.
						I	**CT16B1_CAP1** — Capture input 1 for 16-bit timer 1.
						IO	**SSP1_MISO** — Master In Slave Out for SSP1.
PIO0_23	39	52	83	[3]	I; PU	IO	**PIO0_23** — General-purpose digital input/output pin.
						AI	**ADC_1** — A/D converter, input channel 1.
						-	**R_9** — Reserved.
						I	**$\overline{\text{U0\_RI}}$** — Ring Indicator input for USART0.
						IO	**SSP1_SSEL** — Slave select for SSP1.
PIO1_0	-	62	97	[6]	I; PU	IO	**PIO1_0** — General-purpose digital input/output pin.
						O	**CT32B1_MAT0** — Match output 0 for 32-bit timer 1.
						-	**R_10** — Reserved.
						O	**U2_TXD** — Transmitter output for USART2.
PIO1_1	-	-	28	[6]	I; PU	IO	**PIO1_1** — General-purpose digital input/output pin.
						O	**CT32B1_MAT1** — Match output 1 for 32-bit timer 1.
						-	**R_11** — Reserved.
						O	**$\overline{\text{U0\_DTR}}$** — Data Terminal Ready output for USART0.
PIO1_2	-	-	55	[6]	I; PU	IO	**PIO1_2** — General-purpose digital input/output pin.
						O	**CT32B1_MAT2** — Match output 2 for 32-bit timer 1.
						-	**R_12** — Reserved.
						I	**U1_RXD** — Receiver input for USART1.
PIO1_3	-	-	72	[3]	I; PU	IO	**PIO1_3** — General-purpose digital input/output pin.
						O	**CT32B1_MAT3** — Match output 3 for 32-bit timer 1.
						-	**R_13** — Reserved.
						IO	**I2C1_SDA** — I^2C-bus data input/output (not open-drain).
						AI	**ADC_5** — A/D converter, input channel 5.
PIO1_4	-	-	23	[6]	I; PU	IO	**PIO1_4** — General-purpose digital input/output pin.
						I	**CT32B1_CAP0** — Capture input 0 for 32-bit timer 1.
						-	**R_14** — Reserved.
						I	**$\overline{\text{U0\_DSR}}$** — Data Set Ready input for USART0.

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO1_5	-	-	47	[6]	I; PU	IO	**PIO1_5** — General-purpose digital input/output pin.
						I	**CT32B1_CAP1** — Capture input 1 for 32-bit timer 1.
						-	**R_15** — Reserved.
						I	**$\overline{\text{U0\_DCD}}$** — Data Carrier Detect input for USART0.
PIO1_6	-	-	98	[6]	I; PU	IO	**PIO1_6** — General-purpose digital input/output pin.
						-	**R_16** — Reserved.
						I	**U2_RXD** — Receiver input for USART2.
						I	**CT32B0_CAP2** — Capture input 2 for 32-bit timer 0.
PIO1_7	-	6	10	[6]	I; PU	IO	**PIO1_7** — General-purpose digital input/output pin.
						-	**R_17** — Reserved.
						I	**$\overline{\text{U2\_CTS}}$** — Clear To Send input for USART2.
						I	**CT16B1_CAP0** — Capture input 0 for 32-bit timer 1.
PIO1_8	-	-	61	[6]	I; PU	IO	**PIO1_8** — General-purpose digital input/output pin.
						-	**R_18** — Reserved.
						O	**U1_TXD** — Transmitter output for USART1.
						I	**CT16B0_CAP0** — Capture input 0 for 16-bit timer 0.
PIO1_9	-	55	86	[3]	I; PU	IO	**PIO1_9** — General-purpose digital input/output pin.
						I	**$\overline{\text{U0\_CTS}}$** — Clear To Send input for USART0.
						O	**CT16B1_MAT1** — Match output 1 for 16-bit timer 1.
						I	**ADC_0** — A/D converter, input channel 0.
PIO1_10	-	13	18	[6]	I; PU	IO	**PIO1_10** — General-purpose digital input/output pin.
						O	**$\overline{\text{U2\_RTS}}$** — Request To Send output for USART2.
						IO	**U2_SCLK** — Serial clock input/output for USART2 in synchronous mode.
						O	**CT16B1_MAT0** — Match output 0 for 16-bit timer 1.
PIO1_11	-	-	65	[6]	I; PU	IO	**PIO1_11** — General-purpose digital input/output pin.
						IO	**I2C1_SCL** — I^2C1-bus clock input/output (not open-drain).
						O	**CT16B0_MAT2** — Match output 2 for 16-bit timer 0.
						I	**$\overline{\text{U0\_RI}}$** — Ring Indicator input for USART0.
PIO1_12	-	-	89	[6]	I; PU	IO	**PIO1_12** — General-purpose digital input/output pin.
						IO	**SSP0_MOSI** — Master Out Slave In for SSP0.
						O	**CT16B0_MAT1** — Match output 1 for 16-bit timer 0.
						-	**R_21** — Reserved.
PIO1_13	36	49	78	[6]	I; PU	IO	**PIO1_13** — General-purpose digital input/output pin.
						I	**$\overline{\text{U1\_CTS}}$** — Clear To Send input for USART1.
						O	**SCT0_OUT3** — SCTimer0/PWM output 3.
						-	**R_22** — Reserved.

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO1_14	-	-	79	[6]	I; PU	IO	**PIO1_14 —** General-purpose digital input/output pin.
						IO	**I2C1_SDA —** I^2C1-bus data input/output (not open-drain).
						O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
						-	**R_23 —** Reserved.
PIO1_15	-	-	87	[6]	I; PU	IO	**PIO1_15 —** General-purpose digital input/output pin.
						IO	**SSP0_SSEL —** Slave select for SSP0.
						O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
						-	**R_24 —** Reserved.
PIO1_16	-	-	96	[6]	I; PU	IO	**PIO1_16 —** General-purpose digital input/output pin.
						IO	**SSP0_MISO —** Master In Slave Out for SSP0.
						O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
						-	**R_25 —** Reserved.
PIO1_17	-	-	34	[6]	I; PU	IO	**PIO1_17 —** General-purpose digital input/output pin.
						I	**CT16B0_CAP2 —** Capture input 2 for 16-bit timer 0.
						I	**U0_RXD —** Receiver input for USART0.
						-	**R_26 —** Reserved.
PIO1_18	-	-	43	[6]	I; PU	IO	**PIO1_18 —** General-purpose digital input/output pin.
						I	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
						O	**U0_TXD —** Transmitter output for USART0.
						-	**R_27 —** Reserved.
PIO1_19	-	64	4	[6]	I; PU	IO	**PIO1_19 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U2\_CTS}}$ —** Clear To Send input for USART2.
						O	**SCT0_OUT0 —** SCTimer0/PWM output 0.
						-	**R_28 —** Reserved.
PIO1_20	13	18	29	[6]	I; PU	IO	**PIO1_20 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U0\_DSR}}$ —** Data Set Ready input for USART0.
						IO	**SSP1_SCK —** Serial clock for SSP1.
						O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO1_21	25	35	56	[6]	I; PU	IO	**PIO1_21 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U0\_DCD}}$ —** Data Carrier Detect input for USART0.
						IO	**SSP1_MISO —** Master In Slave Out for SSP1.
						I	**CT16B0_CAP2 —** Capture input 2 for 16-bit timer 0.
PIO1_22	-	-	80	[3]	I; PU	IO	**PIO1_22 —** General-purpose digital input/output pin.
						IO	**SSP1_MOSI —** Master Out Slave In for SSP1.
						I	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
						AI	**ADC_4 —** A/D converter, input channel 4.
						-	**R_29 —** Reserved.

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO1_23	18	23	35	[6]	I; PU	IO	**PIO1_23 —** General-purpose digital input/output pin.
						O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
						IO	**SSP1_SSEL —** Slave select for SSP1.
						O	**U2_TXD —** Transmitter output for USART2.
PIO1_24	22	28	42	[6]	I; PU	IO	**PIO1_24 —** General-purpose digital input/output pin.
						O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
						IO	**I2C1_SDA —** I^2C-bus data input/output (not open-drain).
PIO1_25	-	-	100	[6]	I; PU	IO	**PIO1_25 —** General-purpose digital input/output pin.
						O	**U2_RTS —** Request To Send output for USART2.
						IO	**U2_SCLK —** Serial clock input/output for USART2 in synchronous mode.
						I	**SCT0_IN0 —** SCTimer0/PWM input 0.
						-	**R_30 —** Reserved.
PIO1_26	-	15	20	[6]	I; PU	IO	**PIO1_26 —** General-purpose digital input/output pin.
						O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
						I	**U0_RXD —** Receiver input for USART0.
						-	**R_19 —** Reserved.
PIO1_27	-	17	22	[6]	I; PU	IO	**PIO1_27 —** General-purpose digital input/output pin.
						O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
						O	**U0_TXD —** Transmitter output for USART0.
						-	**R_20 —** Reserved.
						IO	**SSP1_SCK —** Serial clock for SSP1.
PIO1_28	-	31	46	[6]	I; PU	IO	**PIO1_28 —** General-purpose digital input/output pin.
						I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
						IO	**U0_SCLK —** Serial clock input/output for USART in synchronous mode.
						O	**U0_RTS —** Request To Send output for USART0.
PIO1_29	-	41	63	[3]	I; PU	IO	**PIO1_29 —** General-purpose digital input/output pin.
						IO	**SSP0_SCK —** Serial clock for SSP0.
						I	**CT32B0_CAP2 —** Capture input 2 for 32-bit timer 0.
						O	**U0_DTR —** Data Terminal Ready output for USART0.
						AI	**ADC_10 —** A/D converter, input channel 10.
PIO1_30	-	44	67	[6]	I; PU	IO	**PIO1_30 —** General-purpose digital input/output pin.
						IO	**I2C1_SCL —** I^2C1-bus clock input/output (not open-drain).
						I	**SCT0_IN3 —** SCTimer0/PWM input 3.
						-	**R_31 —** Reserved.
PIO1_31	-	-	48	[5]	I; PU	IO	**PIO1_31 —** General-purpose digital input/output pin (high-current output driver).

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO2_0	6	8	12	[10]	I; PU	IO	**PIO2_0 —** General-purpose digital input/output pin.
						AI	**XTALIN —** Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
PIO2_1	7	9	13	[10]	I; PU	IO	**PIO2_1 —** General-purpose digital input/output pin.
						AO	**XTALOUT —** Output from the oscillator amplifier.
PIO2_2	12	16	21	[6]	I; PU	IO	**PIO2_2 —** General-purpose digital input/output pin.
						O	**$\overline{\text{U3\_RTS}}$ —** Request To Send output for USART3.
						IO	**U3_SCLK —** Serial clock input/output for USART3 in synchronous mode.
							SCT0_OUT1 — SCTimer0/PWM output 1.
PIO2_3	-	-	36	[6]	I; PU	IO	**PIO2_3 —** General-purpose digital input/output pin.
						I	**U3_RXD —** Receiver input for USART3.
						O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO2_4	-	-	41	[6]	I; PU	IO	**PIO2_4 —** General-purpose digital input/output pin.
						O	**U3_TXD —** Transmitter output for USART3.
						O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO2_5	9	11	15	[6]	I; PU	IO	**PIO2_5 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U3\_CTS}}$ —** Clear To Send input for USART3.
						I	**SCT0_IN1 —** SCTimer0/PWM input 1.
PIO2_6	-	24	37	[6]	I; PU	IO	**PIO2_6 —** General-purpose digital input/output pin.
						O	**$\overline{\text{U1\_RTS}}$ —** Request To Send output for USART1.
						IO	**U1_SCLK —** Serial clock input/output for USART1 in synchronous mode.
						I	**SCT0_IN2 —** SCTimer0/PWM input 2.
PIO2_7	21	27	40	[6]	I; PU	IO	**PIO2_7 —** General-purpose digital input/output pin.
						IO	**SSP0_SCK —** Serial clock for SSP0.
						I	**SCT0_OUT2 —** SCTimer0/PWM output 2.
PIO2_8	-	-	2	[6]	I; PU	IO	**PIO2_8 —** General-purpose digital input/output pin.
						I	**SCT1_IN0 —** SCTimer1/PWM input 0.
PIO2_9	-	-	3	[6]	I; PU	IO	**PIO2_9 —** General-purpose digital input/output pin.
						I	**SCT1_IN1 —** SCTimer1/PWM_IN1
PIO2_10	-	-	16	[6]	I; PU	IO	**PIO2_10 —** General-purpose digital input/output pin.
						O	**$\overline{\text{U4\_RTS}}$ —** Request To Send output for USART4.
						IO	**U4_SCLK —** Serial clock input/output for USART4 in synchronous mode.
PIO2_11	-	-	24	[6]	I; PU	IO	**PIO2_11 —** General-purpose digital input/output pin.
						I	**U4_RXD —** Receiver input for USART4.
PIO2_12	-	-	25	[6]	I; PU	IO	**PIO2_12 —** General-purpose digital input/output pin.
						O	**U4_TXD —** Transmitter output for USART4.

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO2_13	-	-	26	[6]	I; PU	IO	**PIO2_13 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U4\_CTS}}$ —** Clear To Send input for USART4.
PIO2_14	-	-	27	[6]	I; PU	IO	**PIO2_14 —** General-purpose digital input/output pin.
						I	**SCT1_IN2 —** SCTimer1/PWM input 2.
PIO2_15	-	32	49	[6]	I; PU	IO	**PIO2_15 —** General-purpose digital input/output pin.
						I	**SCT1_IN3 —** SCTimer1/PWM input 3.
PIO2_16	-	-	50	[6]	I; PU	IO	**PIO2_16 —** General-purpose digital input/output pin.
						O	**SCT1_OUT0 —** SCTimer1/PWM output 0.
PIO2_17	-	-	51	[6]	I; PU	IO	**PIO2_17 —** General-purpose digital input/output pin.
						O	**SCT1_OUT1 —** SCTimer1/PWM output 1.
PIO2_18	-	33	52	[6]	I; PU	IO	**PIO2_18 —** General-purpose port 2 input/output 18.
						O	**SCT1_OUT2 —** SCTimer1/PWM output 2.
PIO2_19	-	36	57	[6]	I; PU	IO	**PIO2_19 —** General-purpose port 2 input/output 19.
						O	**SCT1_OUT3 —** SCTimer1/PWM output 3.
PIO2_20	-	-	75	[6]	I; PU	IO	**PIO2_20 —** General-purpose port 2 input/output 20.
PIO2_21	-	-	76	[6]	I; PU	IO	**PIO2_21 —** General-purpose port 2 input/output 21.
PIO2_22	-	-	77	[6]	I; PU	IO	**PIO2_22 —** General-purpose port 2 input/output 22.
PIO2_23	-	-	1	[6]	I; PU	IO	**PIO2_23 —** General-purpose port 2 input/output 23.
$\overline{\text{RSTOUT}}$	-	-	88	[6]	IA	IO	Internal reset status output.
USB_DP	20	26	39	[9]	F	-	USB bidirectional D+ line. Pad includes internal 33 Ω series termination resistor.
USB_DM	19	25	38	[9]	F	-	USB bidirectional D− line. Pad includes internal 33 Ω series termination resistor.
RTCXIN	48	1	5	[2]	-	-	RTC oscillator input. This input should be grounded if the RTC is not used.
RTCXOUT	1	2	6	[2]	-	-	RTC oscillator output.
VREFP	34	47	73		-	-	ADC positive reference voltage. If the ADC is not used, tie VREFP to V_{DD}.
VREFN	35	48	74		-	-	ADC negative voltage reference. If the ADC is not used, tie VREFN to V_{SS}.
V_{DDA}	40	53	84		-	-	Analog voltage supply. V_{DDA}should typically be the same voltages as V_{DD} but should be isolated to minimize noise and error. V_{DDA} should be tied to V_{DD} if the ADC is not used.
V_{DD}	44, 8	58, 10, 34, 59	92, 14, 71, 54, 93		-	-	Supply voltage to the internal regulator and the external rail.

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100	Reset state[1]	Type	Description of pin functions
VBAT	47	63	99	-	-	Battery supply. Supplies power to the RTC. If no battery is used, tie VBAT to VDD.
V_{SSA}	41	54	85	-	-	Analog ground. V_{SSA}should typically be the same voltage as V_{SS} but should be isolated to minimize noise and error. V_{SSA} should be tied to V_{SS} if the ADC is not used.
V_{SS}	43, 2, 5	57, 3, 7	91, 7, 11, 53, 70	-	-	Ground.

[1] Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled;
F = floating; If the pins are not used, tie floating pins to ground or power to minimize power consumption.

[2] Special analog pad.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as analog input, digital section of the pad is disabled and the pin is not 5 V tolerant; includes digital, programmable filter.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as analog input, digital section of the pad is disabled and the pin is not 5 V tolerant; includes digital input glitch filter. WAKEUP pin. The wake-up pin function can be disabled and the pin can be used for other purposes if the RTC is enabled for waking up the part from Deep power-down mode.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[7] I^2C-bus pin compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[8] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[9] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[10] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog crystal oscillator connections. When configured for the crystal oscillator input/output, digital section of the pad is disabled and the pin is not 5 V tolerant; includes digital, programmable filter.

8. Functional description

8.1 ARM Cortex-M0+ core

The ARM Cortex-M0+ core runs at an operating frequency of up to 50 MHz using a two-stage pipeline. Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The ARM Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

8.2 AHB multilayer matrix

The AHB multilayer matrix supports three masters, the M0+ core, the DMA, and the USB. All masters can access all slaves (peripherals and memories).

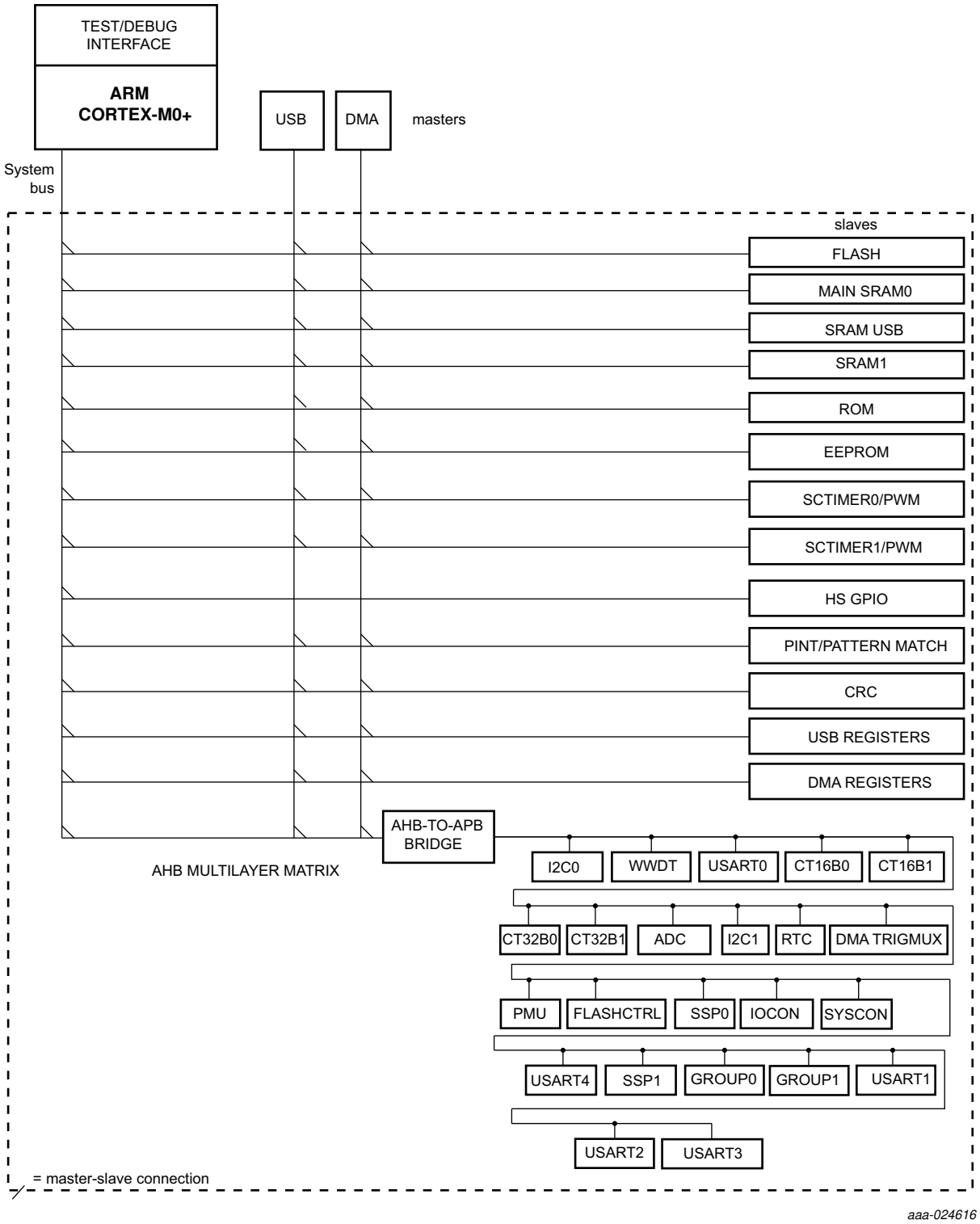


Fig 7. AHB multilayer matrix

8.3 On-chip flash programming memory

The LPC11U6x contain up to 256 KB on-chip flash program memory. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip bootloader software.

The flash memory is divided into 24 x 4 KB and 5 x 32 KB sectors. Individual pages of 256 byte each can be erased using the IAP erase page command.

8.4 EEPROM

The LPC11U6x contain 4 KB of on-chip byte-erasable and byte-programmable EEPROM data memory. The EEPROM can be programmed using In-Application Programming (IAP) via the on-chip bootloader software.

8.5 SRAM

The LPC11U6x contain a total of up to 36 KB on-chip static RAM memory. The main SRAM block contains either 8 KB, 16 KB, or 32 KB of main SRAM0. Two additional SRAM blocks of 2 KB (SRAM1 and USB SRAM) are located in separate areas of the memory map. See Figure 8.

8.6 On-chip ROM

The on-chip ROM contains the bootloader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.
- IAP support for EEPROM
- USB API
- Power profiles for configuring power consumption and PLL settings
- 32-bit integer division routines
- APIs to use the following peripherals:
  - I2C
  - USART0 and USART1/2/3/4
  - DMA

8.7 Memory mapping

The LPC11U6x incorporates several distinct memory regions, shown in the following figures. Figure 8 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB (Advanced High-performance Bus) peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB (Advanced Peripheral Bus) peripheral area is 512 KB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 KB of space. This addressing scheme allows simplifying the address decoding for each peripheral.

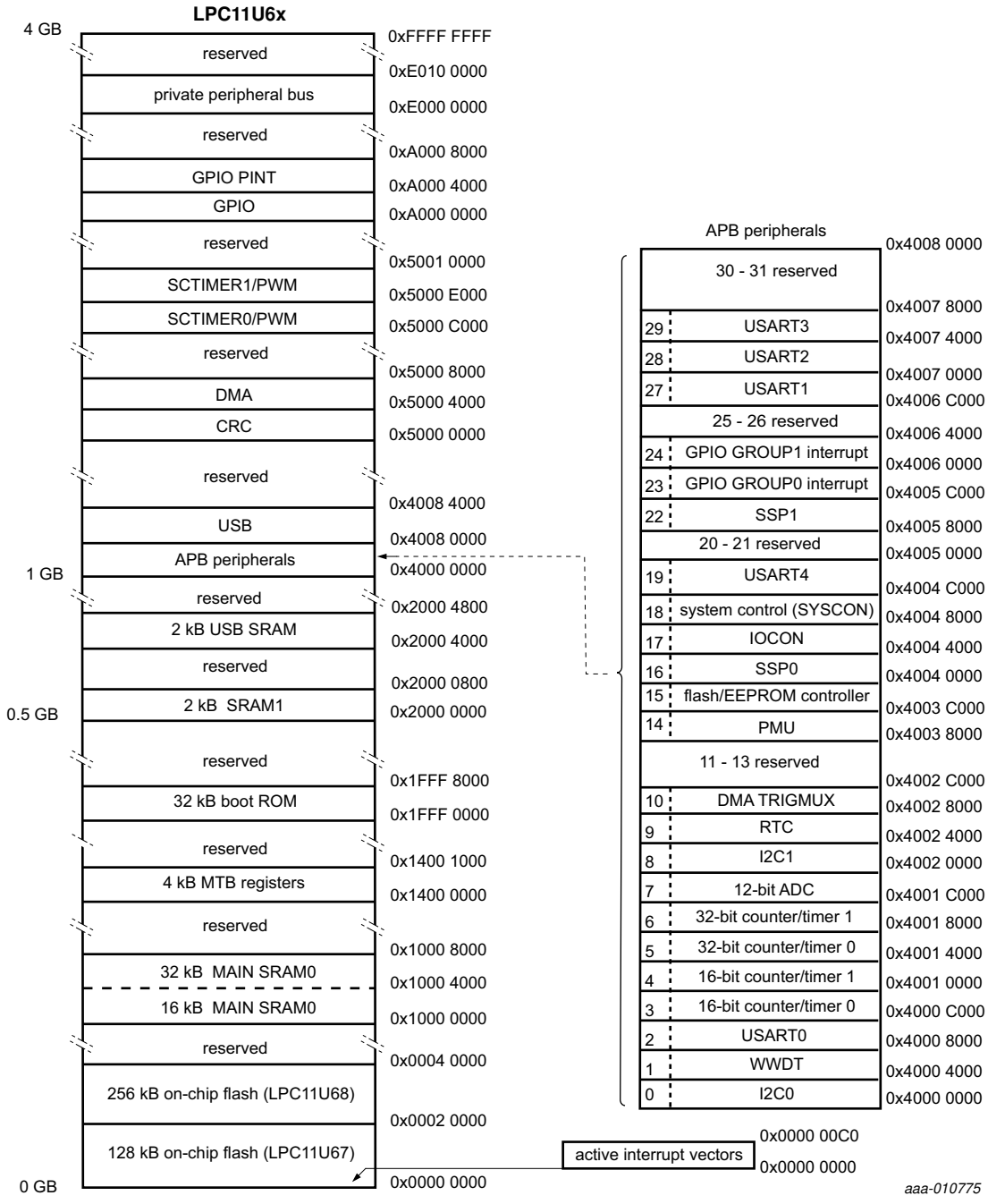


Fig 8. LPC11U6x Memory map

8.8 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.8.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC11U6x, the NVIC supports vectored interrupts for each of the peripherals and the eight pin interrupts. The following peripheral interrupts are ORed to contribute to one interrupt in the NVIC:
  - USART1, USART4
  - USART2, USART3
  - SCTimer0/PWM, SCTimer1/PWM
  - BOD, WWDT
  - ADC end-of-sequence A interrupt, threshold crossing interrupt
  - ADC end-of-sequence B interrupt, overrun interrupt
  - Flash, EEPROM
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation.

8.8.2 Interrupt sources

Each peripheral device has at least one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

8.9 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Connect peripherals to the appropriate pins before activating the peripheral and before enabling any related interrupt.

Enabling an analog function disables the digital pad. However, the internal pull-up and pull-down resistors as well as the pin hysteresis must be disabled to obtain an accurate reading of the analog input.

8.9.1 Features

- Programmable pin function.
- Programmable pull-up, pull-down, or repeater mode.
- All pins (except PIO0_4 and PIO0_5) are pulled up to 3.3 V (V_{DD} = 3.3 V) if their pull-up resistor is enabled.
- Programmable pseudo open-drain mode.
- Programmable (on/off) 10 ns glitch filter on pins PIO0_22, PIO0_23, PIO0_11 to PIO0_16, PIO1_3, PIO1_9, PIO1_22, and PIO1_29. The glitch filter is turned on by default.
- Programmable hysteresis.
- Programmable input inverter.

- Digital filter with programmable filter constant on all pins. The minimum filter constant is 1/50 MHz = 20 ns.

8.9.2 Standard I/O pad configuration

Figure 9 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input digital filter selectable on all pins. In addition, a 10 ns digital glitch filter is selectable on pins with analog function.
- Analog input

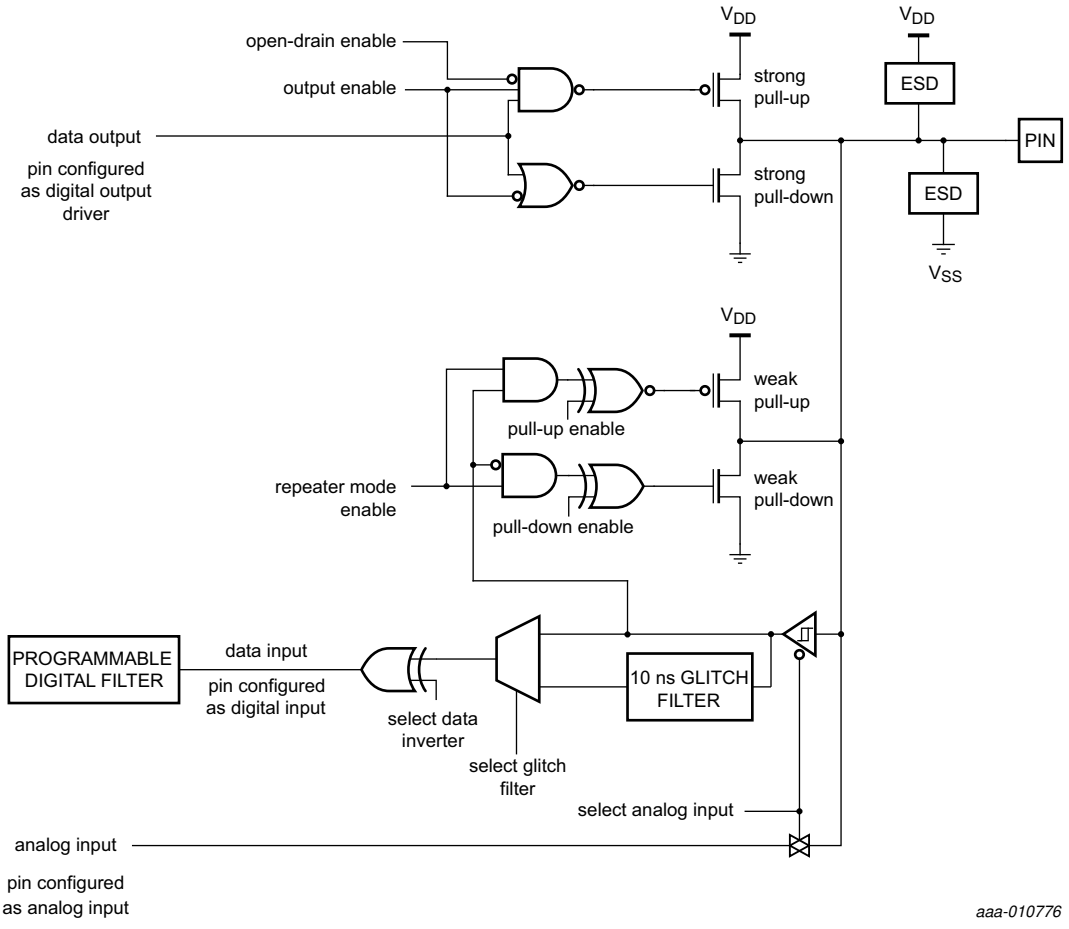


Fig 9. Standard I/O pin configuration

8.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC11U6x use accelerated GPIO functions:

- GPIO registers are on the ARM Cortex M0+ IO bus for fastest possible single-cycle I/O timing, allowing GPIO toggling with rates of up to 25 MHz.
- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

8.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.

8.11 Pin interrupt/pattern match engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

The pattern match engine can be used, in conjunction with software, to create complex state machines based on pin inputs.

Any digital pin except pins PIO2_8 and PIO2_23 can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are on the IO+ bus for fast single-cycle access.

8.11.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins except pins PIO2_8 and PIO2_23 as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the part from sleep mode, deep-sleep mode, and power-down mode.
- Pin interrupt pattern match engine
  - Up to 8 pins can be selected from all digital pins except pins PIO2_8 and PIO2_23 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can be programmed to generate an RXEV notification to the ARM CPU as well.
  - The pattern match engine does not facilitate wake-up.