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LPC82x

32-bit ARM® Cortex®-M0+ microcontroller; up to 32 kB flash and 8 kB SRAM; 12-bit ADC; comparator

Rev. 1.3 — 4 April 2018 Product data sheet

1. General description

The LPC82x are an ARM Cortex-M0+ based, low-cost 32-bit MCU family operating at CPU frequencies of up to 30 MHz. The LPC82x support up to 32 KB of flash memory and 8 KB of SRAM.

The peripheral complement of the LPC82x includes a CRC engine, four I^2C-bus interfaces, up to three USARTs, up to two SPI interfaces, one multi-rate timer, self-wake-up timer, and state-configurable timer with PWM function (SCTimer/PWM), a DMA, one 12-bit ADC and one analog comparator, function-configurable I/O ports through a switch matrix, an input pattern match engine, and up to 29 general-purpose I/O pins.

For additional documentation related to the LPC82x parts, see Section 18.

2. Features and benefits

- System:
  - ARM Cortex-M0+ processor (revision r0p1), running at frequencies of up to 30 MHz with single-cycle multiplier and fast single-cycle I/O port.
  - ARM Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC).
  - System tick timer.
  - AHB multilayer matrix.
  - Serial Wire Debug (SWD) with four break points and two watch points. JTAG boundary scan (BSDL) supported.
  - MTB
- Memory:
  - Up to 32 KB on-chip flash programming memory with 64 Byte page write and erase. Code Read Protection (CRP) supported.
  - 8 KB SRAM.
- ROM API support:
  - Boot loader.
  - On-chip ROM APIs for ADC, SPI, I2C, USART, power configuration (power profiles) and integer divide.
  - Flash In-Application Programming (IAP) and In-System Programming (ISP).
- Digital peripherals:
  - High-speed GPIO interface connected to the ARM Cortex-M0+ IO bus with up to 29 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, programmable open-drain mode, input inverter, and digital filter. GPIO direction control supports independent set/clear/toggle of individual bits.
  - High-current source output driver (20 mA) on four pins.

- High-current sink driver (20 mA) on two true open-drain pins.
- GPIO interrupt generation capability with boolean pattern-matching feature on eight GPIO inputs.
- Switch matrix for flexible configuration of each I/O pin function.
- CRC engine.
- DMA with 18 channels and 9 trigger inputs.

- Timers:
  - State Configurable Timer (SCTimer/PWM) with input and output functions (including capture and match) for timing and PWM applications. Each SCTimer/PWM input is multiplexed to allow selecting from several input sources such as pins, ADC interrupt, or comparator output.
  - Four channel Multi-Rate Timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Self-Wake-up Timer (WKT) clocked from either the IRC, a low-power, low-frequency internal oscillator, or an external clock input in the always-on power domain.
  - Windowed Watchdog timer (WWDT).
- Analog peripherals:
  - One 12-bit ADC with up to 12 input channels with multiple internal and external trigger inputs and with sample rates of up to 1.2 Msamples/s. The ADC supports two independent conversion sequences.
  - Comparator with four input pins and external or internal reference voltage.
- Serial peripherals:
  - Three USART interfaces with pin functions assigned through the switch matrix and one common fractional baud rate generator.
  - Two SPI controllers with pin functions assigned through the switch matrix.
  - Four I^2C-bus interfaces. One I2C supports Fast-mode Plus with 1 Mbit/s data rates on two true open-drain pins and listen mode. Three I2Cs support data rates up to 400 kbit/s on standard digital pins.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1.5 % accuracy that can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator, the external clock input, or the internal RC oscillator.
  - Clock output function with divider that can reflect all internal clock sources.
- Power control:
  - Power consumption in active mode as low as 90 uA/MHz in low-current mode using the IRC as the clock source.
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode.
  - Wake-up from Deep-sleep and Power-down modes on activity on USART, SPI, and I2C peripherals.
  - Timer-controlled self wake-up from Deep power-down mode.

- Power-On Reset (POR).
- Brownout detect (BOD).

- Unique device serial number for identification.
- Single power supply (1.8 V to 3.6 V).
- Operating temperature range -40 °C to +105 °C.
- Available in a TSSOP20 and HVQFN33 (5x5) package.

3. Applications

- Sensor gateways
- Industrial
- Gaming controllers
- 8/16-bit applications
- Consumer
- Climate control
- Simple motor control
- Portables and wearables
- Lighting
- Motor control
- Fire and security applications

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC824M201JHI33	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC822M101JHI33	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC824M201JDH20	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
LPC822M101JDH20	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash/ KB	SRAM/ KB	USART	I^2C	SPI	ADC channels	Comparator	GPIO	Package
LPC824M201JHI33	32	8	3	4	2	12	Y	29	HVQFN33
LPC822M101JHI33	16	4	3	4	2	12	Y	29	HVQFN33
LPC824M201JDH20	32	8	3	4	2	5	Y	16	TSSOP20
LPC822M101JDH20	16	4	3	4	2	5	y	16	TSSOP20

5. Marking

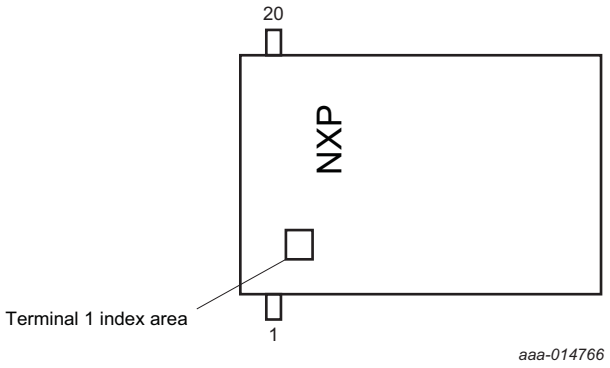


Fig 1. TSSOP20 package marking

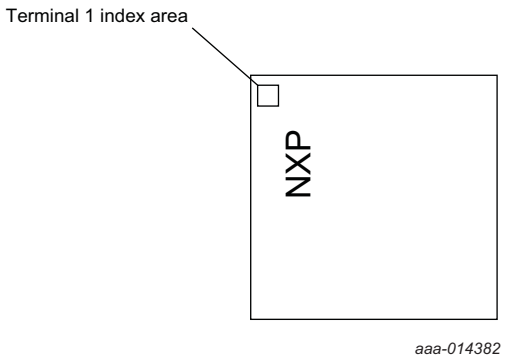


Fig 2. HVQFN33 package marking

The HVQFN33 packages typically have the following top-side marking:

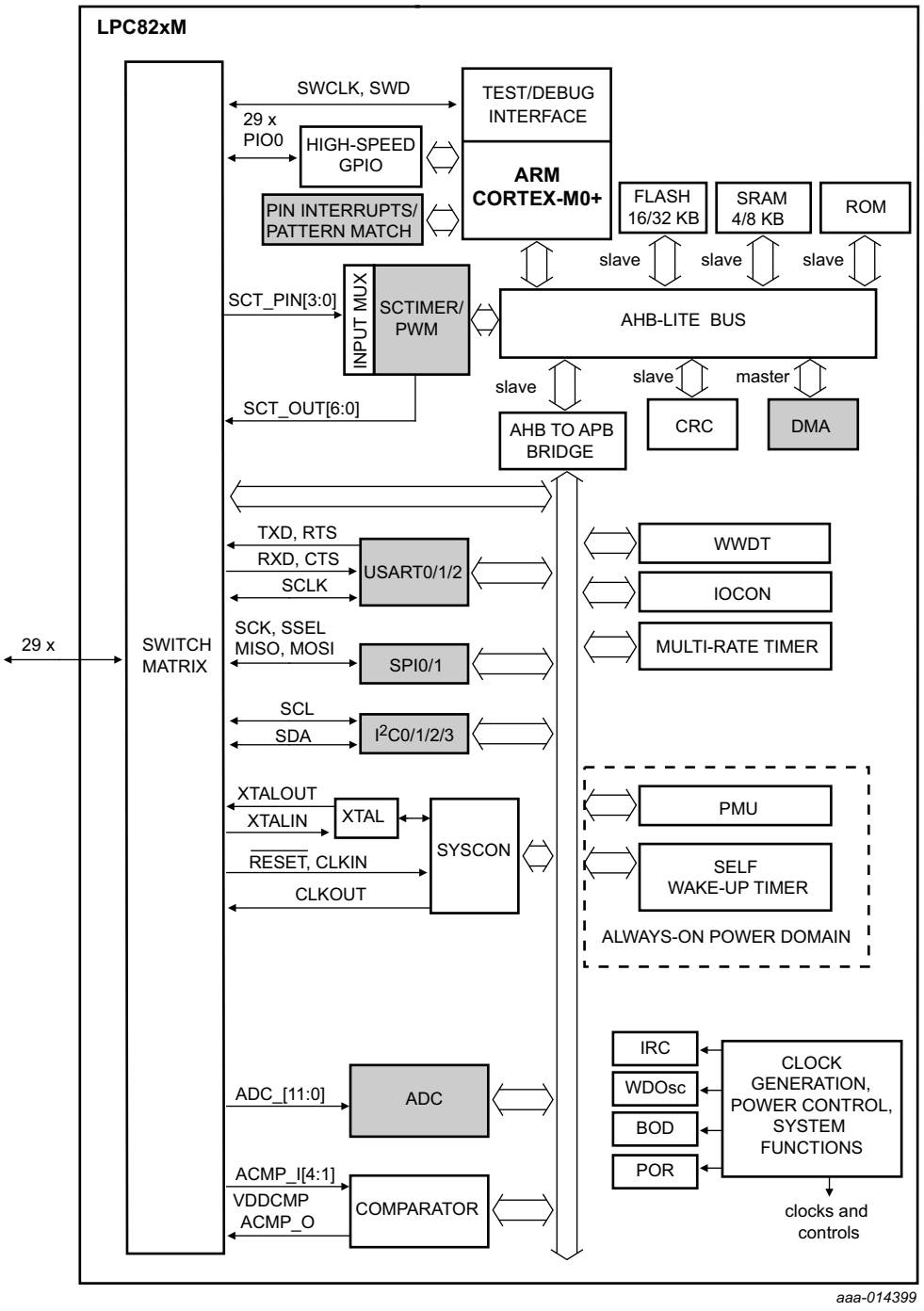
82xJ
xx xx
yywwxR

The TSSOP20 packages typically have the following top-side marking:

LPC82x
Mx01J
xxxxxxxx
zzywwxR

In the last line, field ‘y’ or ‘yy’ states the year the device was manufactured. Field ‘ww’ states the week the device was manufactured during that year. Field ‘R’ states the chip revision.

6. Block diagram



Gray-shaded blocks show peripherals that can provide hardware triggers or fixed DMA requests for DMA transfers.

Fig 3. LPC82x block diagram

7. Pinning information

7.1 Pinning

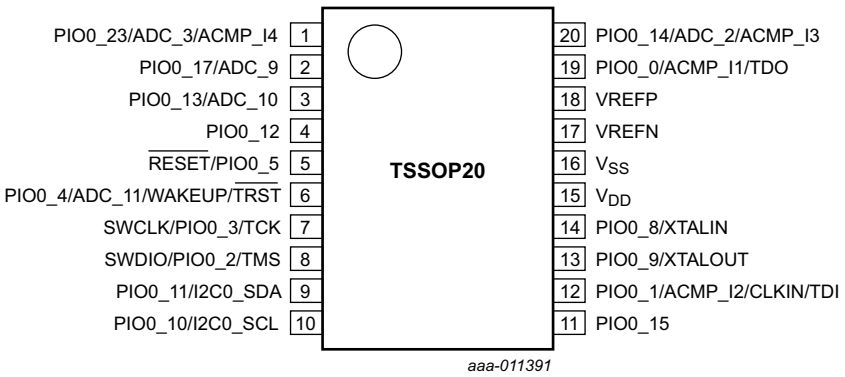


Fig 4. Pin configuration TSSOP20 package

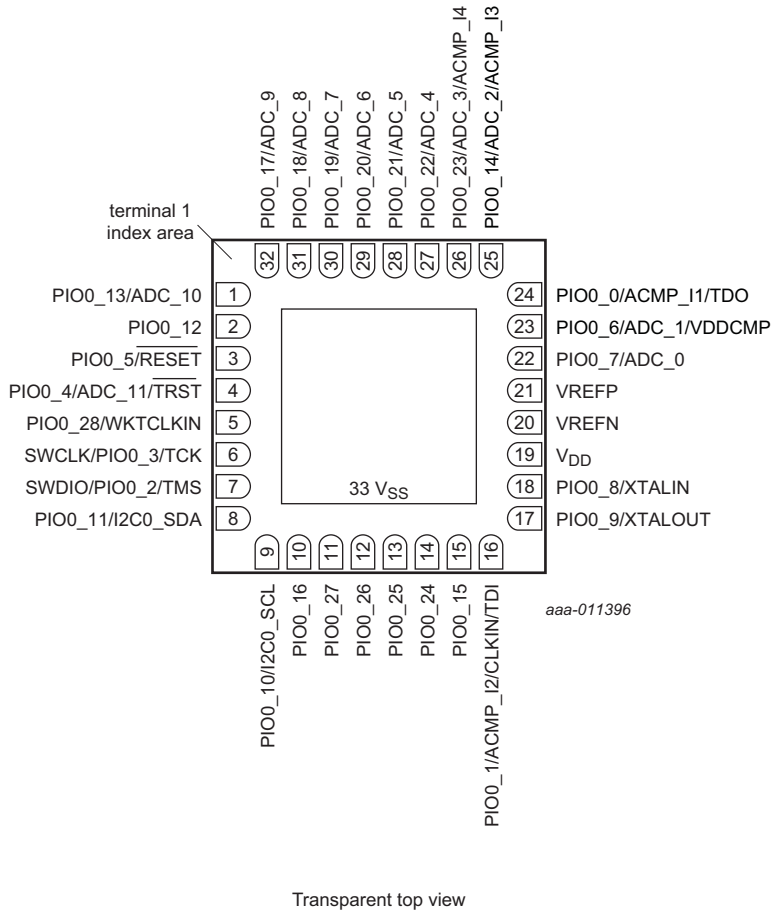


Fig 5. Pin configuration HVQFN33 package

7.2 Pin description

The pin description table Table 3 shows the pin functions that are fixed to specific pins on each package. These fixed-pin functions are selectable through the switch matrix between GPIO and the comparator, ADC, SWD, $\overline{\text{RESET}}$, and the XTAL pins. By default, the GPIO function is selected except on pins PIO0_2, PIO0_3, and PIO0_5. JTAG functions are available in boundary scan mode only.

Movable function for the I2C, USART, SPI, and SCT pin functions can be assigned through the switch matrix to any pin that is not power or ground in place of the pin's fixed functions.

The following exceptions apply:

Do not assign more than one output to any pin. However, more than one input can be assigned to a pin. Once any function is assigned to a pin, the pin's GPIO functionality is disabled.

Pin PIO0_4 triggers a wake-up from Deep power-down mode. If the part must wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin.

The JTAG functions TDO, TDI, TCK, TMS, and $\overline{\text{TRST}}$ are selected on pins PIO0_0 to PIO0_4 by hardware when the part is in boundary scan mode.

Table 3. Pin description

Symbol	TSSOP20	HVQFN33		Reset state[1]	Type	Description
PIO0_0/ACMP_I1/ TDO	19	24	[2]	I; PU	IO	**PIO0_0 —** General-purpose port 0 input/output 0. In ISP mode, this is the U0_RXD pin. In boundary scan mode: TDO (Test Data Out).
					A	**ACMP_I1 —** Analog comparator input 1.
PIO0_1/ACMP_I2/ CLKIN/TDI	12	16	[2]	I; PU	IO	**PIO0_1 —** General-purpose port 0 input/output 1. In boundary scan mode: TDI (Test Data In).
					A	**ACMP_I2 —** Analog comparator input 2.
					I	**CLKIN —** External clock input.
SWDIO/PIO0_2/ TMS	8	7	[4]	I; PU	IO	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
					I/O	**PIO0_2 —** General-purpose port 0 input/output 2.
SWCLK/PIO0_3/ TCK	7	6	[4]	I; PU	I	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
					IO	**PIO0_3 —** General-purpose port 0 input/output 3.

Table 3. Pin description

Symbol	TSSOP20	HVQFN33		Reset state[1]	Type	Description
PIO0_4/ADC_11/ TRSTN/WAKEUP	6	4	[3]	I; PU	IO	**PIO0_4 —** General-purpose port 0 input/output 4. In boundary scan mode: $\overline{\text{TRST}}$ (Test Reset). In ISP mode, this pin is the U0_TXD pin. This pin triggers a wake-up from Deep power-down mode. If the part must wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin. This pin should be pulled HIGH externally before entering Deep power-down mode. A LOW-going pulse as short as 50 ns causes the chip to exit Deep power-down mode and wakes up the part.
					A	**ADC_11 —** ADC input 11.
$\overline{\text{RESET}}$/PIO0_5	5	3	[7]	I; PU	IO	**$\overline{\text{RESET}}$ —** External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO or for any movable function if an external $\overline{\text{RESET}}$ function is not needed and the Deep power-down mode is not used.
					I	**PIO0_5 —** General-purpose port 0 input/output 5.
PIO0_6/ADC_1/ VDDCMP	-	23	[10]	I; PU	IO	**PIO0_6 —** General-purpose port 0 input/output 6.
					A	**ADC_1 —** ADC input 1.
					A	**VDDCMP —** Alternate reference voltage for the analog comparator.
PIO0_7/ADC_0	-	22	[2]	I; PU	IO	**PIO0_7 —** General-purpose port 0 input/output 7.
					A	**ADC_0 —** ADC input 0.
PIO0_8/XTALIN	14	18	[8]	I; PU	IO	**PIO0_8 —** General-purpose port 0 input/output 8.
					A	**XTALIN —** Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.95 V.
PIO0_9/XTALOUT	13	17	[8]	I; PU	IO	**PIO0_9 —** General-purpose port 0 input/output 9.
					A	**XTALOUT —** Output from the oscillator circuit.
PIO0_10/I2C0_SCL	10	9	[6]	Inactive	I; F	**PIO0_10 —** General-purpose port 0 input/output 10 (open-drain).
						I2C0_SCL — Open-drain I^2C-bus clock input/output. High-current sink if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_11/I2C0_SDA	9	8	[6]	Inactive	I; F	**PIO0_11 —** General-purpose port 0 input/output 11 (open-drain).
						I2C0_SDA — Open-drain I^2C-bus data input/output. High-current sink if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_12	4	2	[4]	I; PU	IO	**PIO0_12 —** General-purpose port 0 input/output 12. ISP entry pin. A LOW level on this pin during reset starts the ISP command handler.
PIO0_13/ADC_10	3	1	[2]	I; PU	IO	**PIO0_13 —** General-purpose port 0 input/output 13.
					A	**ADC_10 —** ADC input 10.

Table 3. Pin description

Symbol	TSSOP20	HVQFN33		Reset state[1]	Type	Description
PIO0_14/ ACMP_I3/ADC_2	20	25	[2]	I; PU	IO	**PIO0_14 —** General-purpose port 0 input/output 14.
					A	**ACMP_I3 —** Analog comparator common input 3.
					A	**ADC_2 —** ADC input 2.
PIO0_15	11	15	[5]	I; PU	IO	**PIO0_15 —** General-purpose port 0 input/output 15.
PIO0_16	-	10	[4]	I; PU	IO	**PIO0_16 —** General-purpose port 0 input/output 16.
PIO0_17/ADC_9	2	32	[2]	I; PU	IO	**PIO0_17 —** General-purpose port 0 input/output 17.
					A	**ADC_9 —** ADC input 9.
PIO0_18/ADC_8	-	31	[2]	I; PU	IO	**PIO0_18 —** General-purpose port 0 input/output 18.
					A	**ADC_8 —** ADC input 8.
PIO0_19/ADC_7	-	30	[2]	I; PU	IO	**PIO0_19 —** General-purpose port 0 input/output 19.
					A	**ADC_7 —** ADC input 7.
PIO0_20/ADC_6	-	29	[2]	I; PU	IO	**PIO0_20 —** General-purpose port 0 input/output 20.
					A	**ADC_6 —** ADC input 6.
PIO0_21/ADC_5	-	28	[2]	I; PU	IO	**PIO0_21 —** General-purpose port 0 input/output 21.
					A	**ADC_5 —** ADC input 5.
PIO0_22/ADC_4	-	27	[2]	I; PU	IO	**PIO0_22 —** General-purpose port 0 input/output 22.
					A	**ADC_4 —** ADC input 4.
PIO0_23/ADC_3/ ACMP_I4	1	26	[2]	I; PU	IO	**PIO0_23 —** General-purpose port 0 input/output 23.
					A	**ADC_3 —** ADC input 3.
					A	**ACMP_I4 —** Analog comparator common input 4.
PIO0_24	-	14	[5]	I; PU	IO	**PIO0_24 —** General-purpose port 0 input/output 24.
PIO0_25	-	13	[5]	I; PU	IO	**PIO0_25 —** General-purpose port 0 input/output 25.
PIO0_26	-	12	[5]	I; PU	IO	**PIO0_26 —** General-purpose port 0 input/output 26.
PIO0_27	-	11	[5]	I; PU	IO	**PIO0_27 —** General-purpose port 0 input/output 27.
PIO0_28/ WKTCLKIN	-	5	[3]	I; PU	IO	**PIO0_28 —** General-purpose port 0 input/output 28. This pin can host an external clock for the self-wake-up timer. To use the pin as a self-wake-up timer clock input, select the external clock in the wake-up timer CTRL register. The external clock input is active in all power modes, including deep power-down.
V_{DD}	15	19		-	-	Supply voltage for the I/O pad ring, the core voltage regulator, and the analog peripherals.
V_{SS}	16	33[11]		-	-	Ground.
VREFN	17	20		-	-	ADC negative reference voltage.
VREFP	18	21		-	-	ADC positive reference voltage. Must be equal or lower than V_{DD}.

[1] Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled; F = floating. For pin states in the different power modes, see Section 14.5 “Pin states in different power modes”. For termination on unused pins, see Section 14.4 “Termination of unused pins”.

[2] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis. This pin is active in Deep power-down mode and includes a 20 ns glitch filter (active in all power modes). In Deep power-down mode, pulling the WAKEUP pin LOW wakes up the chip. The wake-up pin function can be disabled and the pin can be used for other purposes, if the WKT low-power oscillator is enabled for waking up the part from Deep power-down mode. See Table 17 “Dynamic characteristics: WKTCLKIN pin” for the WKTCLKIN input.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[6] True open-drain pin. I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. Do not use this pad for high-speed applications such as SPI or USART. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[7] See Figure 10 for the reset pad configuration. This pin includes a 20 ns glitch filter (active in all power modes). $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[8] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog I/O for the system oscillator. When configured for XTALIN and XTALOUT, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[9] The WKTCLKIN function is enabled in the DPDCTRL register in the PMU. See the LPC82x user manual.

[10] The digital part of this pin is 3 V tolerant pin due to special analog functionality. Pin provides standard digital I/O functions with configurable modes, configurable hysteresis, and an analog input. When configured as an analog input, the digital section of the pin is disabled.

[11] Thermal pad for HVQFN33.

Table 4. Movable functions (assign to pins PIO0_0 to PIO0_28 through switch matrix)

Function name	Type	Description
U0_TXD	O	Transmitter output for USART0.
U0_RXD	I	Receiver input for USART0.
$\overline{\text{U0\_RTS}}$	O	Request To Send output for USART0.
$\overline{\text{U0\_CTS}}$	I	Clear To Send input for USART0.
U0_SCLK	I/O	Serial clock input/output for USART0 in synchronous mode.
U1_TXD	O	Transmitter output for USART1.
U1_RXD	I	Receiver input for USART1.
$\overline{\text{U1\_RTS}}$	O	Request To Send output for USART1.
$\overline{\text{U1\_CTS}}$	I	Clear To Send input for USART1.
U1_SCLK	I/O	Serial clock input/output for USART1 in synchronous mode.
U2_TXD	O	Transmitter output for USART2.
U2_RXD	I	Receiver input for USART2.
$\overline{\text{U2\_RTS}}$	O	Request To Send output for USART1.
$\overline{\text{U2\_CTS}}$	I	Clear To Send input for USART1.
U2_SCLK	I/O	Serial clock input/output for USART1 in synchronous mode.
SPI0_SCK	I/O	Serial clock for SPI0.
SPI0_MOSI	I/O	Master Out Slave In for SPI0.
SPI0_MISO	I/O	Master In Slave Out for SPI0.
SPI0_SSEL0	I/O	Slave select 0 for SPI0.
SPI0_SSEL1	I/O	Slave select 1 for SPI0.
SPI0_SSEL2	I/O	Slave select 2 for SPI0.
SPI0_SSEL3	I/O	Slave select 3 for SPI0.
SPI1_SCK	I/O	Serial clock for SPI1.

Table 4. Movable functions (assign to pins PIO0_0 to PIO0_28 through switch matrix)

Function name	Type	Description
SPI1_MOSI	I/O	Master Out Slave In for SPI1.
SPI1_MISO	I/O	Master In Slave Out for SPI1.
SPI1_SSEL0	I/O	Slave select 0 for SPI1.
SPI1_SSEL1	I/O	Slave select 1 for SPI1.
SCT_PIN0	I	Pin input 0 to the SCT input multiplexer.
SCT_PIN1	I	Pin input 1 to the SCT input multiplexer.
SCT_PIN2	I	Pin input 2 to the SCT input multiplexer.
SCT_PIN3	I	Pin input 3 to the SCT input multiplexer.
SCT_OUT0	O	SCT output 0.
SCT_OUT1	O	SCT output 1.
SCT_OUT2	O	SCT output 2.
SCT_OUT3	O	SCT output 3.
SCT_OUT4	O	SCT output 4.
SCT_OUT5	O	SCT output 5.
I2C1_SDA	I/O	I^2C1-bus data input/output.
I2C1_SCL	I/O	I^2C1-bus clock input/output.
I2C2_SDA	I/O	I^2C2-bus data input/output.
I2C2_SCL	I/O	I^2C2-bus clock input/output.
I2C3_SDA	I/O	I^2C3-bus data input/output.
I2C3_SCL	I/O	I^2C3-bus clock input/output.
ADC_PINTRIG0	I	ADC external pin trigger input 0.
ADC_PINTRIG1	I	ADC external pin trigger input 1.
ACMP_O	O	Analog comparator output.
CLKOUT	O	Clock output.
GPIO_INT_BMAT	O	Output of the pattern match engine.

8. Functional description

8.1 ARM Cortex-M0+ core

The ARM Cortex-M0+ core runs at an operating frequency of up to 30 MHz using a two-stage pipeline. The core revision is r0p1.

Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The ARM Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

8.2 On-chip flash program memory

The LPC82x contain up to 32 KB of on-chip flash program memory. The flash memory supports a 64 Byte page size with page write and erase.

8.3 On-chip SRAM

The LPC82x contain a total of 8 KB on-chip static RAM data memory in two separate SRAM blocks with one combined clock for both SRAM blocks.

8.4 On-chip ROM

The on-chip ROM contains the bootloader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.
- Power profiles for configuring power consumption and PLL settings
- 32-bit integer division routines
- APIs to use the following peripherals:
  - SPI
  - USART
  - I2C
  - ADC

8.5 Memory map

The LPC82x incorporates several distinct memory regions. Figure 6 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The ARM private peripheral bus includes the ARM core registers for controlling the NVIC, the system tick timer (SysTick), and the reduced power modes.

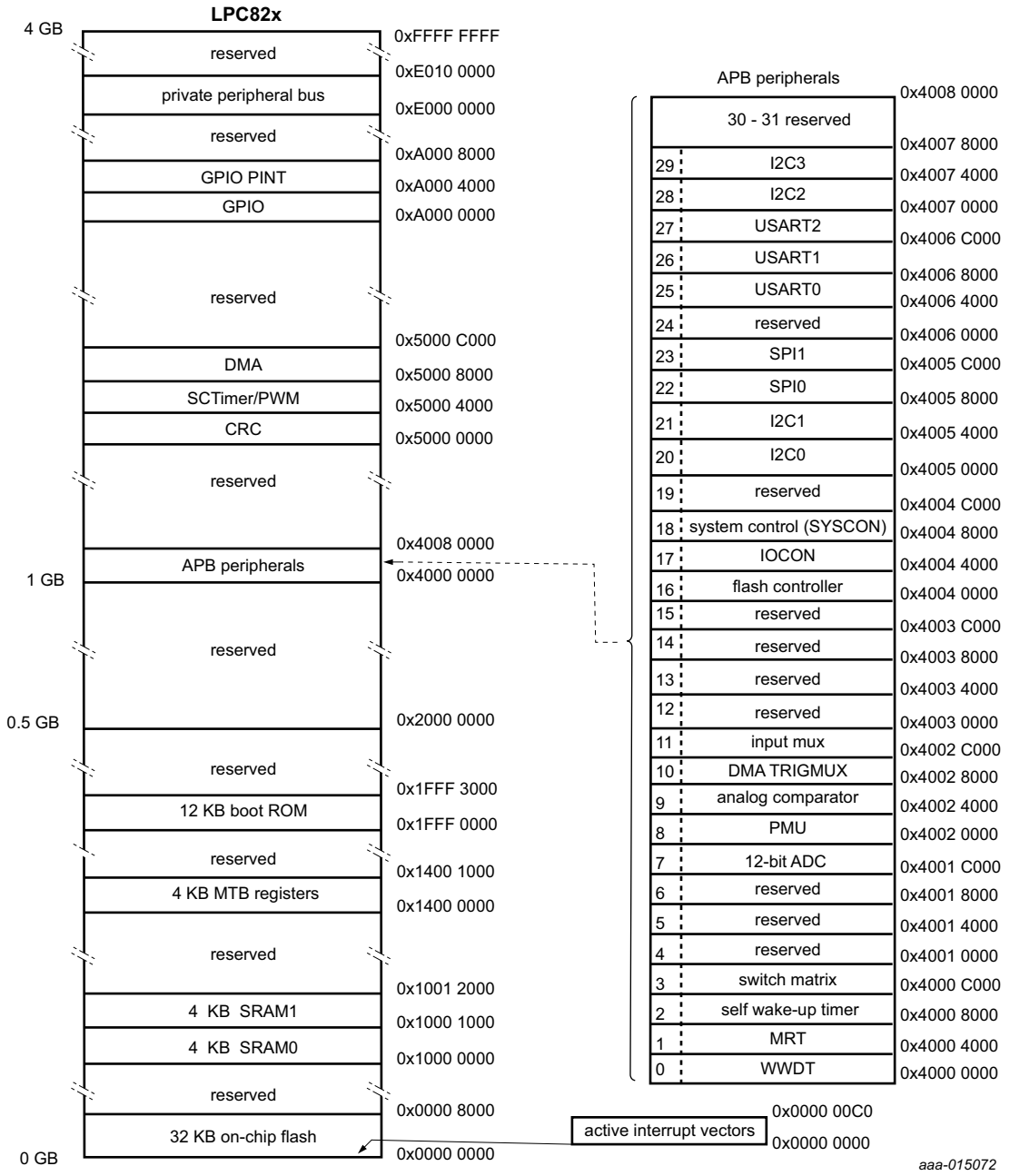


Fig 6. LPC82x Memory mapping

8.6 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.6.1 Features

- Nested Vectored Interrupt Controller is a part of the ARM Cortex-M0+.

- Tightly coupled interrupt controller provides low interrupt latency.
- Controls system exceptions and peripheral interrupts.
- Supports 32 vectored interrupts.
- In the LPC82x, the NVIC supports vectored interrupts for each of the peripherals and the eight pin interrupts.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the ARM exceptions SVCall and PendSV.
- Supports NMI.

8.6.2 Interrupt sources

Each peripheral device has at least one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

8.7 System tick timer

The ARM Cortex-M0+ includes a 24-bit system tick timer (SysTick) that is intended to generate a dedicated SysTick exception at a fixed time interval (typically 10 ms).

8.8 I/O configuration

The IOCON block controls the configuration of the I/O pins. Each digital or mixed digital/analog pin with the PIO0_n designator (except the true open-drain pins PIO0_10 and PIO0_11) in Table 3 can be configured as follows:

- Enable or disable the weak internal pull-up and pull-down resistors.
- Select a pseudo open-drain mode. The input cannot be pulled up above V_{DD}. The pins are not 5 V tolerant when V_{DD} is grounded.
- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see Figure 9 “LPC82x clock generation”). You can also bypass the glitch filter.
- Invert the input signal.
- Hysteresis can be enabled or disabled.
- For pins PIO0_10 and PIO0_11, select the I2C-mode and output driver for standard digital operation, for I2C standard and fast modes, or for I2C Fast mode+.
- The switch matrix setting enables the analog input mode on pins with analog and digital functions. Enabling the analog mode disconnects the digital functionality.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See Section 8.9 for details.

8.8.1 Standard I/O pad configuration

Figure 7 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output.
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled.
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled.

- Digital input: Repeater mode enabled/disabled.
- Digital input: Programmable input digital filter selectable on all pins.
- Analog input: Selected through the switch matrix.

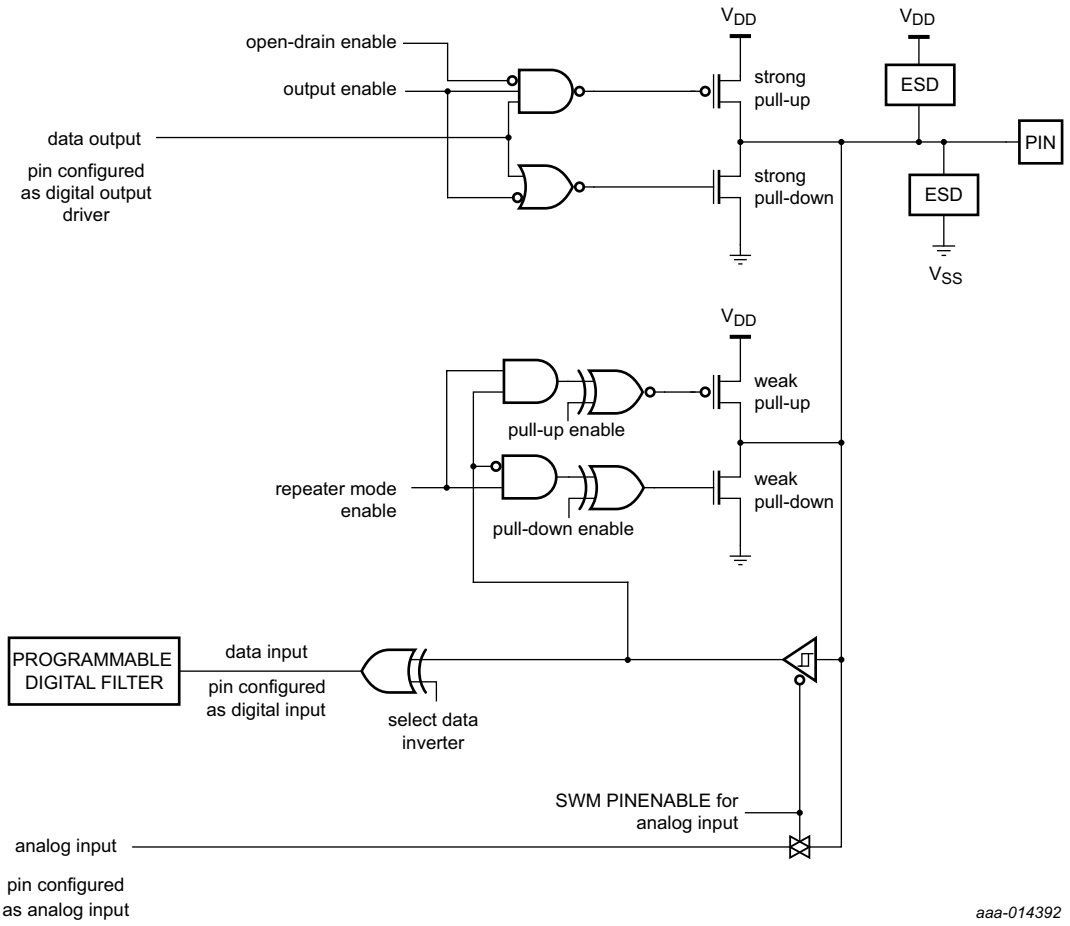


Fig 7. Standard I/O pad configuration

8.9 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, SCT, and I2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 4.

Functions that need specialized pads like the oscillator pins XTALIN and XTALOUT can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Table 3. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

8.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC82x use accelerated GPIO functions:

- GPIO registers are on the ARM Cortex-M0+ IO bus for fastest possible single-cycle I/O timing, allowing GPIO toggling with rates of up to 15 MHz.
- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin. Except for pins SWDIO/PIO0_2, SWCLK/PIO0_3, and RESET/PIO0_5, the switch matrix enables the GPIO port pin function by default.

8.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to GPIO inputs with internal pull-up resistors enabled after reset - except for the I^2C-bus true open-drain pins PIO0_10 and PIO0_11.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 7).
- Direction (input/output) can be set and cleared individually.
- Pin direction bits can be toggled.

8.11 Pin interrupt/pattern match engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

The pattern match engine can be used, with software, to create complex state machines based on pin inputs.

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are on the IO+ bus for fast single-cycle access.

8.11.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.

- Pin interrupts can wake up the LPC82x from sleep mode, deep-sleep mode, and power-down mode.

- Pin interrupt pattern match engine
  - Up to eight pins can be selected from all digital pins to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can be also programmed to generate an RXEV notification to the ARM CPU. The RXEV signal can be connected to a pin.
  - The pattern match engine does not facilitate wake-up.

8.12 DMA controller

The DMA controller can access all memories and the USART, SPI, I2C, and ADC peripherals using DMA requests or triggers. DMA transfers can also be triggered by internal events like the ADC interrupts, the pin interrupts (PININT0 and PININT1), the SCTimer DMA requests, and the DMA trigger outputs.

8.12.1 Features

- 18 channels with each channel connected to peripheral request inputs.
- DMA operations can be triggered by on-chip events or by two pin interrupts. Each DMA channel can select one trigger input from 9 sources.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache with two entries.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

8.12.2 DMA trigger input MUX (TRIGMUX)

Each DMA trigger is connected to a programmable multiplexer which connects the trigger input to one of multiple trigger sources. Each multiplexer supports the same trigger sources: the ADC sequence interrupts, the SCT DMA request lines, and pin interrupts PININT0 and PININT1, and the outputs of the DMA triggers 0 and 1 for chaining DMA triggers.

8.13 USART0/1/2

All USART functions are movable functions and are assigned to pins through the switch matrix.

8.13.1 Features

- Maximum bit rates of 1.875 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode for USART functions connected to all digital pins except the open-drain pins.

- 7, 8, or 9 data bits and 1 or 2 stop bits
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare. (RS-485 possible with software address detection and transceiver direction control.)
- Parity generation and checking: odd, even, or none.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator.
- A fractional rate divider is shared among all UARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Separate data and flow control loopback modes for testing.
- Baud rate clock can also be output in asynchronous mode.
- Supported by on-chip ROM API.

8.14 SPI0/1

All SPI functions are movable functions and are assigned to pins through the switch matrix.

8.14.1 Features

- Maximum data rates of up to 30 Mbit/s in master mode and up to 18 Mbit/s in slave mode for SPI functions connected to all digital pins except the open-drain pins.
- Data frames of 1 to 16 bits supported directly. Larger frames supported by software.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data, which can be useful while setting up an SPI memory.
- Control information can optionally be written along with data, which allows very versatile operation, including “any length” frames.
- One Slave Select input/output with selectable polarity and flexible usage.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

8.15 I2C-bus interface (I2C0/1/2/3)

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the

capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master.

The I2C0-bus functions are fixed-pin functions. All other I2C-bus functions for I2C1/2/3 are movable functions and can be assigned through the switch matrix to any pin. However, only the true open-drain pins provide the electrical characteristics to support the full I2C-bus specification (see Ref. 3).

8.15.1 Features

- I2C0 supports Fast-mode Plus with data rates of up to 1 Mbit/s in addition to standard and fast modes on two true open-drain pins.
- True open-drain pins provide fail-safe operation: When the power to an I^2C-bus device is switched off, the SDA and SCL pins connected to the I^2C0-bus are floating and do not disturb the bus.
- I2C1/2/3 support standard and fast mode with data rates of up to 400 kbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I^2C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I^2C bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.

8.16 SCTimer/PWM

The state configurable timer can perform basic 16-bit and 32-bit timer/counter functions with match outputs and external and internal capture inputs. In addition, the SCTimer/PWM can employ up to eight different programmable states, which can change under the control of events, to provide complex timing patterns.

The inputs to the SCT are multiplexed between movable functions from the switch matrix and internal connections such as the ADC threshold compare interrupt, the comparator output, and the ARM core signals ARM_TXEV and DEBUG_HALTED. The signal on each SCT input is selected through the INPUT MUX.

All outputs of the SCT are movable functions and are assigned to pins through the switch matrix. One SCT output can also be selected as one of the ADC conversion triggers.

8.16.1 Features

- Each SCTimer/PWM supports:
  - Eight match/capture registers.
  - Eight events.
  - Eight states.

- Four inputs. Each input is configurable through an input multiplexer to use one of four external pins (connected through the switch matrix) or one of four internal sources. The maximum input signal frequency is 25 MHz.
- Six outputs. Connected to pins through the switch matrix.

- Counter/timer features:
  - Each SCTimer is configurable as two 16-bit counters or one 32-bit counter.
  - Counters can be clocked by the system clock or selected input.
  - Configurable as up counters or up-down counters.
  - Configurable number of match and capture registers. Up to eight match and capture registers total.
  - Upon match create the following events: interrupt; stop, limit, halt the timer or change counting direction; toggle outputs.
  - Counter value can be loaded into capture register triggered by a match or input/output toggle.
- PWM features:
  - Counters can be used with match registers to toggle outputs and create time-proportioned PWM signals.
  - Up to six single-edge or dual-edge PWM outputs with independent duty cycle and common PWM cycle length.
- Event creation features:
  - The following conditions define an event: a counter match condition, an input (or output) condition such as a rising or falling edge or level, a combination of match and/or input/output condition.
  - Selected events can limit, halt, start, or stop a counter or change its direction.
  - Events trigger state changes, output toggles, interrupts, and DMA transactions.
  - Match register 0 can be used as an automatic limit.
  - In bidirectional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- State control features:
  - A state is defined by events that can happen in the state while the counter is running.
  - A state changes into another state as a result of an event.
  - Each event can be assigned to one or more states.
  - State variable allows sequencing across multiple counter cycles.
- One SCTimer match output can be selected as ADC hardware trigger input.

8.16.2 SCTimer/PWM input MUX (INPUT MUX)

Each input of the SCTimer/PWM is connected to a programmable multiplexer which allows to connect one of multiple internal or external sources to the input. The available sources are the same for each SCTimer/PWM input and can be selected from four pins configured through the switch matrix, the ADC threshold compare interrupt, the comparator output, and the ARM core signals ARM_TXEV and DEBUG_HALTED.

8.17 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

8.17.1 Features

- 31-bit interrupt timer
- Four channels independently counting down from individually set values
- Bus stall, repeat and one-shot interrupt modes

8.18 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to service the watchdog timer periodically within a programmable time window.

8.18.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WatchDog Clock (WDCLK) is generated by the dedicated watchdog oscillator (WDOSC).

8.19 Self-Wake-up Timer (WKT)

The self-wake-up timer is a 32-bit, loadable down counter. Writing any non-zero value to this timer automatically enables the counter and launches a count-down sequence. When the counter is used as a wake-up timer, this write can occur prior to entering a reduced power mode.

8.19.1 Features

- 32-bit loadable down counter. Counter starts automatically when a count value is loaded. Time-out generates an interrupt/wake up request.
- The WKT resides in a separate, always-on power domain.
- The WKT supports three clock sources: an external clock on the WKTCLKIN pin, the low-power oscillator, and the IRC. The low-power oscillator is located in the always-on power domain, so it can be used as the clock source in Deep power-down mode.

- The WKT can be used for waking up the part from any reduced power mode, including Deep power-down mode, or for general-purpose timing.

8.20 Analog comparator (ACMP)

The analog comparator with selectable hysteresis can compare voltage levels on external pins and internal voltages.

After power-up and after switching the input channels of the comparator, the output of the voltage ladder must be allowed to settle to its stable value before it can be used as a comparator reference input. Settling times are given in Table 25.

The analog comparator output is a movable function and is assigned to a pin through the switch matrix. The comparator inputs and the voltage reference are enabled through the switch matrix.

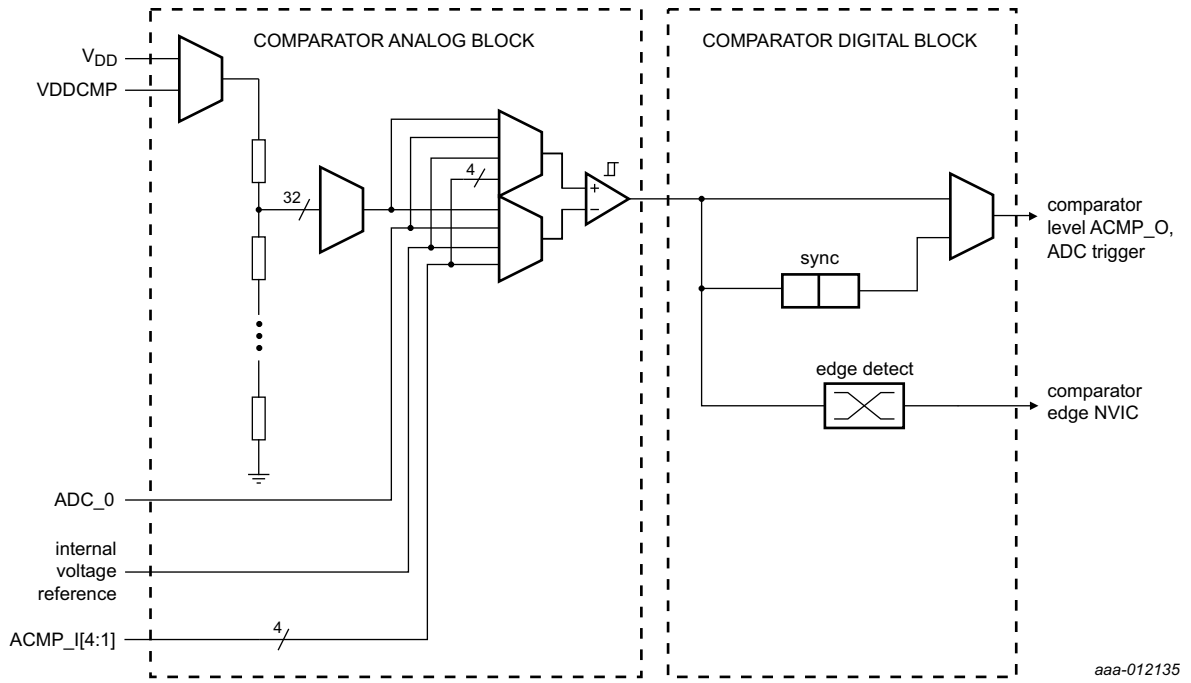


Fig 8. Comparator block diagram

8.20.1 Features

- Selectable 0 mV, 10 mV (± 5 mV), and 20 mV (± 10 mV), 40 mV (± 20 mV) input hysteresis.
- Two selectable external voltages (V_{DD} or VDDCMP on pin PIO0_6); fully configurable on either positive or negative input channel.
- Internal voltage reference from band gap selectable on either positive or negative input channel.
- 32-stage voltage ladder with the internal reference voltage selectable on either the positive or the negative input channel.

- Voltage ladder source voltage is selectable from an external pin or the main 3.3 V supply voltage rail.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Interrupt output is connected to NVIC.
- Comparator level output is connected to output pin ACMP_O.
- One comparator output is internally collected to the ADC trigger input multiplexer.

8.21 Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12 bit and fast conversion rates of up to 1.2 MSamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the pin triggers, the SCT output SCT_OUT3, the analog comparator output, and the ARM TXEV.

The ADC includes a hardware threshold compare function with zero-crossing detection.

Remark: For best performance, select VREFP and VREFN at the same voltage levels as V_{DD} and V_{SS}. When selecting VREFP and VREFN different from VDD and VSS, ensure that the voltage midpoints are the same:

(VREFP-VREFN)/2 + VREFN = V_{DD}/2

8.21.1 Features

- 12-bit successive approximation analog to digital converter.
- 12-bit conversion rate of up to 1.2 MSamples/s.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and zero-crossing detection.
- Power-down mode and low-power operating mode.
- Measurement range VREFN to VREFP (not to exceed V_{DD} voltage level).
- Burst conversion mode for single or multiple inputs.
- Hardware calibration mode.

8.22 Clocking and power control

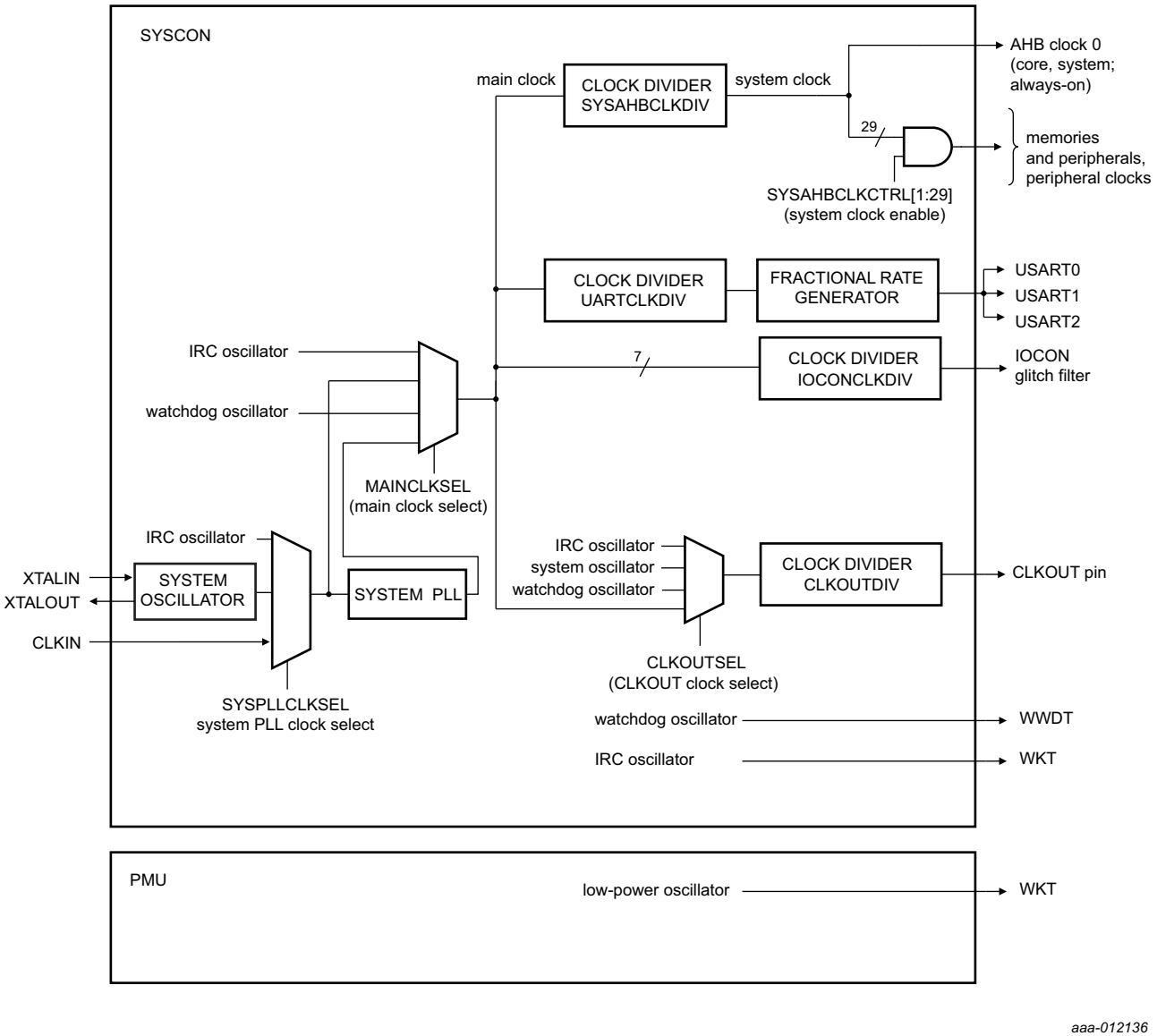


Fig 9. LPC82x clock generation

8.22.1 Crystal and internal oscillators

The LPC82x include four independent oscillators:

1. The crystal oscillator (SysOsc) operating at frequencies between 1 MHz and 25 MHz.
2. The internal RC Oscillator (IRC) with a fixed frequency of 12 MHz.
3. The internal low-power, low-frequency Oscillator with a nominal frequency of 10 kHz with 40% accuracy for use with the self-wake-up timer.
4. The dedicated Watchdog Oscillator (WDOsc) with a programmable nominal frequency between 9.4 kHz and 2.3 MHz with 40% accuracy.

Each oscillator, except the low-frequency oscillator, can be used for more than one purpose as required in a particular application.

Following reset, the LPC82x operates from the IRC until switched by software allowing the part to run without any external crystal and the bootloader code to operate at a known frequency.

See Figure 9 for an overview of the LPC82x clock generation.

8.22.1.1 Internal RC Oscillator (IRC)

The IRC may be used as the clock source for the WWDT, and/or as the clock that drives the PLL and then the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1.5 % accuracy over the entire voltage and temperature range.

The IRC can be used as a clock source for the CPU with or without using the PLL. The IRC frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

Upon power-up or any chip reset, the LPC82x use the IRC as the clock source. Software may later switch to one of the other available clock sources.

8.22.1.2 Crystal Oscillator (SysOsc)

The crystal oscillator can be used as the clock source for the CPU, with or without using the PLL.

The SysOsc operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

8.22.1.3 Internal Low-power Oscillator and Watchdog Oscillator (WDOsc)

The nominal frequency of the WDOsc is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over silicon process variations is ± 40%.

The WDOsc is a dedicated oscillator for the windowed WWDT.

The internal low-power 10 kHz (± 40% accuracy) oscillator serves as the clock input to the WKT. This oscillator can be configured to run in all low-power modes.

8.22.2 Clock input

An external clock source can be supplied on the selected CLKIN pin directly to the PLL input. When selecting a clock signal for the CLKIN pin, follow the specifications for digital I/O pins in Table 8 “Static characteristics, supply pins” and Table 16 “Dynamic characteristics: I/O pins[1]”.

An 1.8 V external clock source can be supplied on the XTALIN pins to the system oscillator limiting the voltage of this signal (see Section 14.1).

The maximum frequency for both clock signals is 25 MHz.

8.22.3 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within