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UM10539

NVT2003DP, NVT2004TL and NVT2006PW demo boards

Rev. 1 — 7 March 2012 **User manual**

Document information

Info	Content
Keywords	NVT, voltage translator, level translator, level shift, passive voltage translator, passive level translator, passive level shift, I2C-bus, SMBus, SPI, NVT2003, NVT2004, NVT2006
Abstract	NXP Voltage Translators (NVT) are used in bidirectional signaling voltage level translation applications for I/O buses with incompatible logic levels. The NVT2003, NVT2004, and NVT2006 are three-, four- and six-channel voltage translators, operational from 1.0 V to 3.6 V at $V_{CC(A)}$ (low voltage side) and from 1.8 V to 5.5 V at $V_{CC(B)}$ (high voltage side) without directional control for open-drain or push-pull I/O devices.

Revision history

Rev	Date	Description
v.1	20120307	user manual; initial version

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1. Introduction

The NVT2003DP (OM13319), NVT2004TL (OM13316) and NVT2006PW (OM13323) demo boards are designed to evaluate the NXP 3-channel, 4-channel and 6-channel bidirectional voltage level translators. The demo boards interface between device I/Os operating at different voltage levels. Since the NVT2003DP, NVT2004TL and NVT2006PW devices are passive devices, pull-up resistors may be needed depending on the I/O interface type (totem pole or open-drain), difference in translation voltage, and the translation direction (high to low voltage, low to high voltage, or bidirectional). The NVT2003DP, NVT2004TL and NVT2006PW devices allow translations between any voltages from 1.0 V to 5.5 V.

Please refer to NVT2003/04/06 data sheet (Ref. 1) and application note *AN11127 (*Ref. 2) for more detailed information.

019aac708

a. NVT2003DP (OM13319)

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b. NVT2004TL (OM13316)

019aac710

c. NVT2006PW (OM13323)

Fig 1. Bidirectional voltage level translators demo boards

2. Hardware description

2.1 Schematic

The demo boards contain footprints for the NVT2003DP, NVT2004TL and NVT2006PW, where the jumpers, headers, and passive components are shared. The NVT2003DP, NVT2004TL and NVT2006PW demo board schematic is shown in Figure 2. Pin 2 and pin 3 on J1 need to be shorted to enable the part. Pin 1 and pin 8 on J3 are power and GND for the low voltage side. Pin 1 and pin 8 on J4 are power and GND for the high voltage side. All Bn I/O pins on the right side have 10 kΩ pull-up resistors to VREFB and all An I/O pins on the left side have 10 kΩ pull-up resistors to VREFA through jumper J2. A shunt needs to be installed at J2 if VREFB − VREFA < 1 V. If VREFB − VREFA ≥ 1 V, then the J2 should be open and resistors R2 through R7 must be removed. If they are not removed, then a resistive path exists between the A-side I/Os that can impact the efficiency and signal integrity of the solution.

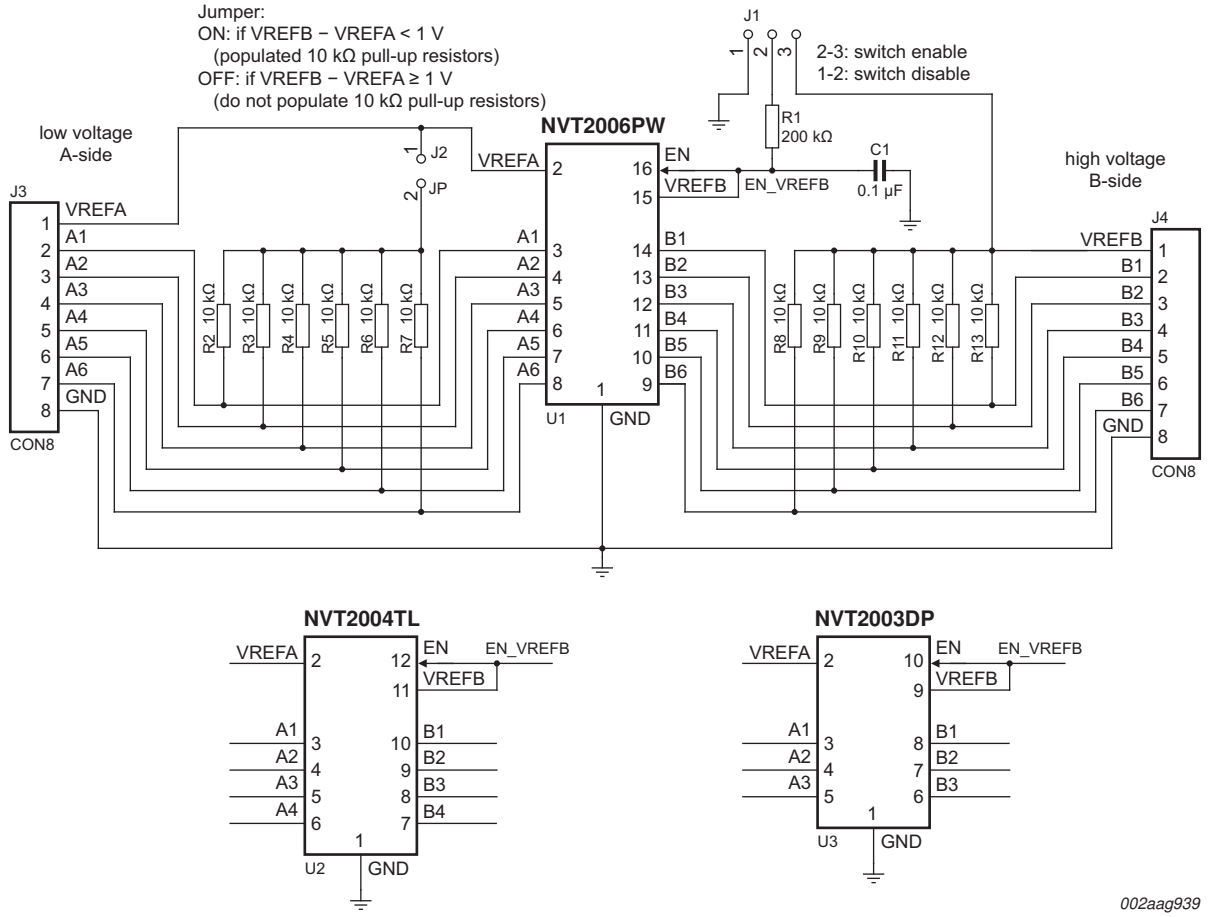

Fig 2. NVT2003DP, NVT2004TL and NVT2006PW demo board schematic

2.2 Jumper and header functions

The functions of the jumpers and headers on this demo board are shown in Table 1.

Table 1. Header descriptions for NVT2003DP (OM13319), NVT2004TL (OM13316) or NVT2006PW (OM13323) demo boards

Jumper/header	Function	Notes
J1 (3-pin)	Device switch enable or disable control	Short pins 2 and 3 to enable the NVT2003DP, NVT2004TL or NVT2006PW device (default). When pins 1 and 2 are shorted, the device is disabled.
J2 (2-pin)	Connects 10 kΩ pull-up resistors to VREFA on low voltage side for VREFB – VREFA < 1 V	Short pins 1 and 2 to connect 10 kΩ pull-up resistors to VREFA on low voltage side. **Remark:** Pins 1 and 2 must be open and 10 kΩ pull-up resistors must be removed when VREFB – VREFA ≥ 1 V.
J3 (8-pin)	Low voltage VREFA, GND and An I/O signal connect pins	Pin 1 = VREFA: low voltage power. Pin 8 = GND: low voltage ground. A[1:3] are low voltage signals for NVT2003DP. A[1:4] are low voltage signals for NVT2004TL. A[1:6] are low voltage signals for NVT2006PW.
J4 (8-pin)	High voltage VREFB, GND and Bn I/O signal connect pins	Pin 1 = VREFB: high voltage power. Pin 8 = GND: high voltage ground. B[1:3] are high voltage signals for NVT2003DP. B[1:4] are high voltage signals for NVT2004TL. B[1:6] are high voltage signals for NVT2006PW.

3. Abbreviations

Table 2. Abbreviations

Acronym	Description
I^2C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
SPI	Serial Peripheral Interface
SMBus	System Management Bus

4. References

[1] **NVT2003/04/06, "Bidirectional voltage-level translator for open-drain and push-pull applications" —** Product data sheet; NXP Semiconductors; www.nxp.com/documents/data_sheet/NVT2003_04_06.pdf

[2] **AN11127, "Bidirectional voltage level translators NVT20xx, PCA9306, GTL2000, GTL2002, GTL2003, GTL2010" —** application note; NXP Semiconductors; www.nxp.com/documents/application_note/AN11127.pdf

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