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PCU9955

16-channel UFm I²C-bus 57 mA constant current LED driver

Rev. 2.1 — 29 June 2015 Product data sheet

1. General description

The PCU9955 is an Ultra-Fast mode (UFm) I²C-bus controlled 16-channel constant current LED driver optimized for dimming and blinking 57 mA Red/Green/Blue/Amber (RGBA) LEDs in amusement products. Each LEDn output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 31.25 kHz with a duty cycle that is adjustable from 0 % to 99.6 % to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 122 Hz and an adjustable frequency between 15 Hz to once every 16.8 seconds with a duty cycle that is adjustable from 0 % to 99.6 % that is used to either dim or blink all LEDs with the same value.

Each LEDn output can be off, on (no PWM control), set at its individual PWM controller value or at both individual and group PWM controller values. The PCU9955 operates with a supply voltage range of 3 V to 5.5 V and the constant current sink LEDn outputs allow up to 40 V for the LED supply. The output current is adjustable with an 8-bit linear DAC from 225 μA to 57 mA.

This device has built-in open, short load and overtemperature detection circuitry. The thermal shutdown feature protects the device when internal junction temperature exceeds the limit allowed for the process.

The PCU9955 device is the first LED controller device in a new Ultra Fast-mode (UFm) I²C-bus family. UFm I²C-bus devices offer higher frequency (up to 5 MHz). The UFm I²C-bus slave devices operate in receive-only mode. That is, only I²C writes to PCU9955 are supported. As such, there are no status registers in PCU9955. The PCU9955 allows significantly higher data transfer rate compared to the Fast-mode Plus versions (PCA9952/55).

Software programmable LED Group and three Sub Call I²C-bus addresses allow all or defined groups of PCU9955 devices to respond to a common I²C-bus address, allowing for example, all red LEDs to be turned on or off at the same time, thus minimizing I²C-bus commands. On power-up, PCU9955 will have a unique Sub Call address to identify it as a 16-channel LED driver. This allows mixing of devices with different channel widths. Four hardware address pins on PCU9955 allow up to 16 devices on the same bus.

The Software Reset (SWRST) function allows the master to perform a reset of the PCU9955 through the I²C-bus, identical to the Power-On Reset (POR) that initializes the registers to their default state causing the output current switches to be OFF (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.

2. Features and benefits

- 16 LED drivers. Each output programmable at:
  - Off
  - On
  - Programmable LED brightness
  - Programmable group dimming/blinking mixed with individual LED brightness
  - Programmable LEDn output enable delay to reduce EMI and surge currents
- 16 constant current output channels can sink up to 57 mA, tolerate up to 40 V when OFF
- Output current adjusted through an external resistor
- Output current accuracy
  - ±6 % between output channels
  - ±8 % between PCU9955 devices
- Thermal shutdown for overtemperature
- 5 MHz Ultra Fast-mode compatible I²C-bus interface
- 256-step (8-bit) linear programmable brightness per LEDn output varying from fully off (default) to maximum brightness using a 31.25 kHz PWM signal
- 256-step group brightness control allows general dimming (using a 122 Hz PWM signal) from fully off to maximum brightness (default)
- 256-step group blinking programmable from 15 Hz to 16.8 s and duty cycle from 0 % to 99.6 %
- Output state change programmable on the Acknowledge (bit 9, this bit is always set to 1 by I²C-bus master) or the STOP Command to update outputs byte-by-byte or all at the same time (default to 'Change on STOP').
- 4 hardware address pins allow 16 PCU9955 devices to be connected to the same I²C-bus and to be individually programmed
- 4 software programmable I²C-bus addresses (one LED Group Call address and three LED Sub Call addresses) allow groups of devices to be addressed at the same time in any combination (for example, one register used for 'All Call' so that all the PCU9955s on the I²C-bus can be addressed at the same time and the second register used for three different addresses so that 1/3 of all devices on the bus can be addressed at the same time in a group). Software enable and disable for each programmable I²C-bus address.
- Unique power-up default Sub Call address allows mixing of devices with different channel widths
- Software Reset feature (SWRST Call) allows the device to be reset through the I²C-bus
- 8 MHz internal oscillator requires no external components
- Internal power-on reset
- Noise filter on USDA/USCL inputs
- No glitch on LEDn outputs on power-up
- Low standby current
- Operating power supply voltage (V_{DD}) range of 3 V to 5.5 V
- 5.5 V tolerant inputs on non-LED pins
- −40 °C to +85 °C operation

- ESD protection exceeds 2000 V HBM per JESD22-A114 and 750 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 Class II, Level B
- Package offered: HTSSOP28

3. Applications

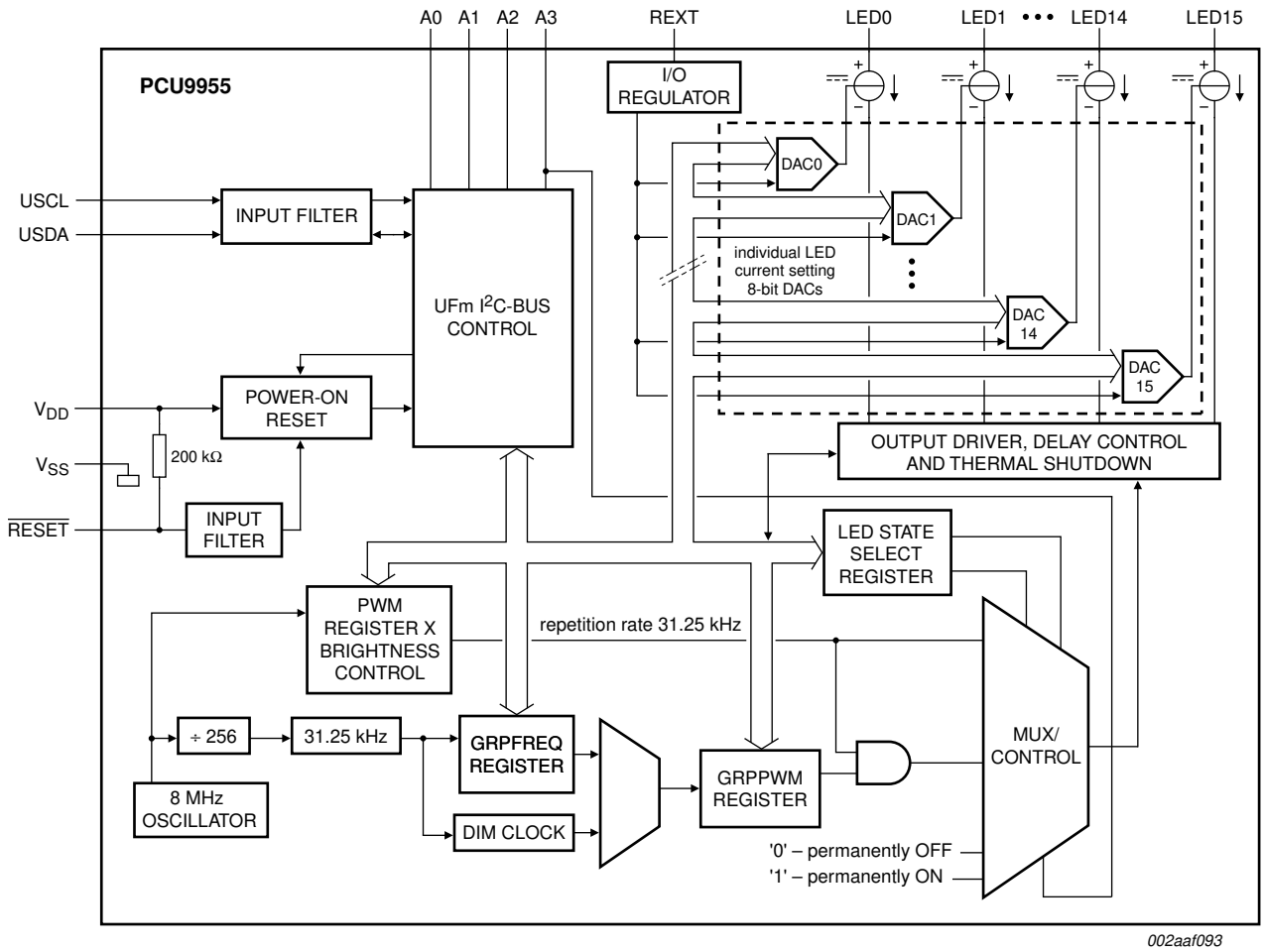
- Amusement products
- RGB or RGBA LED drivers
- LED status information
- LED displays
- LCD backlights
- Keypad backlights for cellular phones or handheld devices

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCU9955TW	PCU9955	HTSSOP28	plastic thermal enhanced thin shrink small outline package; 28 leads; body width 4.4 mm; lead pitch 0.65 mm; exposed die pad	SOT1172-2

5. Block diagram



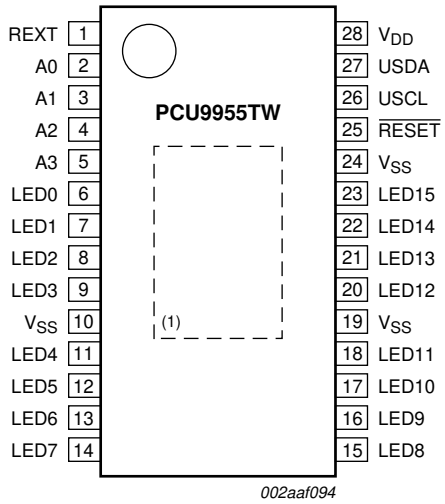
Dim repetition rate = 122 Hz.

Blink repetition rate = 15 Hz to every 16.8 seconds.

Fig 1. Block diagram of PCU9955

6. Pinning information

6.1 Pinning



(1) Thermal pad; connected to V_{SS}.

Fig 2. Pin configuration for HTSSOP28

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
REXT	1	I	current set resistor input; resistor to ground
A0	2	I	address input 0[1]
A1	3	I	address input 1[1]
A2	4	I	address input 2[1]
A3	5	I	address input 3[1]
LED0	6	O	LED driver 0
LED1	7	O	LED driver 1
LED2	8	O	LED driver 2
LED3	9	O	LED driver 3
LED4	11	O	LED driver 4
LED5	12	O	LED driver 5
LED6	13	O	LED driver 6
LED7	14	O	LED driver 7
LED8	15	O	LED driver 8
LED9	16	O	LED driver 9
LED10	17	O	LED driver 10
LED11	18	O	LED driver 11
LED12	20	O	LED driver 12

Table 2. Pin description *...continued*

Symbol	Pin	Type	Description
LED13	21	O	LED driver 13
LED14	22	O	LED driver 14
LED15	23	O	LED driver 15
$\overline{\text{RESET}}$	25	I	active LOW reset input
USCL	26	I	UFm serial clock line
USDA	27	I	UFm serial data line
V_{SS}	10, 19, 24[2]	ground	supply ground
V_{DD}	28	power supply	supply voltage

[1] In order to obtain the best system level ESD performance, a standard pull-up resistor (10 kΩ typical) is required for any address pin connecting to V_{DD}. For additional information on system level ESD performance, please refer to application notes AN10897 and AN11131.

[2] HTSSOP28 package supply ground is connected to both V_{SS} pins and exposed center pad. V_{SS} pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

7. Functional description

Refer to Figure 1 “Block diagram of PCU9955”.

7.1 Device addresses

Following a START condition, the bus master must output the address of the slave it is accessing.

For PCU9955 there are a maximum of 16 possible programmable addresses using the 4 hardware address pins.

7.1.1 Regular I²C-bus slave address

The I²C-bus slave address of the PCU9955 is shown in Figure 3. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW externally.

Remark: Reserved I²C-bus addresses must be used with caution since they can interfere with:

- ‘reserved for future use’ I²C-bus addresses (0000 011, 1111 1XX)
- slave devices that use the 10-bit addressing scheme (1111 0XX)
- slave devices that are designed to respond to the General Call address (0000 000)
- High-speed mode (Hs-mode) master code (0000 1XX)

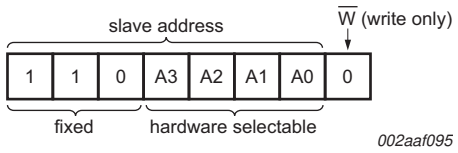


Fig 3. PCU9955 slave address

The last bit of the address byte defines the operation to be performed. Only writes to PCU9955 are supported, therefore the last bit is set to 0.

7.1.2 LED All Call I²C-bus address

- Default power-up value (ALLCALLADR register): E0h or 1110 000X
- Programmable through I²C-bus (volatile programming)
- At power-up, LED All Call I²C-bus address is enabled.

See Section 7.3.10 “ALLCALLADR, LED All Call I²C-bus address” for more detail.

Remark: The default LED All Call I²C-bus address (E0h or 1110 000X) must not be used as a regular I²C-bus slave address since this address is enabled at power-up. All of the PCU9955s on the UFm I²C-bus will respond to the address if sent by the I²C-bus master.

7.1.3 LED bit Sub Call I²C-bus addresses

- 3 different I²C-bus addresses can be used
- Default power-up values:
  - SUBADR1 register: ECh or 1110 110X
  - SUBADR2 register: ECh or 1110 110X
  - SUBADR3 register: ECh or 1110 110X
- Programmable through UFm I²C-bus (volatile programming)
- At power-up, SUBADR1 is enabled while SUBADR2 and SUBADR3 I²C-bus addresses are disabled.

Remark: At power-up SUBADR1 identifies this device as a 16-channel driver.

See Section 7.3.9 “LED bit Sub Call I²C-bus addresses for PCU9955” for more detail.

7.2 Control register

Following the slave address, LED All Call address or LED Sub Call address, the bus master will send a byte to the PCU9955, which will be stored in the Control register.

The lowest 7 bits are used as a pointer to determine which register will be accessed (D[6:0]). The highest bit is used as Auto-Increment Flag (AIF). The AIF is active by default at power-up.

This bit along with the MODE1 register bit 5 and bit 6 provide the Auto-Increment feature.

When the Auto-Increment Flag is set (AIF = logic 1), the seven low order bits of the Control register are automatically incremented after a write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values of MODE1 register.

reset state = 80h

Remark: The Control register does not apply to the Software Reset I²C-bus address.

Fig 4. Control register

Table 3. Auto-Increment options

AIF	AI1[1]	AI0[1]	Function
0	0	0	no Auto-Increment
1	0	0	Auto-Increment for registers (00h to 41h). D[6:0] roll over to 00h after the last register 41h is accessed.
1	0	1	Auto-Increment for individual brightness registers only (0Ah to 19h). D[6:0] roll over to 0Ah after the last register (19h) is accessed.
1	1	0	Auto-Increment for MODE1 to IREF15 control registers (00h to 31h). D[6:0] roll over to 00h after the last register (31h) is accessed.
1	1	1	Auto-Increment for global control registers and individual brightness registers (08h to 19h). D[6:0] roll over to 08h after the last register (19h) is accessed.

[1] AI1 and AI0 come from MODE1 register.

Remark: Other combinations not shown in Table 3 (AIF + AI[1:0] = 001b, 010b and 011b) are reserved and must not be used for proper device operation.

AIF + AI[1:0] = 000b is used when the same register must be accessed several times during a single I²C-bus communication, for example, changes the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

AIF + AI[1:0] = 100b is used when registers 00h to 41h must be sequentially accessed, for example, power-up programming.

AIF + AI[1:0] = 101b is used when the 16 LED drivers must be individually programmed with different values during the same I²C-bus communication, for example, changing color setting to another color setting.

AIF + AI[1:0] = 110b is used when MODE1 to IREF15 registers must be programmed with different settings during the same I²C-bus communication.

AIF + AI[1:0] = 111b is used when the 16 LED drivers must be individually programmed with different values in addition to global programming.

Only the 7 least significant bits D[6:0] are affected by the AIF, AI1 and AI0 bits.

When the Control register is written, the register entry point determined by D[6:0] is the first register that will be addressed and can be anywhere between 00h and 41h (as defined in Table 4). When AIF = 1, the Auto-Increment Flag is set and the rollover value at which the register increment stops and goes to the next one is determined by AIF, AI1 and AI0. See Table 3 for rollover values. For example, if MODE1 register bit AI1 = 0 and AI0 = 1 and if the Control register = 1001 0000, then the register addressing sequence will be (in hexadecimal): 10 → 11 → … → 19 → 0A → 0B → … → 19 → 0A → 0B → … as long as the master keeps sending data.

If MODE1 register bit AI1 = 0 and AI0 = 0 and if the Control register = 1010 0010, then the register addressing sequence will be (in hexadecimal):
22 → 23 → … → 41 → 00 → 01 → … → 19 → 0A → 0B → … as long as the master keeps sending data.

If MODE1 register bit AI1 = 0 and AI0 = 1 and if the Control register = 1000 0101, then the register addressing sequence will be (in hexadecimal):
05 → 06 → … → 19 → 0A → 0B → … → 19 → 0A → 0B → … as long as the master keeps sending data.

Remark: Writing to registers marked ‘not used’ will be ignored.

7.3 Register definitions

Table 4. Register summary

Register number (hexadecimal)	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
00h	0	0	0	0	0	0	0	MODE1	write only	Mode register 1
01h	0	0	0	0	0	0	1	MODE2	write only	Mode register 2
02h	0	0	0	0	0	1	0	LEDOUT0	write only	LEDn output state 0
03h	0	0	0	0	0	1	1	LEDOUT1	write only	LEDn output state 1
04h	0	0	0	0	1	0	0	LEDOUT2	write only	LEDn output state 2
05h	0	0	0	0	1	0	1	LEDOUT3	write only	LEDn output state 3
06h	0	0	0	0	1	1	0	-	write only	not used[1]
07h	0	0	0	0	1	1	1	-	write only	not used[1]
08h	0	0	0	1	0	0	0	GRPPWM	write only	group duty cycle control
09h	0	0	0	1	0	0	1	GRPFREQ	write only	group frequency
0Ah	0	0	0	1	0	1	0	PWM0	write only	brightness control LED0
0Bh	0	0	0	1	0	1	1	PWM1	write only	brightness control LED1
0Ch	0	0	0	1	1	0	0	PWM2	write only	brightness control LED2
0Dh	0	0	0	1	1	0	1	PWM3	write only	brightness control LED3
0Eh	0	0	0	1	1	1	0	PWM4	write only	brightness control LED4
0Fh	0	0	0	1	1	1	1	PWM5	write only	brightness control LED5
10h	0	0	1	0	0	0	0	PWM6	write only	brightness control LED6
11h	0	0	1	0	0	0	1	PWM7	write only	brightness control LED7
12h	0	0	1	0	0	1	0	PWM8	write only	brightness control LED8
13h	0	0	1	0	0	1	1	PWM9	write only	brightness control LED9
14h	0	0	1	0	1	0	0	PWM10	write only	brightness control LED10

Table 4. Register summary *…continued*

Register number (hexadecimal)	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
15h	0	0	1	0	1	0	1	PWM11	write only	brightness control LED11
16h	0	0	1	0	1	1	0	PWM12	write only	brightness control LED12
17h	0	0	1	0	1	1	1	PWM13	write only	brightness control LED13
18h	0	0	1	1	0	0	0	PWM14	write only	brightness control LED14
19h	0	0	1	1	0	0	1	PWM15	write only	brightness control LED15
1Ah to 21h	-	-	-	-	-	-	-	-	write only	not used[1]
22h	0	1	0	0	0	1	0	IREF0	write only	output gain control register 0
23h	0	1	0	0	0	1	1	IREF1	write only	output gain control register 1
24h	0	1	0	0	1	0	0	IREF2	write only	output gain control register 2
25h	0	1	0	0	1	0	1	IREF3	write only	output gain control register 3
26h	0	1	0	0	1	1	0	IREF4	write only	output gain control register 4
27h	0	1	0	0	1	1	1	IREF5	write only	output gain control register 5
28h	0	1	0	1	0	0	0	IREF6	write only	output gain control register 6
29h	0	1	0	1	0	0	1	IREF7	write only	output gain control register 7
2Ah	0	1	0	1	0	1	0	IREF8	write only	output gain control register 8
2Bh	0	1	0	1	0	1	1	IREF9	write only	output gain control register 9
2Ch	0	1	0	1	1	0	0	IREF10	write only	output gain control register 10
2Dh	0	1	0	1	1	0	1	IREF11	write only	output gain control register 11
2Eh	0	1	0	1	1	1	0	IREF12	write only	output gain control register 12
2Fh	0	1	0	1	1	1	1	IREF13	write only	output gain control register 13
30h	0	1	1	0	0	0	0	IREF14	write only	output gain control register 14
31h	0	1	1	0	0	0	1	IREF15	write only	output gain control register 15
32h to 39h	-	-	-	-	-	-	-	-	write only	not used[1]
3Ah	0	1	1	1	0	1	0	OFFSET	write only	Offset/delay on LEDn outputs
3Bh	0	1	1	1	0	1	1	SUBADR1	write only	I²C-bus subaddress 1
3Ch	0	1	1	1	1	0	0	SUBADR2	write only	I²C-bus subaddress 2
3Dh	0	1	1	1	1	0	1	SUBADR3	write only	I²C-bus subaddress 3
3Eh	0	1	1	1	1	1	0	ALLCALLADR	write only	All Call I²C-bus address
3Fh	0	1	1	1	1	1	1	RESERVED1	write only	reserved[2]
40h	-	-	-	-	-	-	-	-	write only	not used[1]
41h	-	-	-	-	-	-	-	-	write only	not used[1]
42h	1	0	0	0	0	1	0	PWMALL	write only	brightness control for all LEDn
43h	1	0	0	0	0	1	1	IREFALL	write only	output gain control for all registers IREF0 to IREF15
44h to 7Fh	-	-	-	-	-	-	-	-	write only	not used[1]

[1] **Remark:** Writing to registers marked ‘not used’ will be ignored.

[2] **Remark:** Writing to registers marked ‘reserved’ will not change any functionality in the chip.

7.3.1 MODE1 — Mode register 1

Table 5. MODE1 - Mode register 1 (address 00h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	AIF	-	-	not used
6	AI1	W only	0*	Auto-Increment bit 1 = 0. Auto-increment range as defined in Table 3.
			1	Auto-Increment bit 1 = 1. Auto-increment range as defined in Table 3.
5	AI0	W only	0*	Auto-Increment bit 0 = 0. Auto-increment range as defined in Table 3.
			1	Auto-Increment bit 0 = 1. Auto-increment range as defined in Table 3.
4	SLEEP	W only	0*	Normal mode[1].
			1	Low power mode. Oscillator off[2][3].
3	SUB1	W only	0	PCU9955 does not respond to I²C-bus subaddress 1.
			1*	PCU9955 responds to I²C-bus subaddress 1.
2	SUB2	W only	0*	PCU9955 does not respond to I²C-bus subaddress 2.
			1	PCU9955 responds to I²C-bus subaddress 2.
1	SUB3	W only	0*	PCU9955 does not respond to I²C-bus subaddress 3.
			1	PCU9955 responds to I²C-bus subaddress 3.
0	ALLCALL	W only	0	PCU9955 does not respond to LED All Call I²C-bus address.
			1*	PCU9955 responds to LED All Call I²C-bus address.

[1] It takes 500 µs max. for the oscillator to be up and running once SLEEP bit has been set to logic 0. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM or GRPFREQ registers are accessed within the 500 µs window.

[2] No blinking or dimming is possible when the oscillator is off.

[3] The device must be reset if the LED driver output state is set to LDRx=11 after the device is set back to Normal mode.

7.3.2 MODE2 — Mode register 2

Table 6. MODE2 - Mode register 2 (address 01h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	-	-	-	not used
6	-	-	-	not used
5	DMBLNK	W only	0*	group control = dimming.
			1	group control = blinking.
4	-	-	0*	reserved
3	OCH	W only	0*	outputs change on STOP command[1]
			1	outputs change on ACK, this 9th bit is always set to 1 by UFm I²C-bus master

Table 6. MODE2 - Mode register 2 (address 01h) bit description *…continued*

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
2	-	-	1*	reserved
1	-	-	0*	reserved
0	-	-	1*	reserved

[1] Change of the outputs at the STOP command allows synchronizing outputs of more than one PCU9955. Applicable to registers from 02h (LEDOUT0) to 3Ah (OFFSET) only.

7.3.3 LEDOUT0 to LEDOUT3, LED driver output state

Table 7. LEDOUT0 to LEDOUT3 - LED driver output state registers (address 02h to 05h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
02h	LEDOUT0	7:6	LDR3	W only	00*	LED3 output state control
		5:4	LDR2	W only	00*	LED2 output state control
		3:2	LDR1	W only	00*	LED1 output state control
		1:0	LDR0	W only	00*	LED0 output state control
03h	LEDOUT1	7:6	LDR7	W only	00*	LED7 output state control
		5:4	LDR6	W only	00*	LED6 output state control
		3:2	LDR5	W only	00*	LED5 output state control
		1:0	LDR4	W only	00*	LED4 output state control
04h	LEDOUT2	7:6	LDR11	W only	00*	LED11 output state control
		5:4	LDR10	W only	00*	LED10 output state control
		3:2	LDR9	W only	00*	LED9 output state control
		1:0	LDR8	W only	00*	LED8 output state control
05h	LEDOUT3	7:6	LDR15	W only	00*	LED15 output state control
		5:4	LDR14	W only	00*	LED14 output state control
		3:2	LDR13	W only	00*	LED13 output state control
		1:0	LDR12	W only	00*	LED12 output state control

LDRx = 00 — LED driver x is off (default power-up state, x = 0 to 15).

LDRx = 01 — LED driver x is fully on (individual brightness and group dimming/blinking not controlled).

LDRx = 10 — LED driver x individual brightness can be controlled through its PWMx register.

LDRx = 11 — LED driver x individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

Remark: Setting the device in low power mode while being on group dimming/blinking mode may cause the LED output state to be in an unknown state after the device is set back to normal mode. The device must be reset and all register values reprogrammed.

7.3.4 GRPPWM, group duty cycle control

Table 8. GRPPWM - Group brightness control register (address 08h) bit description

*Legend: * default value*

Address	Register	Bit	Symbol	Access	Value	Description
08h	GRPPWM	7:0	GDC[7:0]	W only	1111 1111*	GRPPWM register

When DMBLNK bit (MODE2 register) is programmed with logic 0, a 122 Hz fixed frequency signal is superimposed with the 31.25 kHz individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LEDn outputs to be dimmed with the same value. The value in GRPFREQ is then a 'Don't care'.

General brightness for the 16 outputs is controlled through 256 linear steps from 00h (0 % duty cycle = LEDn output off) to FFh (99.6 % duty cycle = maximum brightness). Applicable to LEDn outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

When DMBLNK bit is programmed with logic 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 15 Hz to 16.8 s) and GRPPWM the duty cycle (ON/OFF ratio in %).

$$duty\ cycle = \frac{GDC[7:0]}{256} \quad (1)$$

7.3.5 GRPFREQ, group frequency

Table 9. GRPFREQ - Group frequency register (address 09h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
09h	GRPFREQ	7:0	GFRQ[7:0]	W only	0000 0000*	GRPFREQ register

GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a 'Don't care' when DMBLNK = 0. Applicable to LEDn outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

Blinking period is controlled through 256 linear steps from 00h (67 ms, frequency 15 Hz) to FFh (16.8 s).

$$global\ blinking\ period = \frac{GFRQ[7:0]+1}{15.26}(s) \quad (2)$$

7.3.6 PWM0 to PWM15, individual brightness control

Table 10. PWM0 to PWM15 - PWM registers 0 to 15 (address 0Ah to 19h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
0Ah	PWM0	7:0	IDC0[7:0]	W only	0000 0000*	PWM0 Individual Duty Cycle
0Bh	PWM1	7:0	IDC1[7:0]	W only	0000 0000*	PWM1 Individual Duty Cycle
0Ch	PWM2	7:0	IDC2[7:0]	W only	0000 0000*	PWM2 Individual Duty Cycle
0Dh	PWM3	7:0	IDC3[7:0]	W only	0000 0000*	PWM3 Individual Duty Cycle
0Eh	PWM4	7:0	IDC4[7:0]	W only	0000 0000*	PWM4 Individual Duty Cycle

Table 10. PWM0 to PWM15 - PWM registers 0 to 15 (address 0Ah to 19h) bit description

…continued

Address	Register	Bit	Symbol	Access	Value	Description
0Fh	PWM5	7:0	IDC5[7:0]	W only	0000 0000*	PWM5 Individual Duty Cycle
10h	PWM6	7:0	IDC6[7:0]	W only	0000 0000*	PWM6 Individual Duty Cycle
11h	PWM7	7:0	IDC7[7:0]	W only	0000 0000*	PWM7 Individual Duty Cycle
12h	PWM8	7:0	IDC8[7:0]	W only	0000 0000*	PWM8 Individual Duty Cycle
13h	PWM9	7:0	IDC9[7:0]	W only	0000 0000*	PWM9 Individual Duty Cycle
14h	PWM10	7:0	IDC10[7:0]	W only	0000 0000*	PWM10 Individual Duty Cycle
15h	PWM11	7:0	IDC11[7:0]	W only	0000 0000*	PWM11 Individual Duty Cycle
16h	PWM12	7:0	IDC12[7:0]	W only	0000 0000*	PWM12 Individual Duty Cycle
17h	PWM13	7:0	IDC13[7:0]	W only	0000 0000*	PWM13 Individual Duty Cycle
18h	PWM14	7:0	IDC14[7:0]	W only	0000 0000*	PWM14 Individual Duty Cycle
19h	PWM15	7:0	IDC15[7:0]	W only	0000 0000*	PWM15 Individual Duty Cycle

A 31.25 kHz fixed frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0 % duty cycle = LEDn output off) to FFh (99.6 % duty cycle = LEDn output at maximum brightness). Applicable to LEDn outputs programmed with LDRx = 10 or 11 (LEDOUT0 to LEDOUT3 registers).

$$duty\ cycle = \frac{IDCx[7:0]}{256} \quad (3)$$

Remark: The first lower end 8 steps of PWM and the last (higher end) steps of PWM will not have effective brightness control of LEDs due to edge rate control of LEDn output pins.

7.3.7 IREF0 to IREF15, LEDn output current value registers

These registers reflect the gain settings for output current for LED0 to LED15.

Table 11. IREF0 to IREF15 - LEDn output gain control registers (address 22h to 31h) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
22h	IREF0	7:0	W only	00h*	LED0 output current setting
23h	IREF1	7:0	W only	00h*	LED1 output current setting
24h	IREF2	7:0	W only	00h*	LED2 output current setting
25h	IREF3	7:0	W only	00h*	LED3 output current setting
26h	IREF4	7:0	W only	00h*	LED4 output current setting
27h	IREF5	7:0	W only	00h*	LED5 output current setting
28h	IREF6	7:0	W only	00h*	LED6 output current setting
29h	IREF7	7:0	W only	00h*	LED7 output current setting
2Ah	IREF8	7:0	W only	00h*	LED8 output current setting
2Bh	IREF9	7:0	W only	00h*	LED9 output current setting
2Ch	IREF10	7:0	W only	00h*	LED10 output current setting
2Dh	IREF11	7:0	W only	00h*	LED11 output current setting
2Eh	IREF12	7:0	W only	00h*	LED12 output current setting

Table 11. IREF0 to IREF15 - LEDn output gain control registers (address 22h to 31h) bit description *…continued*

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
2Fh	IREF13	7:0	W only	00h*	LED13 output current setting
30h	IREF14	7:0	W only	00h*	LED14 output current setting
31h	IREF15	7:0	W only	00h*	LED15 output current setting

7.3.8 OFFSET — LEDn output delay offset register

Table 12. OFFSET - LEDn output delay offset register (address 3Ah) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
3Ah	OFFSET	7:4	-	0000*	not used
		3:0	W only	1000*	LEDn output delay offset factor

The PCU9955 can be programmed to have turn-on delay between LEDn outputs. This helps to reduce peak current for the V_{DD} supply and reduces EMI.

The order in which the LEDn outputs are enabled will always be the same (channel 0 will enable first and channel 15 will enable last).

OFFSET control register bits [3:0] determine the delay used between the turn-on times as follows:

0000 = no delay between outputs (all on, all off at the same time)

0001 = delay of 1 clock cycle (125 ns) between successive outputs

0010 = delay of 2 clock cycles (250 ns) between successive outputs

0011 = delay of 3 clock cycles (375 ns) between successive outputs

:

1111 = delay of 15 clock cycles (1.875 μs) between successive outputs

Example: If the value in the OFFSET register is 1000 the corresponding delay = 8 × 125 ns = 1 μs delay between successive outputs.

channel 0 turns on at time 0 μs

channel 1 turns on at time 1 μs

channel 2 turns on at time 2 μs

channel 3 turns on at time 3 μs

channel 4 turns on at time 4 μs

channel 5 turns on at time 5 μs

channel 6 turns on at time 6 μs

channel 7 turns on at time 7 μs

channel 8 turns on at time 8 μs

channel 9 turns on at time 9 μs

channel 10 turns on at time 10 μs

channel 11 turns on at time 11 μs

channel 12 turns on at time 12 μs

channel 13 turns on at time 13 μs

channel 14 turns on at time 14 μs

channel 15 turns on at time 15 μs

7.3.9 LED bit Sub Call I²C-bus addresses for PCU9955

Table 13. SUBADR1 to SUBADR3 - I²C-bus subaddress registers 1 to 3 (address 3Bh to 3Dh) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
3Bh	SUBADR1	7:1	A1[7:1]	W only	1110 110*	I²C-bus subaddress 1
		0	A1[0]	W only	0*	reserved
3Ch	SUBADR2	7:1	A2[7:1]	W only	1110 110*	I²C-bus subaddress 2
		0	A2[0]	W only	0*	reserved
3Dh	SUBADR3	7:1	A3[7:1]	W only	1110 110*	I²C-bus subaddress 3
		0	A3[0]	W only	0*	reserved

Default power-up values are ECh, ECh, ECh. At power-up, SUBADR1 is enabled while SUBADR2 and SUBADR3 are disabled. The power-up default bit subaddress of ECh indicates that this device is a 16-channel LED driver.

All three subaddresses are programmable. Once subaddresses have been programmed to their right values, SUBx bits need to be set to logic 1 in order to have the device respond to these addresses (MODE1 register) (0). When SUBx is set to logic 1, the corresponding I²C-bus subaddress can be used during an UFm I²C-bus write sequence.

7.3.10 ALLCALLADR, LED All Call I²C-bus address

Table 14. ALLCALLADR - LED All Call I²C-bus address register (address 3Eh) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
3Eh	ALLCALLADR	7:1	AC[7:1]	W only	1110 000*	ALLCALL I²C-bus address register
		0	AC[0]	W only	0*	reserved

The LED All Call I²C-bus address allows all the PCU9955s on the bus to be programmed at the same time (ALLCALL bit in register MODE1 must be equal to logic 1 (power-up default state)). This address is programmable through the I²C-bus and can be used during an I²C-bus write sequence. The register address can also be programmed as a Sub Call.

Only the 7 MSBs representing the All Call I²C-bus address are valid. The LSB in the ALLCALLADR register is a 0.

7.3.11 RESERVED1

This register is reserved.

7.3.12 PWMALL — brightness control for all LEDn outputs

When programmed, the value in this register will be used for PWM duty cycle for all the LEDn (n = 0 to 15) outputs.

Table 15. PWMALL - brightness control for all LEDn outputs register (address 42h) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
42h	PWMALL	7:0	W only	0000 0000*	duty cycle for all LEDn outputs

Remark: Write to any of the PWM0 to PWM15 registers will overwrite the value in corresponding PWMn register.

7.3.13 IREFALL — output current value for all LEDn outputs

The output current setting for all outputs is held in this register. When this register is written to or updated, all LEDn outputs will be set to a current corresponding to this register value.

Writes to IREF0 to IREF15 will overwrite the output current settings.

Table 16. IREFALL - Output gain control for all LEDn outputs (address 43h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7:0	IREFALL	W only	00h*	Current gain setting for all LEDn outputs.

7.3.14 LED driver constant current outputs

In LED display applications, PCU9955 provides nearly no current variations from channel to channel and from device to device. The maximum current skew between channels is less than ±6 % and less than ±8 % between devices.

7.3.14.1 Adjusting output current

The PCU9955 scales up the reference current (I_{ref}) set by the external resistor (R_{ext}) to sink the output current (I_O) at each output port. The maximum output current for the outputs can be set using R_{ext}. In addition, the constant value for current drive at each of the outputs is independently programmable using command registers IREF0 to IREF15. Alternatively, programming the IREFALL register allows all outputs to be set at one current value determined by the value in IREFALL register.

Equation 4 and Equation 5 can be used to calculate the minimum and maximum constant current values that can be programmed for the outputs for a chosen R_{ext}.

$$I_O\_LED\_LSB = \frac{900\ mV}{R_{ext}} \times \frac{1}{4} \tag{4}$$

$$I_O\_LED\_MAX = (255 \times I_O\_LED\_LSB) = \left(\frac{900\ mV}{R_{ext}} \times \frac{255}{4}\right) \tag{5}$$

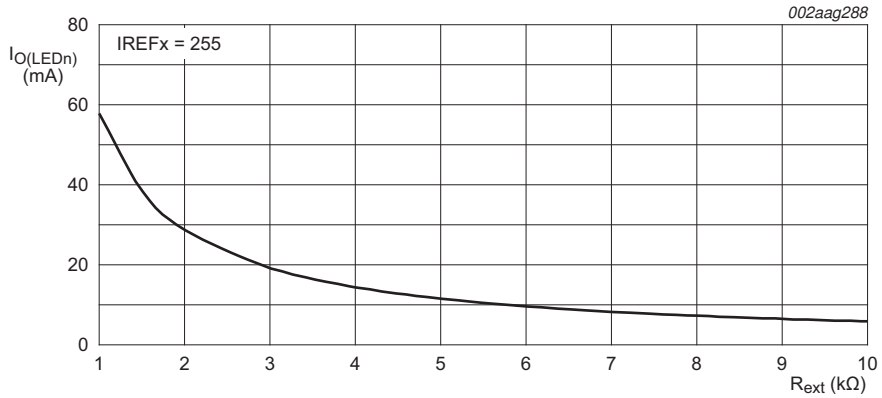
For a given IREFx (x = 0 to 15) setting, $I_O\_LED = IREFx \times \frac{900\ mV}{R_{ext}} \times \frac{1}{4}$.

Example 1: If R_{ext} = 1 kΩ, I_O_LED_LSB = 225 μA, I_O_LED_MAX = 57.375 mA.

So each channel can be programmed with its individual IREFx in 256 steps and in 225 μA increments to a maximum output current of 57.375 mA independently.

Example 2: If R_{ext} = 2 kΩ, I_O_LED_LSB = 112.5 μA, I_O_LED_MAX = 26.687 mA.

So each channel can be programmed with its individual IREFx in 256 steps and in 112.5 μA increments to a maximum output channel of 28.687 mA independently.

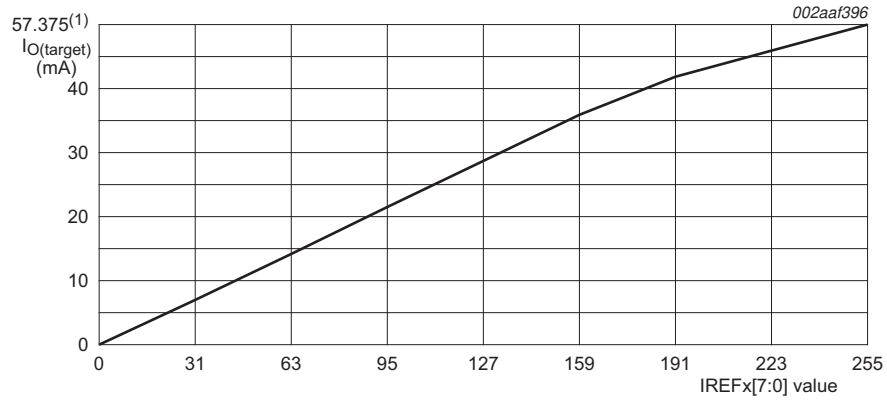


$I_{O(LEDn)}$ (mA) = IREFx × (0.9 / 4) / R_{ext} (kΩ)

maximum $I_{O(LEDn)}$ (mA) = 255 × (0.9 / 4) / R_{ext} (kΩ)

Remark: Default IREFx at power-up = 0.

Fig 5. $I_{O(target)}$ versus R_{ext}



(1) Assuming R_{ext} = 1 kΩ.

Fig 6. $I_{O(target)}$ versus IREFx value

7.3.15 Overtemperature protection

If the PCU9955 chip temperature exceeds its limit ($T_{th(otp)}$, see Table 19), all output channels will be disabled until the temperature drops below its limit minus a small hysteresis (T_{hys}, see Table 19). Once the die temperature reduces below the $T_{th(otp)} - T_{hys}$, the chip will return to the same condition it was prior to the overtemperature event.

7.4 Power-on reset

When power is applied to V_{DD}, an internal power-on reset holds the PCU9955 in a reset condition until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCU9955 registers and I²C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. Thereafter, V_{DD} must be pulled lower than 1 V and stay LOW for longer than 20 μs. The device will reset itself, and allow 2 ms for the device to fully wake up.

7.5 Hardware reset recovery

When a reset of PCU9955 is activated using an active LOW input on the $\overline{\text{RESET}}$ pin, a reset pulse width of 2.5 μs minimum is required. The maximum wait time after $\overline{\text{RESET}}$ pin is released is 1.5 ms.

7.6 Software reset

The Software Reset Call (SWRST Call) allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command.

The maximum wait time after software reset is 1 ms.

The SWRST Call function is defined as the following:

1. A START command is sent by the I²C-bus master.
2. The reserved General Call address ‘0000 000’ with the $\overline{\text{W}}$ bit set to ‘0’ (write) is sent by the I²C-bus master.
3. Since PCU9955 is a UFm I²C-bus device, no acknowledge is returned to the I²C-bus master.
4. Once the General Call address has been sent, the master sends 1 byte with 1 specific value (SWRST data byte 1): Byte 1 = 06h.

   If more than 1 byte of data is sent, they will be ignored by the PCU9955.
5. Once the correct byte (SWRST data byte 1) has been sent, the master sends a STOP command to end the SWRST function: the PCU9955 then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time (t_{BUF}).

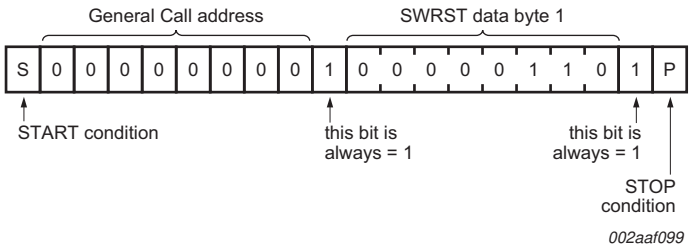


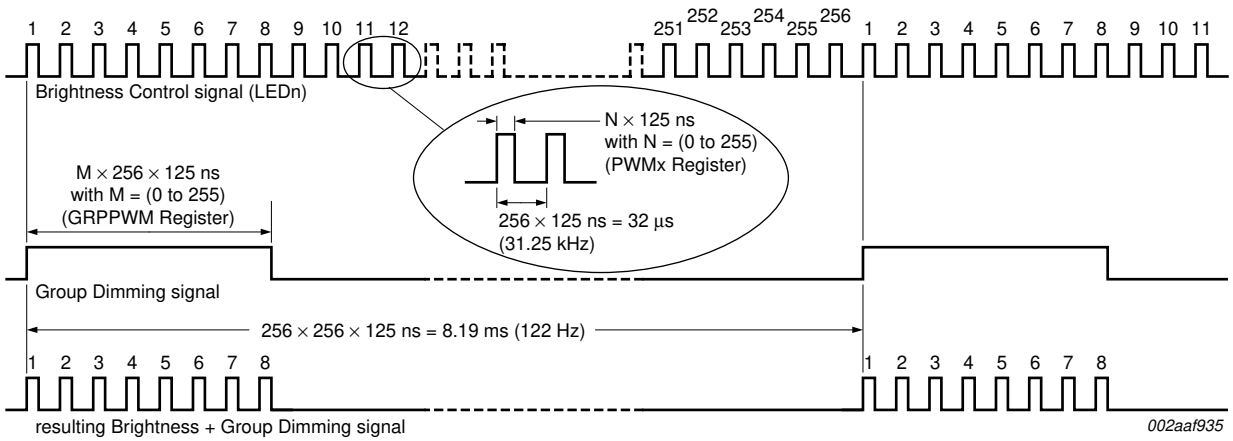
Fig 7. SWRST Call

7.7 Individual brightness control with group dimming/blinking

A 31.25 kHz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control individually the brightness for each LED.

On top of this signal, one of the following signals can be superimposed (this signal can be applied to the 16 LEDn output control registers LEDOUT0 to LEDOUT3):

- A lower 122 Hz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to provide a global brightness control.
- A programmable frequency signal from 15 Hz to every 16.8 seconds (8 bits, 256 steps) with programmable duty cycle (8 bits, 256 steps) is used to provide a global blinking control.



Minimum pulse width for LEDn Brightness Control is 125 ns.

Minimum pulse width for Group Dimming is 32 µs.

When M = 1 (GRPPWM register value), the resulting LEDn Brightness Control + Group Dimming signal will have 1 pulse of the LED Brightness Control signal (pulse width = N × 125 ns, with 'N' defined in PWMx register).

This resulting Brightness + Group Dimming signal above shows a resulting Control signal with M = 8.

Fig 8. Brightness + Group Dimming signals

8. Characteristics of the PCU9955 Ultra Fast-mode I²C-bus

The PCU9955 LED controller uses the new Ultra Fast-mode (UFm) I²C-bus to communicate with the UFm I²C-bus capable host controller. Like the Standard mode and Fast-mode Plus (Fm+) I²C-bus, it uses two lines for communication. They are a serial data line (USDA) and a serial clock line (USCL). The UFm is a unidirectional bus that is capable of higher frequency (up to 5 MHz). The UFm I²C-bus slave devices operate in receive-only mode. That is, only I²C writes to PCU9955 are supported.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the USDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 9).

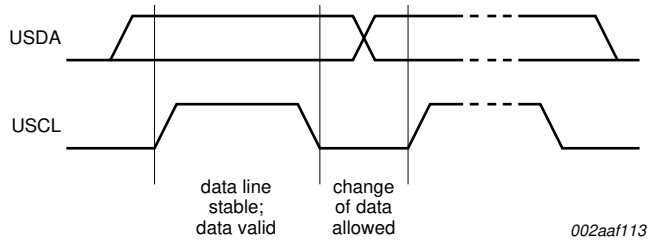


Fig 9. Bit transfer

8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 10).

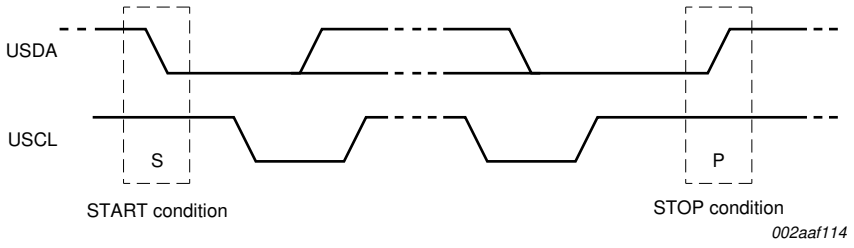


Fig 10. Definition of START and STOP conditions

8.2 System configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 11).

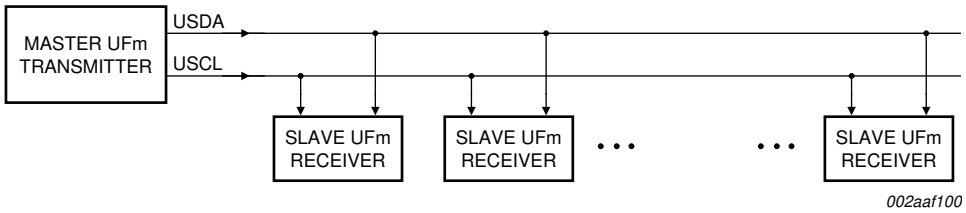


Fig 11. System configuration

8.3 Data transfer

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one bit that is always set to 1. The master generates an extra related clock pulse.

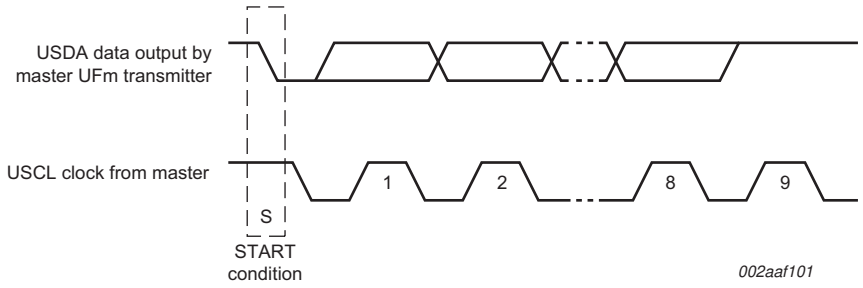
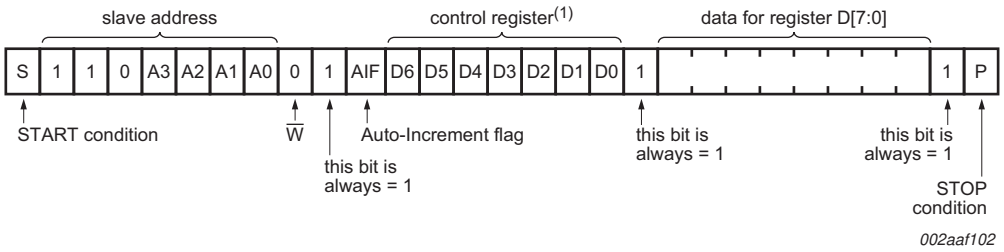


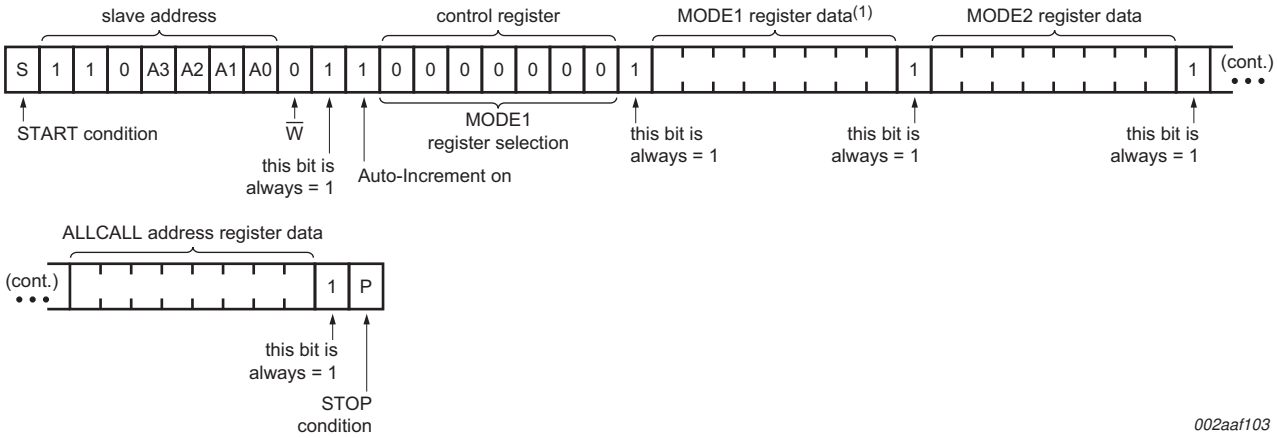
Fig 12. Data transfer

9. Bus transactions



(1) See Table 4 for register definition.

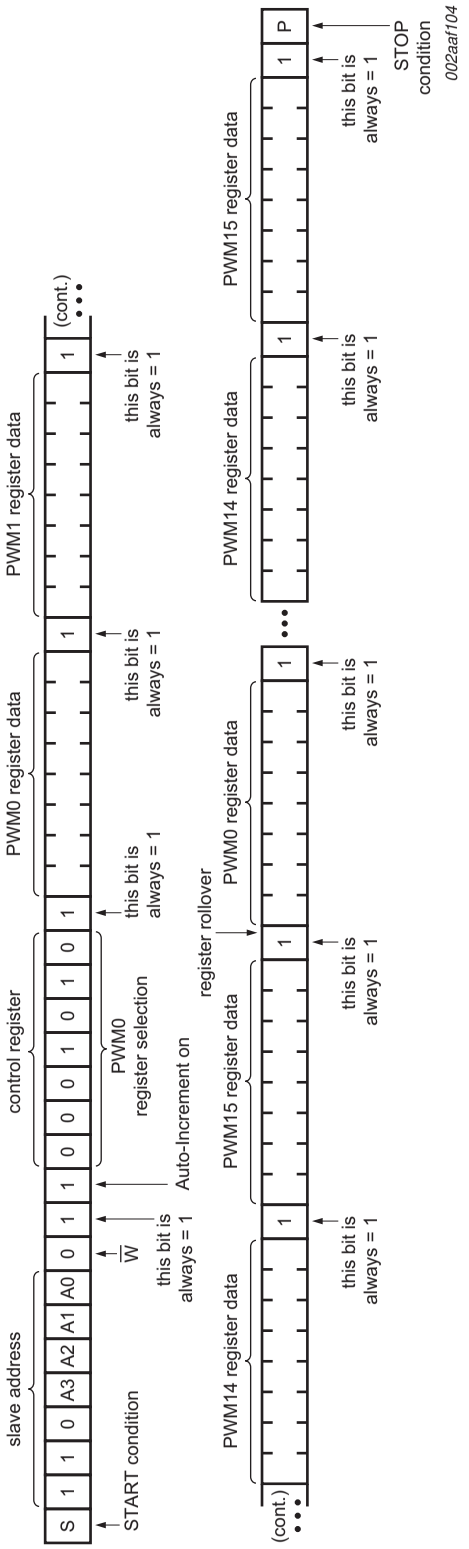
Fig 13. Write to a specific register



(1) AI1, AI0 = 00. See Table 3 for Auto-Increment options.

Remark: Care should be taken to load the appropriate value here in the AI1 and AI0 bits of the MODE1 register for programming the part with the required Auto-Increment options.

Fig 14. Write to all registers using the Auto-Increment feature



This example assumes that AIF + AI[1:0] = 101b.

Fig 15. Multiple writes to Individual Brightness registers only using the Auto-Increment feature