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Middle Power Class-D Speaker Amplifiers

Class-D Speaker Amplifier for Digital Input



BD5451EFV

No.11075EAT17

●Description

BD5451EFV is a Class D Speaker Amplifier designed for Flat-panel TVs in particular for space-saving and low-power consumption, delivers an output power of 15W+15W. This IC employs state-of-the-art Bipolar, CMOS, and DMOS (BCD) process technology that eliminates turn-on resistance in the output power stage and internal loss due to line resistances up to an ultimate level. With this technology, the IC can achieve high efficiency of 90% (15W+15W output with 8Ω load). In addition, the IC is packaged in a compact reverse heat radiation type power package to achieve low power consumption and low heat generation and eliminates necessity of external heat-sink up to a total output power of 30W. This product satisfies both needs for drastic downsizing, low-profile structures and many function, high quality playback of sound system.

●Features

- 1) This IC has one system of digital audio interface.
(I²S format, SDATA: 16 / 20 / 24bit, LRCLK: 32kHz / 44.1kHz / 48kHz, BCLK: 64fs(fixed), MCLK: 256fs(fixed))
- 2) Low supply current at RESET mode.
- 3) The decrease in sound quality because of the change of the power supply voltage is prevented with the feedback circuitry of the output. In addition, a low noise and low distortion are achieved.
Eliminate large electrolytic-capacitors for high performance of Power Supply Rejection.
- 4) S/N of the system can be optimized by adjusting the gain setting among 2 steps. (20dB / 26dB)
- 5) Available for Monaural mode.
- 6) Within the wide range of the power supply voltage, it is possible to operate in a single power supply. (10~18V)
- 7) It contributes to miniaturizing, making to the thin type, and the power saving of the system by high efficiency and low heat.
- 8) Eliminates pop noise generated when the power supply goes on/off, or when the power supply is suddenly shut off.
High quality muting performance is realized by using the soft-muting technology.
- 9) This IC is a highly reliable design to which it has various protection functions.
(High temperature protection, under voltage protection, Output short protection, Output DC voltage protection and Clock stop protection, (MCLK, BCLK, LRCLK))
- 10) Small package (HTSSOP-B28 package) contributes to reduction of PCB area.

●Applications

Flat Panel TVs (LCD, Plasma), Home Audio, Desktop PC, Amusement equipments, Electronic Music equipments, etc.

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Ratings	Unit	Parameter
Supply voltage	V _{CC}	22	V	Pin 14, 15, 16, 27, 28 ※1 ※2
Power dissipation	P _d	3.3	W	※3
		4.7	W	※4
Input voltage	V _{IN}	-0.3 ~ 4.5	V	Pin 1 ~ 6, 13 ※1
Terminal voltage 1	V _{PIN1}	-0.3 ~ 7.0	V	Pin 8, 11, 12 ※1
Terminal voltage 2	V _{PIN2}	-0.3 ~ 4.5	V	Pin 9 ※1
Terminal voltage 3	V _{PIN3}	22	V	Pin 17, 18, 20 ~ 23, 25, 26 ※1
Open-drain terminal voltage	V _{ERR}	-0.3 ~ 22	V	Pin 10 ※1
Operating temperature range	T _{opr}	-25 ~ +85	°C	
Storage temperature range	T _{stg}	-55 ~ +150	°C	
Maximum junction temperature	T _{jmax}	+150	°C	

※1 The voltage that can be applied reference to GND (Pin 7, 19, 24).

※2 Do not, however exceed Pd and T_{jmax}=150°C.

※3 70mm×70mm×1.6mm, FR4, 2-layer glass epoxy board (Copper on bottom layer : 70mm×70mm)
Derating in done at 26.4mW/°C for operating above Ta=25°C. There are thermal via on the board.

※4 70mm×70mm×1.6mm, FR4, 4-layer glass epoxy board (Copper on bottom layer : 70mm×70mm)
Derating in done at 37.6mW/°C for operating above Ta=25°C. There are thermal via on the board.

●Operating conditions (Ta=25°C)

Parameter	Symbol	Ratings	Unit	Parameter
Supply voltage	V _{CC}	10 ~ 18	V	Pin 14, 15, 16, 27, 28 ※1 ※2
Minimum load impedance	R _L	3.6	Ω	V _{CC} ≤ 18V ※5
		3.2		V _{CC} ≤ 16V ※5

※5 Do not, however exceed Pd.

※ No radiation-proof design.

●Electrical characteristics

(Unless otherwise specified Ta=25°C, Vcc=12V, f=1kHz, RL=8Ω, RSTX=3.3V, MUTEX=3.3V, Gain=20dB, fs=48kHz
Output LC filter: L=10μH, C=0.1μF)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Total circuit						
Circuit current (Reset mode)	I _{CC1}	-	0.1	0.2	mA	Pin 14, 15, 16, 27, 28, No load RSTX=0V, MUTEX=0V
Circuit current (Mute mode)	I _{CC2}	-	15	25	mA	Pin 14, 15, 16, 27, 28, No load RSTX=3.3V, MUTEX=0V
Circuit current (Sampling mode)	I _{CC3}	-	50	80	mA	Pin 14, 15, 16, 27, 28, No load RSTX=3.3V, MUTEX=3.3V
Open-drain terminal Low level voltage	V _{ERR}	-	-	0.8	V	Pin 10, I _O =0.5mA
Regulator output voltage 1	V _{REG_G}	4.7	5.0	5.3	V	Pin 11
Regulator output voltage 2	V _{REG_3}	3.0	3.3	3.6	V	Pin 9
High level input voltage	V _{IH}	2.0	-	3.3	V	Pin 1 ~ 6, 13
Low level input voltage	V _{IL}	0	-	0.9	V	Pin 1 ~ 6, 13
Input current (Input pull-down terminal)	I _{IH}	50	66	95	μA	Pin 1 ~ 6, 13, V _{IN} = 3.3V
Speaker Output						
Maximum output power 1	P _{O1}	-	10	-	W	THD+n=10% GAIN=20dB ※6
Maximum output power 2	P _{O2}	-	15	-	W	VCC=15V, THD+n=10% GAIN =26dB ※6
Voltage gain	G _{V20}	19	20	21	dB	P _O =1W, Gain=20dB ※6
	G _{V26}	25	26	27	dB	P _O =1W, Gain=26dB ※6
Total harmonic distortion	THD	-	0.07	-	%	P _O =1W, BW=20~20kHz ※6
Crosstalk	CT	66	80	-	dB	P _O =1W, BW=IHF-A ※6
PSRR	PSRR	-	70	-	dB	V _{ripple} =1V _{rms} , f= 1kHz ※6
Output noise voltage (Sampling mode)	V _{NO}	-	100	200	μV _{rms}	-∞dBFS, BW=IHF-A ※6
PWM sampling frequency	f _{PWM1}	-	256	-	kHz	fs=32kHz ※6
	f _{PWM2}	-	352.8	-	kHz	fs=44.1kHz ※6
	f _{PWM3}	-	384	-	kHz	fs=48kHz ※6

※6 These items show the typical performance of device and depend on board layout, parts, and power supply.
The standard value is in mounting device and parts on surface of ROHM's board directly.

●Electrical characteristic curves (VCC=12V, Ta=25°C, RL=8Ω, Gain=26dB, fin=1kHz, fs=48kHz)
 Measured by ROHM designed 4 layer board.

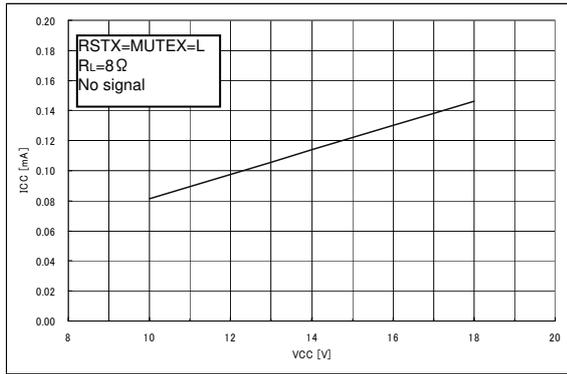


Fig.1
 Current consumption - Power supply voltage

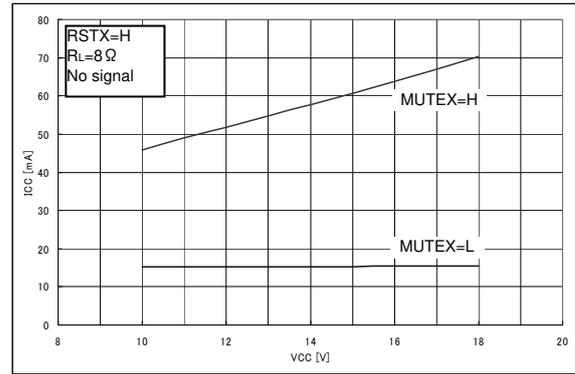


Fig.2
 Current consumption - Power supply voltage

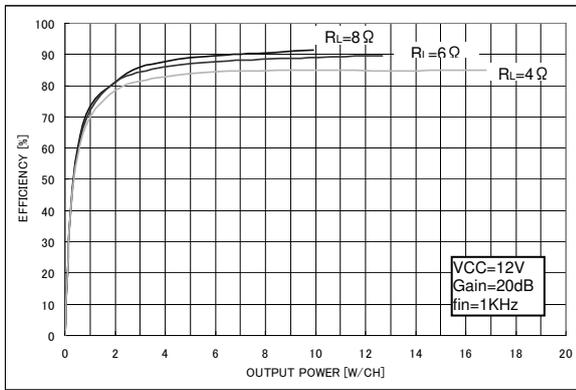


Fig.3
 Efficiency - Output power

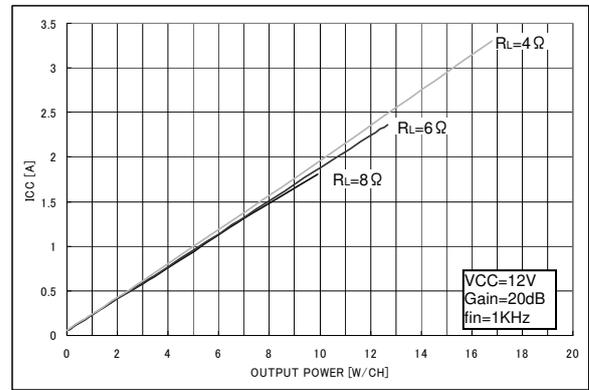


Fig.4
 Current consumption - Output power

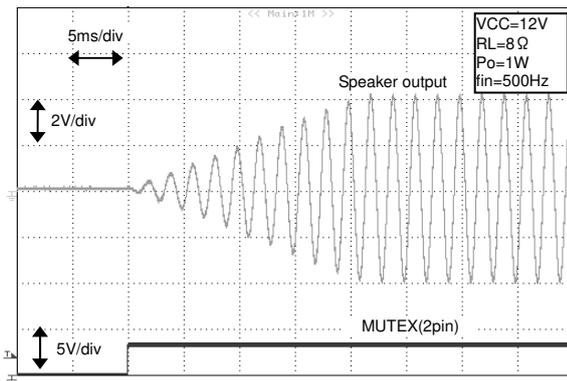


Fig.5
 Wave form when releasing soft-mute

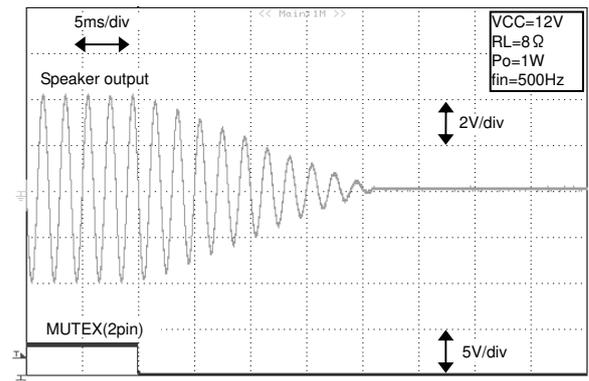


Fig.6
 Wave form when activating soft-mute

●Electrical characteristics (VCC=12V, Gain=26dB, fin=1kHz, fs=48kHz)
 Measured by ROHM designed 4 layer board.

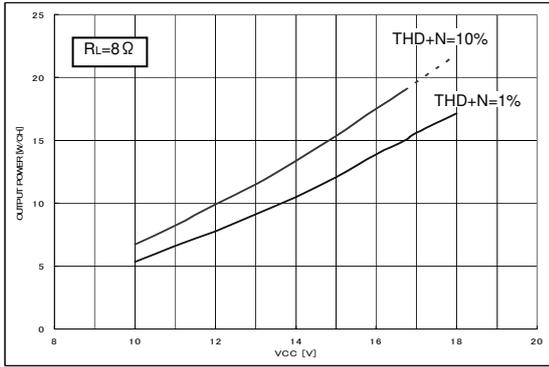


Fig.7
 Output power – Power supply voltage

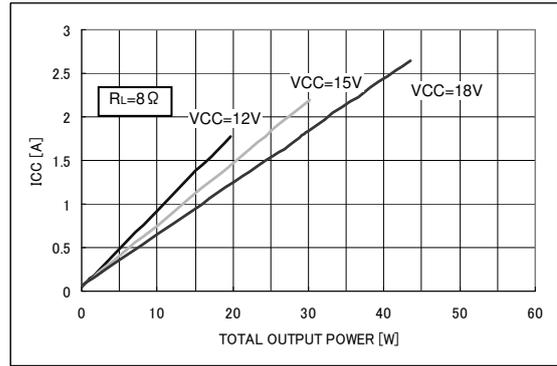


Fig.8
 Current consumption - Output power

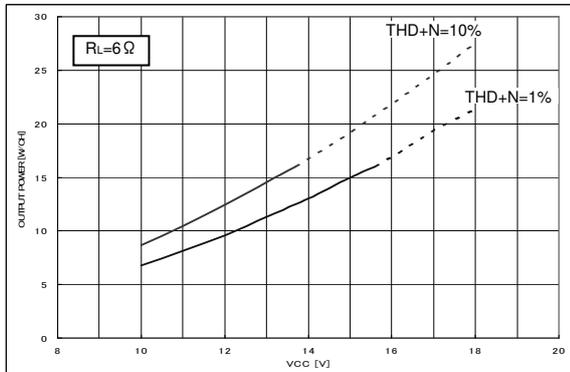


Fig.9
 Output power – Power supply voltage

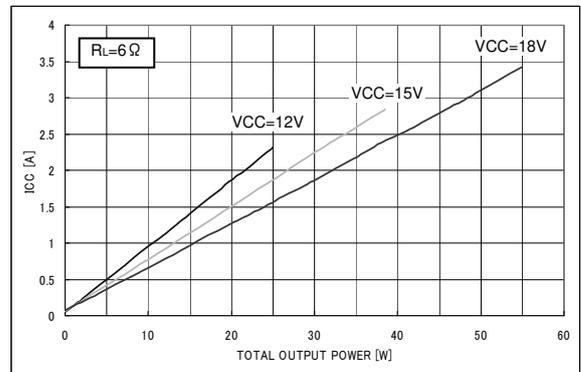


Fig.10
 Current consumption - Output power

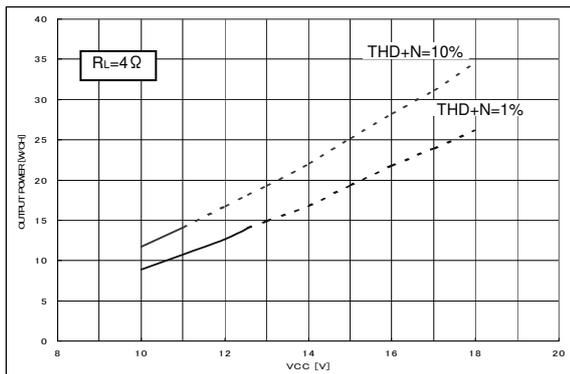


Fig.11
 Output power – Power supply voltage

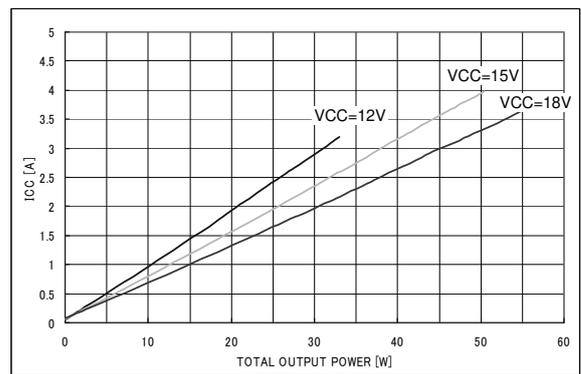


Fig.12
 Current consumption - Output power

※Dotted line means internal dissipation is over package power.

●Electrical characteristic curves(VCC=12V, Ta=25°C, RL=8Ω, Gain=20dB, fin=1kHz, fs=48kHz)

Measured by ROHM designed 4layer board.

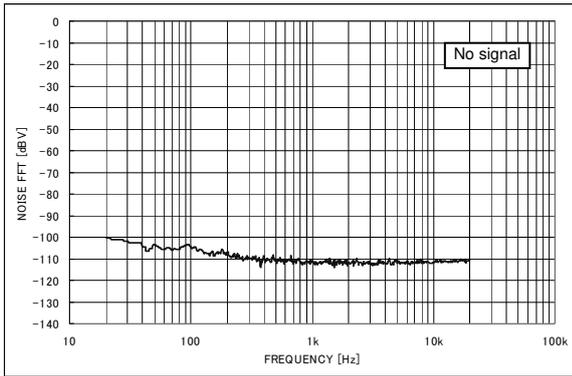


Fig.13
FFT of output noise voltage

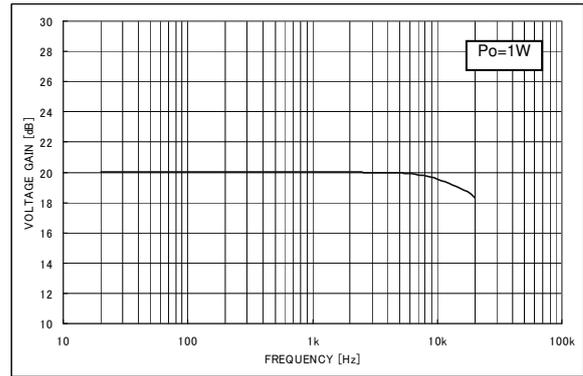


Fig.14
Voltage gain - Frequency

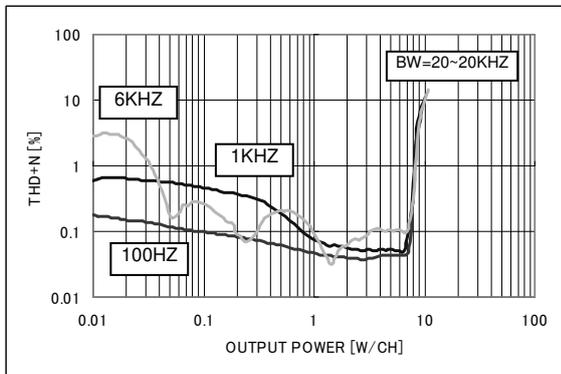


Fig.15
THD+N - Output power

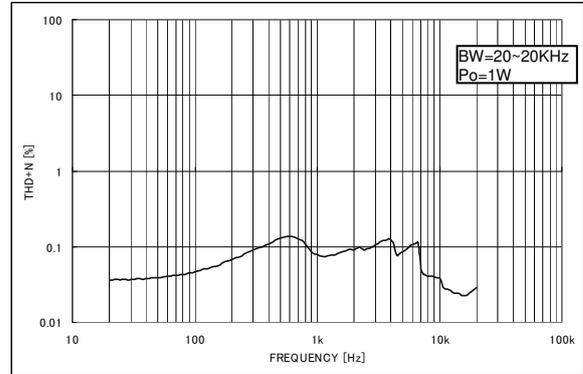


Fig.16
THD+N - Frequency

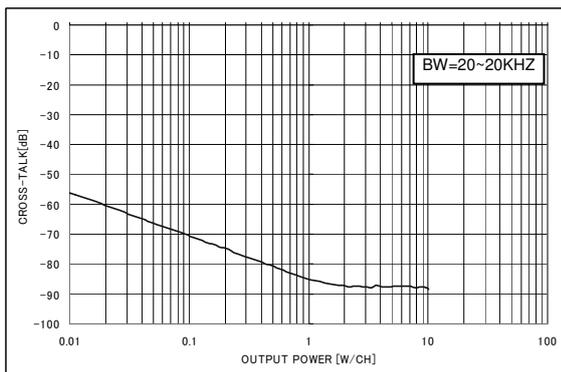


Fig.17
Crosstalk - Output power

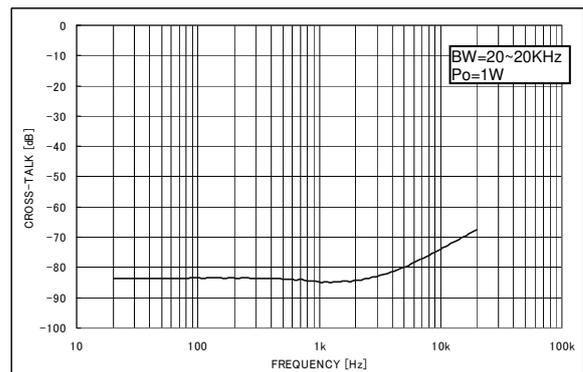


Fig.18
Crosstalk - Frequency

●Electrical characteristic curves(VCC=12V, Ta=25°C, RL=6Ω, Gain=20dB, fin=1kHz, fs=48kHz)

Measured by ROHM designed 4layer board

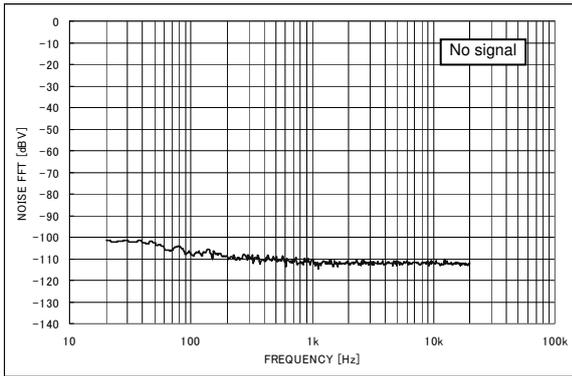


Fig.19
FFT of output noise voltage

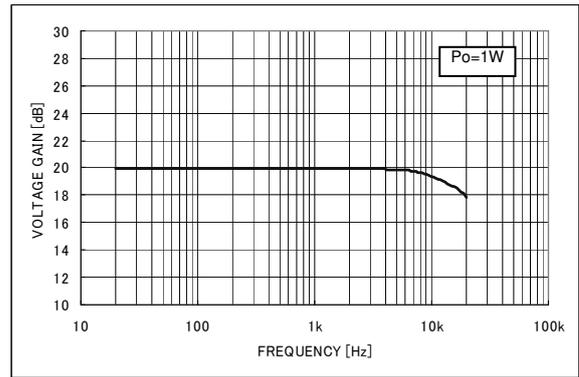


Fig.20
Voltage gain - Frequency

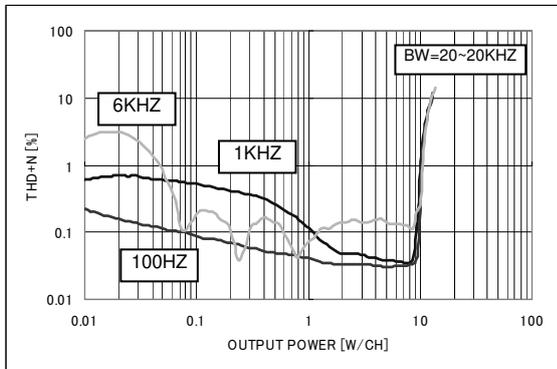


Fig.21
THD+N - Output power

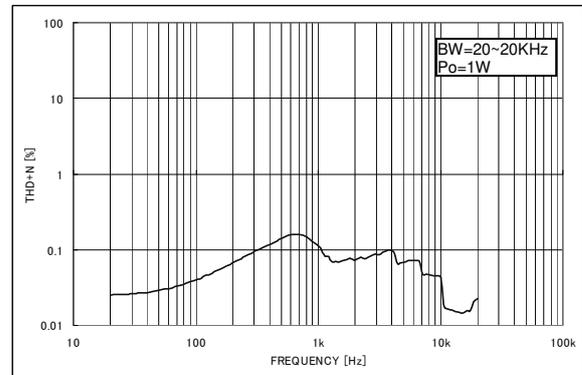


Fig.22
THD+N - Frequency

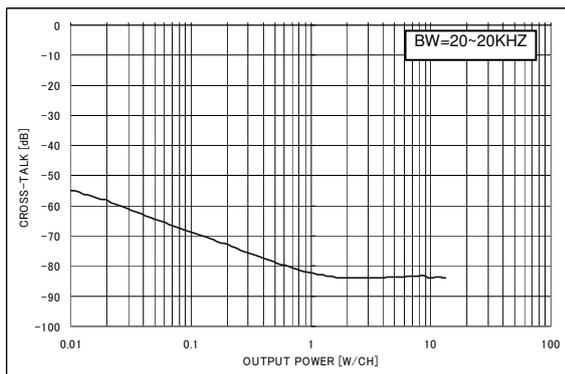


Fig.23
Crosstalk - Output power

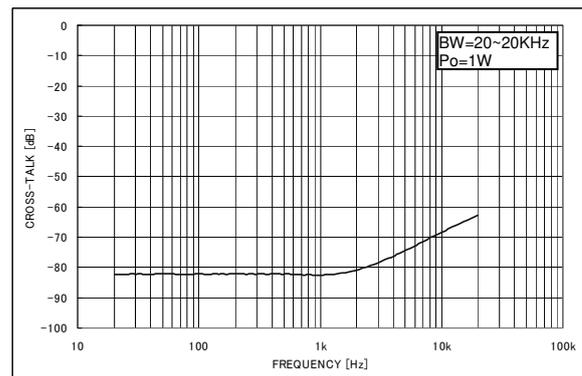


Fig.24
Crosstalk - Frequency

●Electrical characteristic curves(VCC=12V, Ta=25°C, RL=4Ω, Gain=20dB, fin=1kHz, fs=48kHz)

Measured by ROHM designed 4layer board

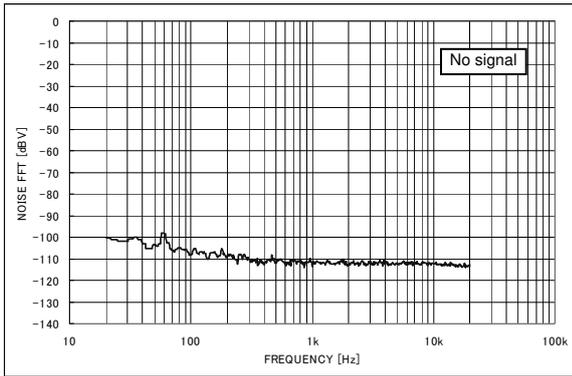


Fig.25
FFT of output noise voltage

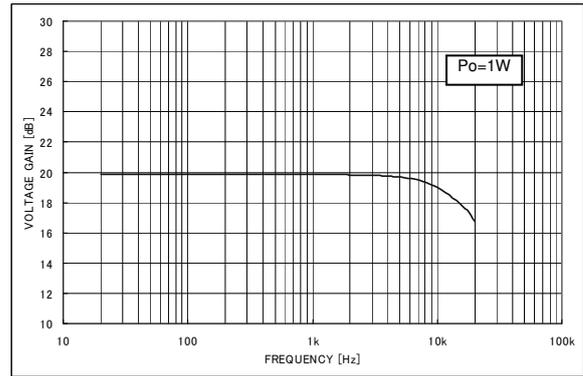


Fig.26
Voltage gain - Frequency

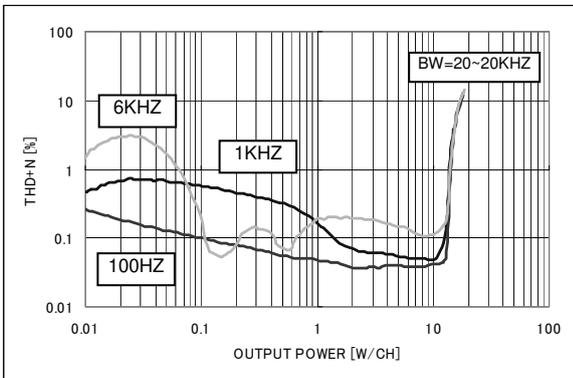


Fig.27
THD+N - Output power

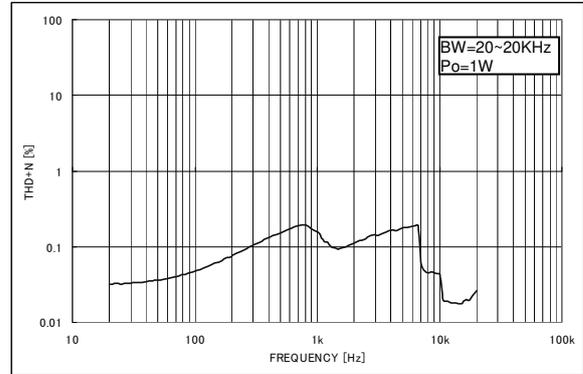


Fig.28
THD+N - Frequency

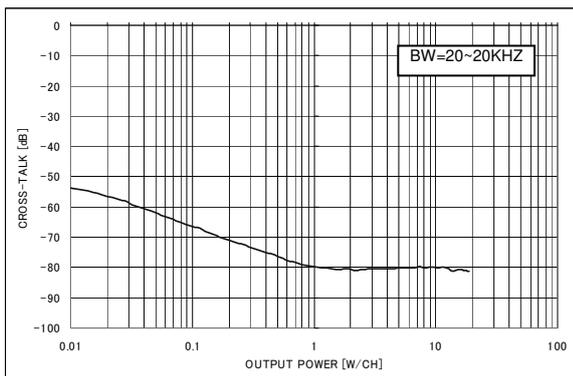


Fig.29
Crosstalk - Output power

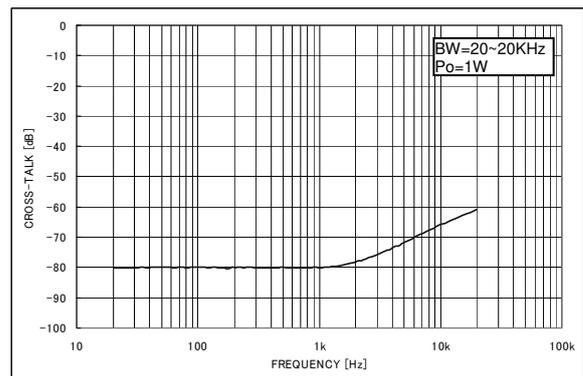
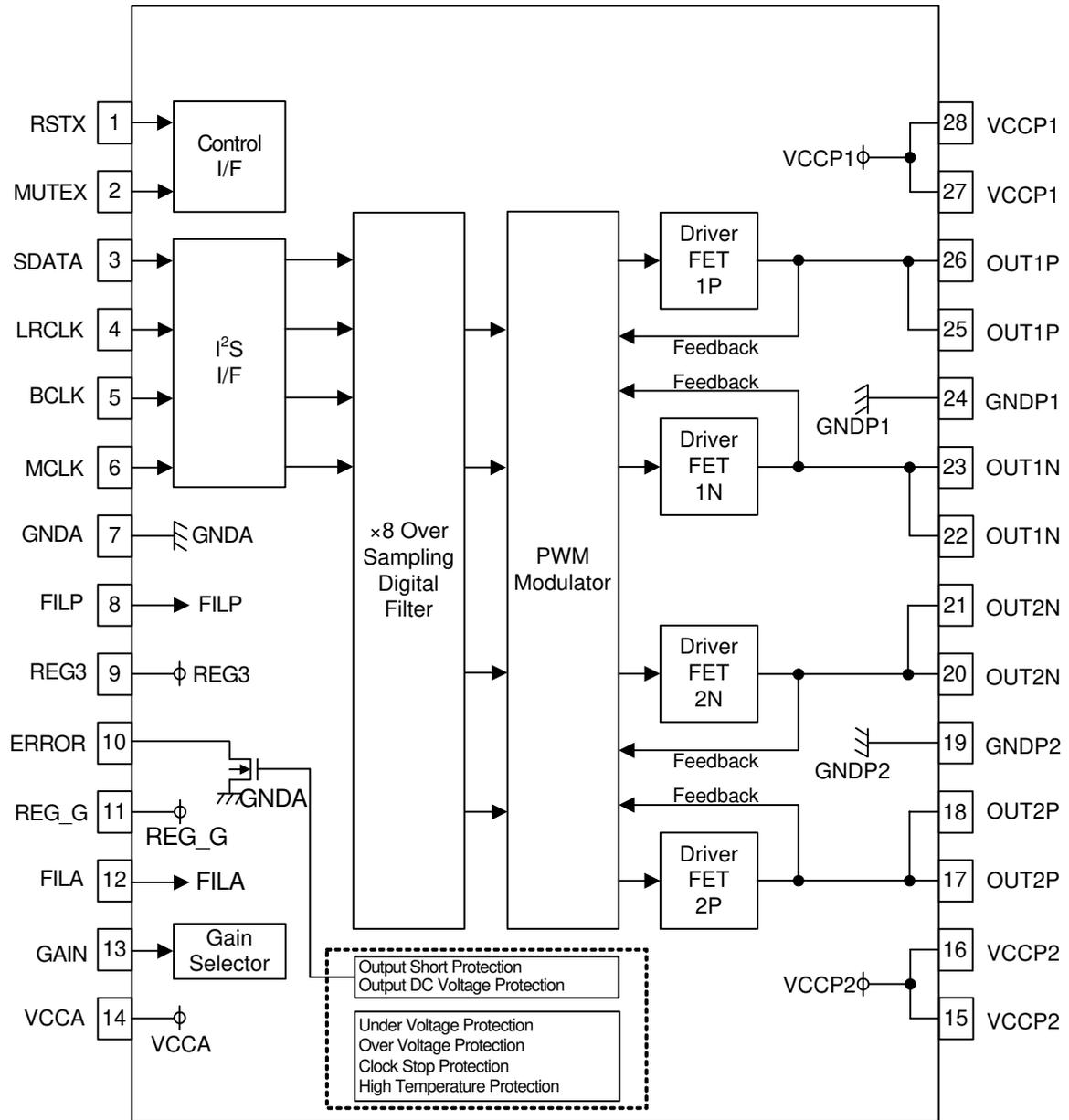


Fig.30
Crosstalk - Frequency

● Pin configuration and Block diagram



●Pin function explanation (Provided pin voltages are typ. Values)

Pin No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
1	RSTX	0V	Reset pin for Digital circuit H: Reset OFF L: Reset ON	
2	MUTEX	0V	Speaker output mute control pin H: Mute OFF L: Mute ON	
3	SDATA		Digital audio signal input pin	
4	LRCLK			
5	BCLK			
6	MCLK			
12	GAIN		Gain setting terminal L: 20dB H: 26dB	
7	GNDA	0V	GND pin for Analog signal	-
8	FILP	1.75V~2.55V	Bias pin for PWM signal Please connect the capacitor.	
9	REG3	3.3V	Internal power supply pin for Digital circuit Please connect the capacitor.	
10	ERROR	3.3V	Error flag pin Please connect pull-up resistor. H: While Normal L: While Error	
11	REG_G	5.2V	Internal power supply pin for Gate driver Please connect the capacitor.	

Pin No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
12	FILA	2.5V	Bias pin for PWM signal. Please connect the capacitor.	
14	VCCA	Vcc	Power supply pin for Analog signal	—
15,16	VCCP2	Vcc	Power supply pin for ch2 PWM signal Please connect the capacitor.	
17,18	OUT2P	Vcc~0V	Output pin of ch2 positive PWM Please connect to Output LPF.	
19	GNDP2	0V	GND pin for ch2 PWM signal	
20,21	OUT2N	Vcc~0V	Output pin of ch2 negative PWM Please connect to Output LPF.	
22,23	OUT1N	Vcc~0V	Output pin of ch1 negative PWM Please connect to Output LPF.	
24	GNDP1	0V	GND pin for ch1 PWM signal	
25,26	OUT1P	Vcc~0V	Output pin of ch1 positive PWM Please connect to Output LPF.	
27,28	VCCP1	—	Power supply pin for ch1 PWM signal Please connect the capacitor.	

● Terminal setting

(1) Gain pin function

GAIN (13pin)	Speaker output gain
L	20dB
H	26dB

(2) RSTX pin, MUTEX pin function

RSTX (1pin)	MUTEX (2pin)	Normalcy		Error detecting	
		PWM output (OUT1P, 1N, 2P, 2N)	ERROR Output	PWM output (OUT1P, 1N, 2P, 2N)	ERROR Output
L	L or H	HiZ_L (Reset mode)	H	HiZ_L (Reset mode)	H
H	L	HiZ_L (MUTE_ON)	H	HiZ_L (MUTE_ON)	L
H	H	Normal operation (MUTE_OFF)	H	HiZ_L (MUTE_ON)	L

※RSTX(1pin)terminal, MUTEX(2pin)terminal are internally pulled down by 50 kΩ (Typ.)

※With RSTX=L data of every register within IC (I²S / I/F part, ×8 over sampling digital filter part, latch circuit when detecting ERROR) becomes unnecessary.

● Input digital audio signal sampling frequency (fs) explanation

PWM sampling frequency, Soft-start, Soft-mute time, and the detection time of the DC voltage protection in the speaker depends on sampling frequency (fs) of the digital audio input.

Sampling frequency of the digital audio input (fs)	PWM sampling frequency (fpwm)	Soft-start / Soft-mute time	DC voltage protection in the speaker detection time
32kHz	256kHz	32msec.	64msec.
44.1kHz	352.8kHz	23msec.	46msec.
48kHz	384kHz	21.5msec.	43msec.

● For voltage gain (Gain setting)

BD5451EFV prescribe voltage gain at speaker output (BTL output) under the definition 0dBV (1Vrms) as full scale input of the digital audio input signal. For example, digital audio input signal = -20dBFS (0.1Vrms), Gain setting = 20dB, Load resistance $R_L = 8\ \Omega$ will give speaker output (BTL output) amplitude as $V_o=1Vrms$. (Output power $P_o = V_o^2/R = 0.125W$)

●Format of digital audio input

- MCLK: It is System Clock input signal.
It will input LRCLK, BCLK, SDATA that synchronizes with this clock that are 256 times of sampling frequency (256fs).
- LRCLK: It is L/R clock input signal.
It corresponds to 32kHz / 44.1kHz / 48kHz with those clock (fs) that are same to the sampling frequency (fs) .
The data of a left channel and a right channel for one sample is input to this section.
- BCLK: It is Bit Clock input signal.
It is used for the latch of data in every one bit by sampling frequency's 64 times sampling frequency (64fs).
- SDATA: It is Data input signal.
It is amplitude data. The data length is different according to the resolution of the input digital audio data.
It corresponds to 16/ 20/ 24 bit.

●I²S data format

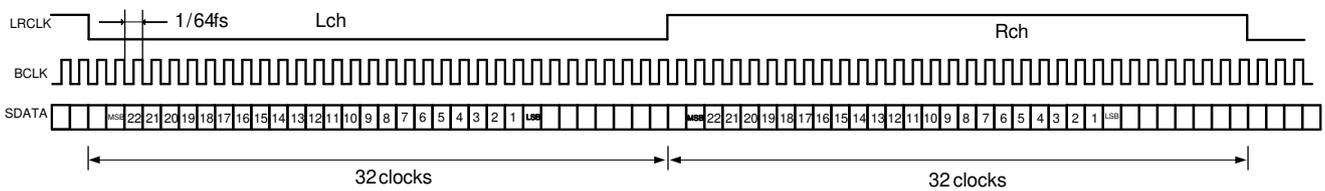


Fig.31 I²S Data Format 64fs, 24 bit Data

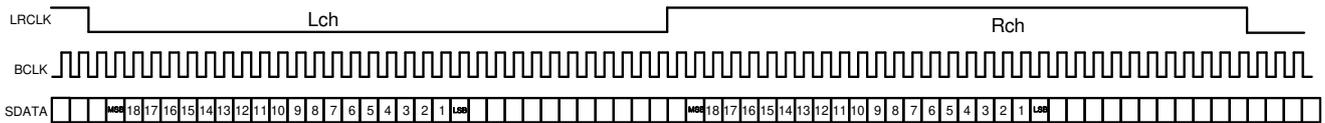


Fig.32 I²S Data Format 64fs, 20 bit Data

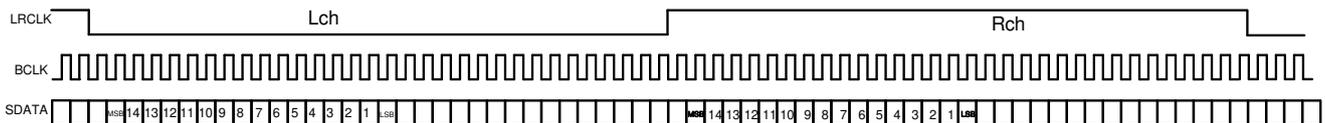


Fig.33 I²S Data Format 64fs, 16 bit Data

The Low section of LRCLK becomes Lch, the High section of LRCLK becomes Rch.
After changing LRCLK, second bit becomes MSB.

●Audio Interface format and timing

Recommended timing and operating conditions (MCLK, BCLK, LRCLK, SDATA)

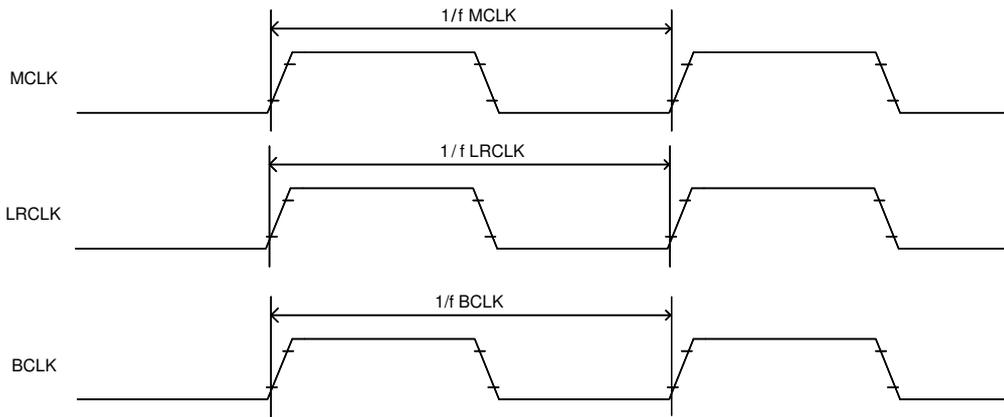


Fig.34 Clock timing

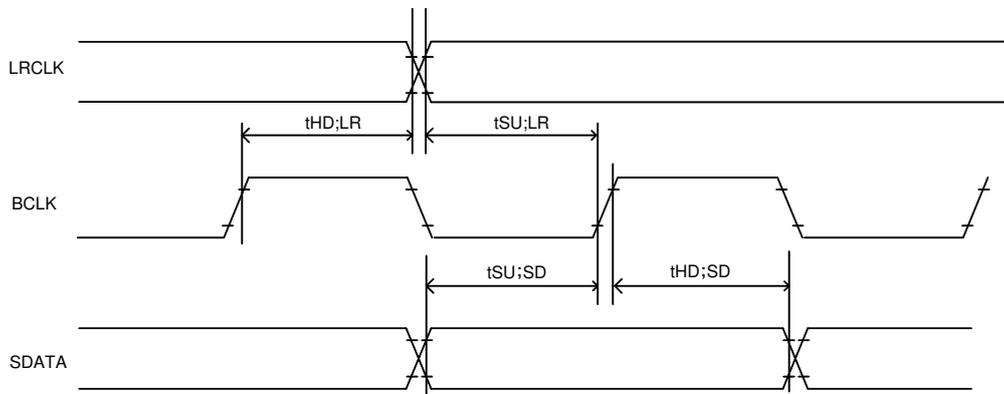


Fig.35 Audio Interface timing (1)

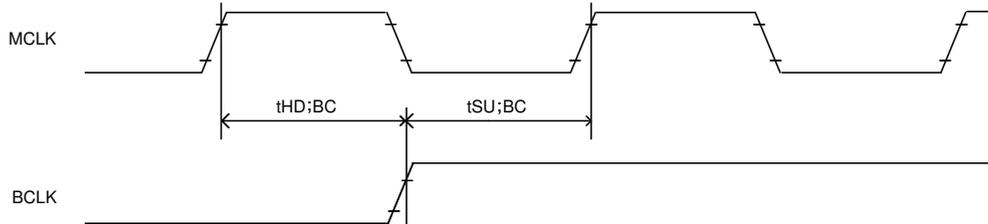


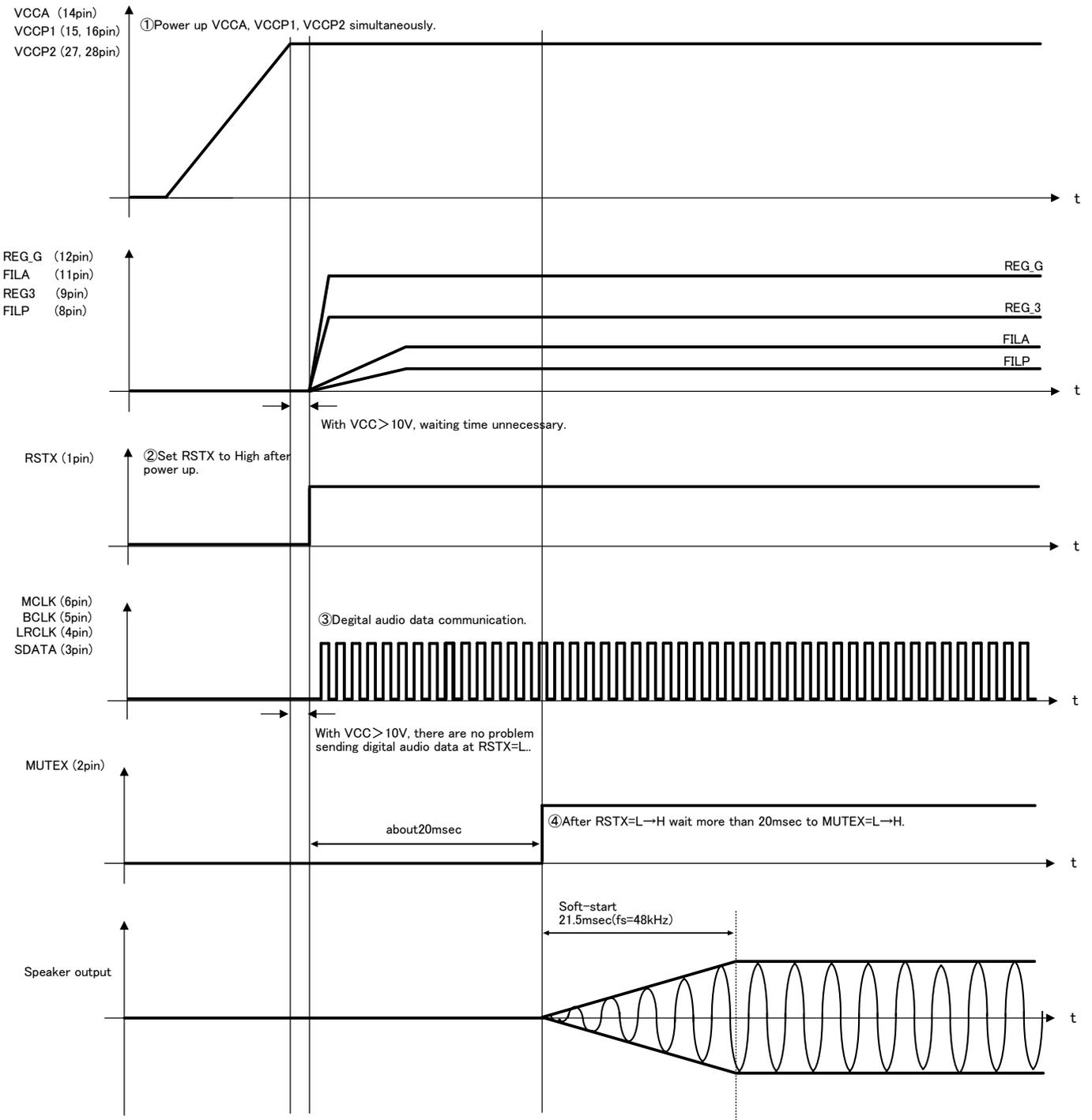
Fig.36 Audio Interface timing (2)

Parameter	Symbol	Limit		Unit
		Min.	Max.	
1 MCLK frequency	fMCLK	8.192	12.288	MHz
2 LRCLK frequency	fLRCLK	32	48	kHz
3 BCLK frequency	fBCLK	2.048	3.072	MHz
4 Setup time, LRCLK※1	tSU;LR	20	—	ns
5 Hold time, LRCLK※1	tHD;LR	20	—	ns
6 Setup time, SDATA	tSU;SD	20	—	ns
7 Hold time, SDATA	tHD;SD	20	—	ns
8 Setup time, BCLK※2	tSU;BC	3	—	ns
9 Hold time, BCLK※2	tHD;BC	7	—	ns

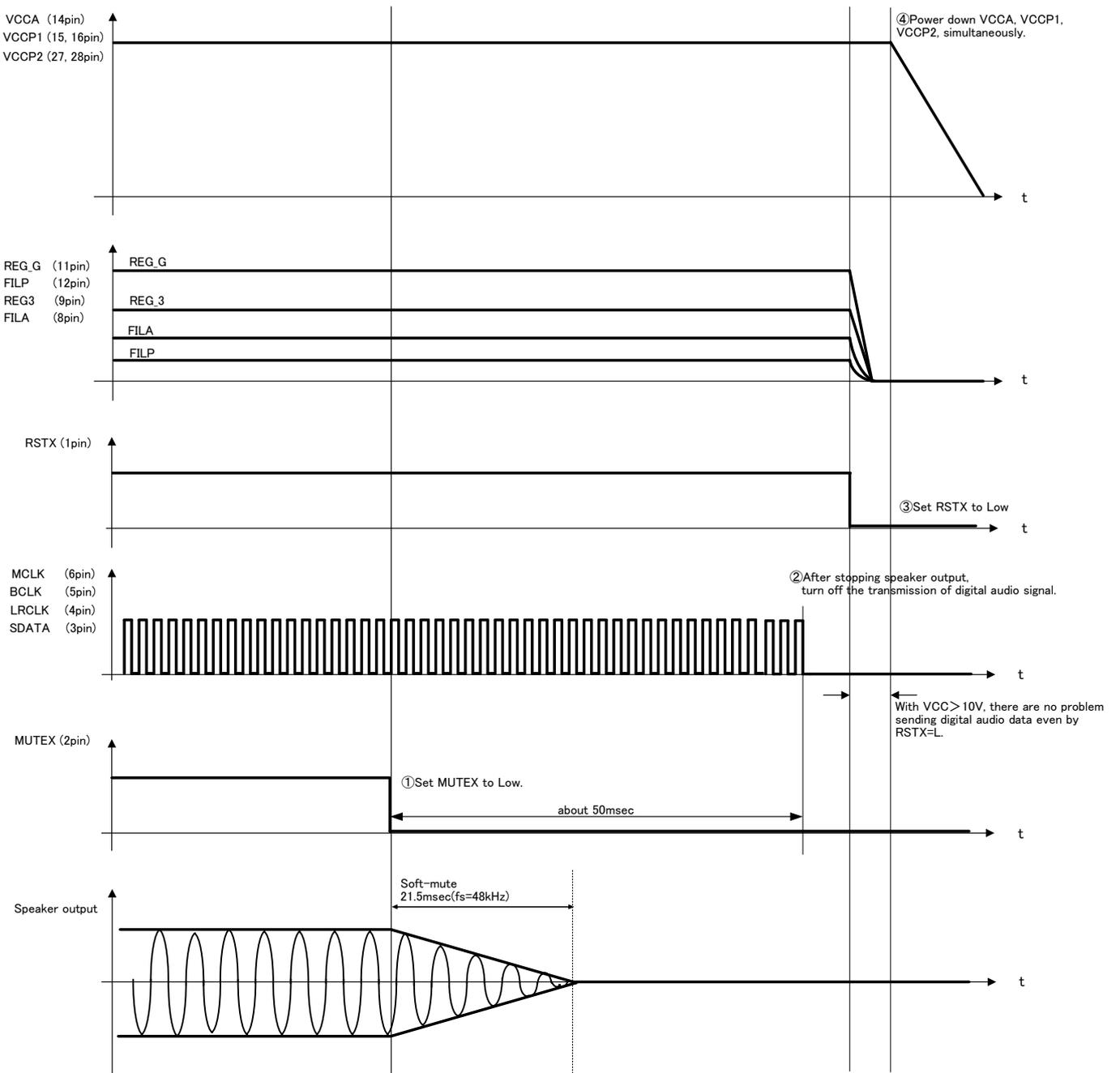
※1 This regulation is to keep rising edge of LRCK and rising edge of BCLK from overlapping.

※2 This regulation is to keep rising edge of MCLK and rising edge of BCLK from overlapping.

●Power supply start-up sequence



●Power supply shut-down sequence



●About the protection function

Protection function	Detecting & Releasing condition		PWM Output	ERROR Output
Output short protection	Detecting condition	Detecting current = 10A (TYP.)	HiZ_Low (Latch)	L (Latch)
DC voltage protection in the speaker	Detecting condition	PWM output Duty=0% or 100% 43msec(fs=48kHz) above fixed	HiZ_Low (Latch)	L (Latch)
High temperature protection	Detecting condition	Chip temperature to be above 150°C (TYP.)	HiZ_Low	H
	Releasing condition	Chip temperature to be below 120°C (TYP.)	Normal operation	
Under voltage protection	Detecting condition	Power supply voltage to be below 8V (TYP.)	HiZ_Low	H
	Releasing condition	Power supply voltage to be above 9V (TYP.)	Normal operation	
Over voltage Protection	Detecting condition	Power supply voltage to be above 21.5V(TYP.)	HiZ_Low	H
	Releasing condition	Power supply voltage to be below 20.5V(TYP.)	Normal operation	
Clock stop protection	Detecting condition	No change to MCLK more than 1μsec (TYP.) or no change to BCLK more than 1μsec (TYP.) or no change to LRCLK more than 21μsec (at fs=48kHz.).	HiZ_Low	H
	Releasing condition	Normal input to MCLK, BCLK and LRCLK.	Normal operation	

* The ERROR pin is Nch open-drain output.

* Once an IC is latched, the circuit is not released automatically even after an abnormal status is removed.

The following procedures ① or ② is available for recovery.

①After turning MUTEX terminal to Low(holding time to Low = 10msec(Min.)) turn back to High again.

②Restore power supply after dropping to power supply voltage $V_{cc} < 3V$ (10msec (Min.) holding) which internal power on reset circuit activates.

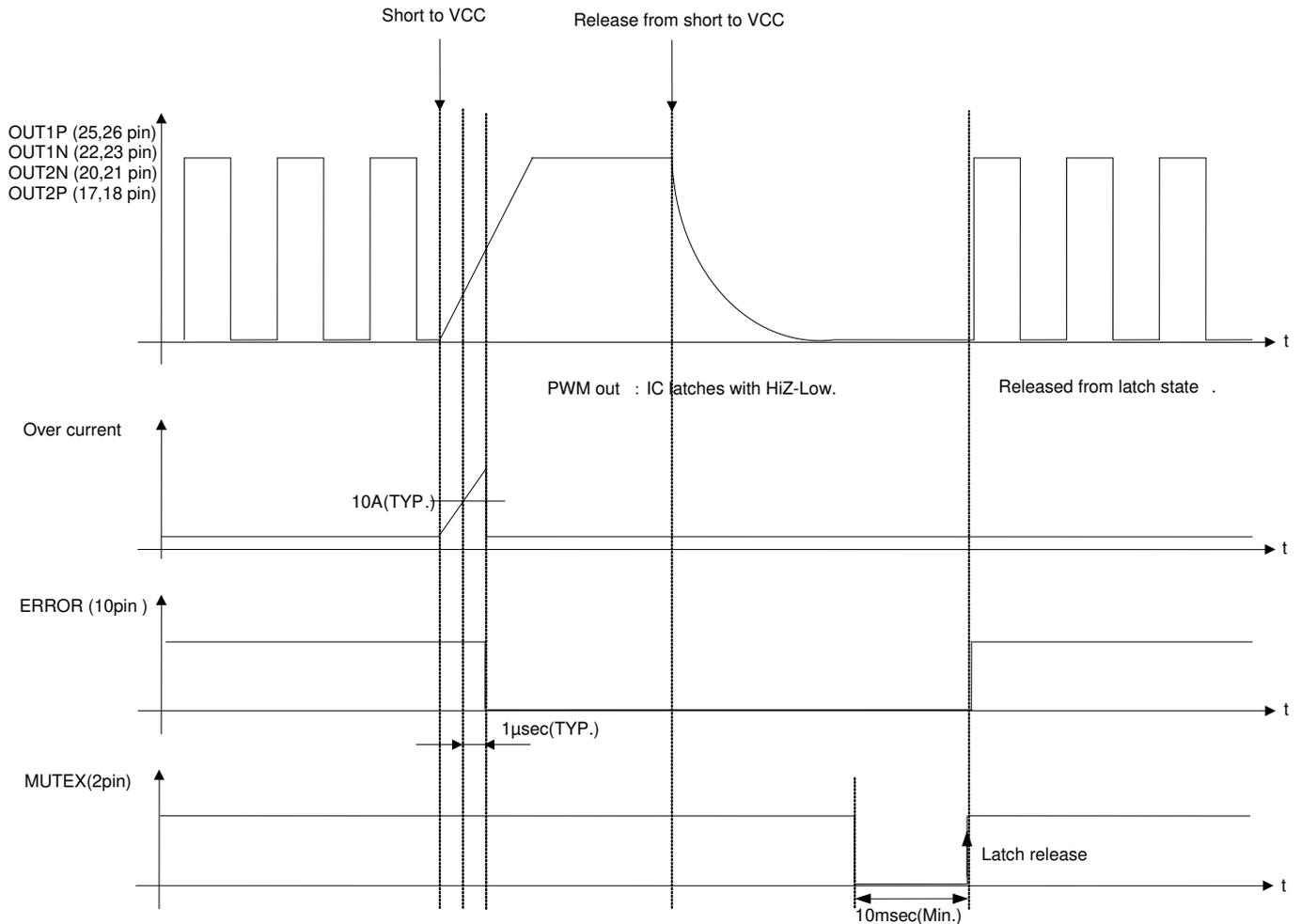
1) Output short protection(Short to the power supply)

This IC has the PWM output short protection circuit that stops the PWM output when the PWM output is short-circuited to the power supply due to abnormality.

Detecting condition - It will detect when MUTEX pin is set High and the current that flows in the PWM output pin becomes 10A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method - ①After turning MUTEX terminal to Low(holding time to Low = 10msec(Min.)) turn back to High again.

②Restore power supply after dropping to power supply voltage $V_{cc} < 3V$ (10msec (Min.) holding) which internal power on reset circuit activates.



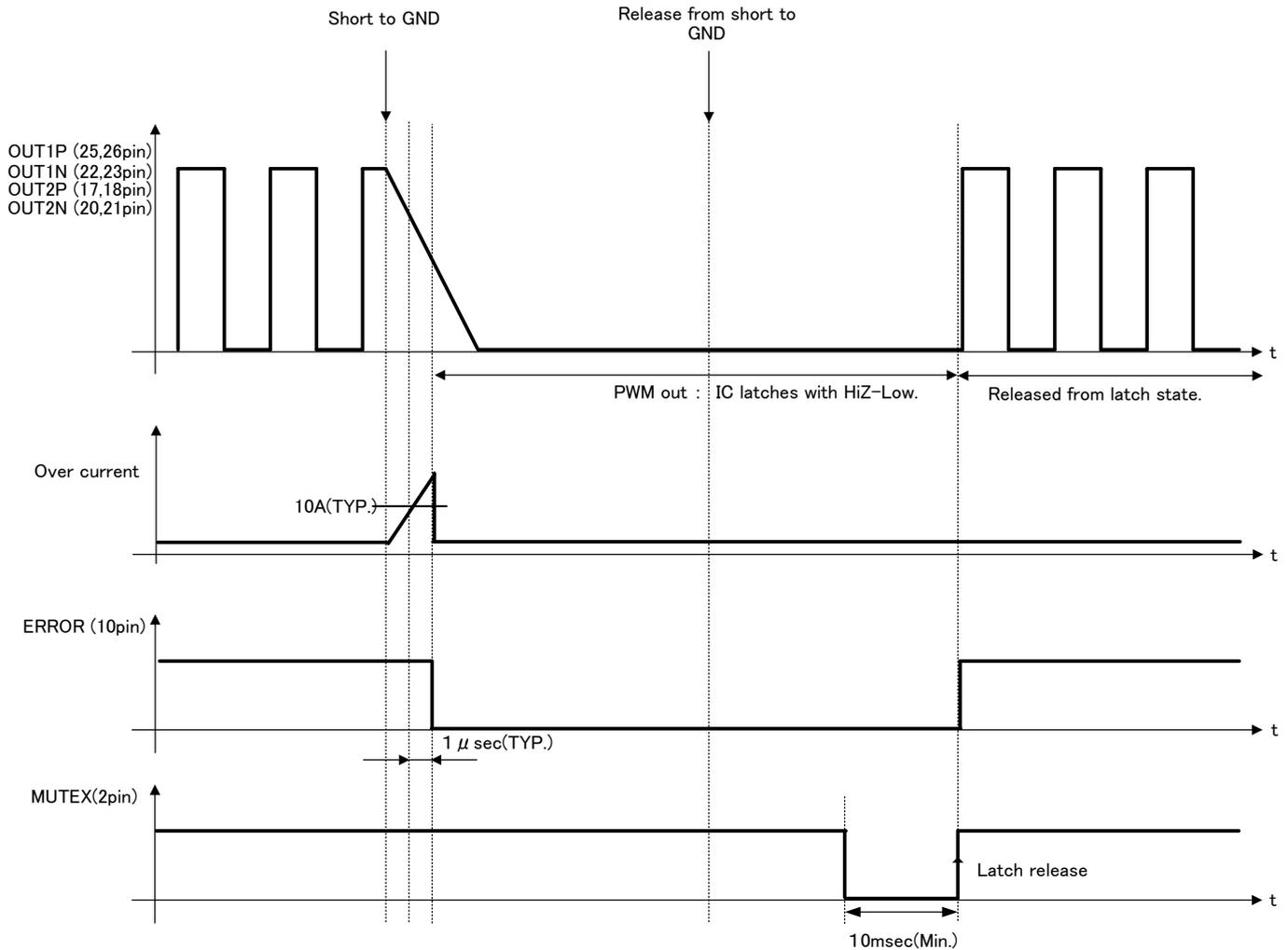
2) Output short protection(Short to GND)

This IC has the PWM output short protection circuit that stops the PWM output when the PWM output is short-circuited to GND due to abnormality.

Detecting condition - It will detect when MUTEX pin is set High and the current that flows in the PWM output terminal becomes 10A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method - ①After turning MUTEX terminal to Low(holding time to Low = 10msec(Min.)) turn back to High again.

②Restore power supply after dropping to power supply voltage $V_{cc} < 3V$ (10msec (Min.) holding) which internal power on reset circuit activates.



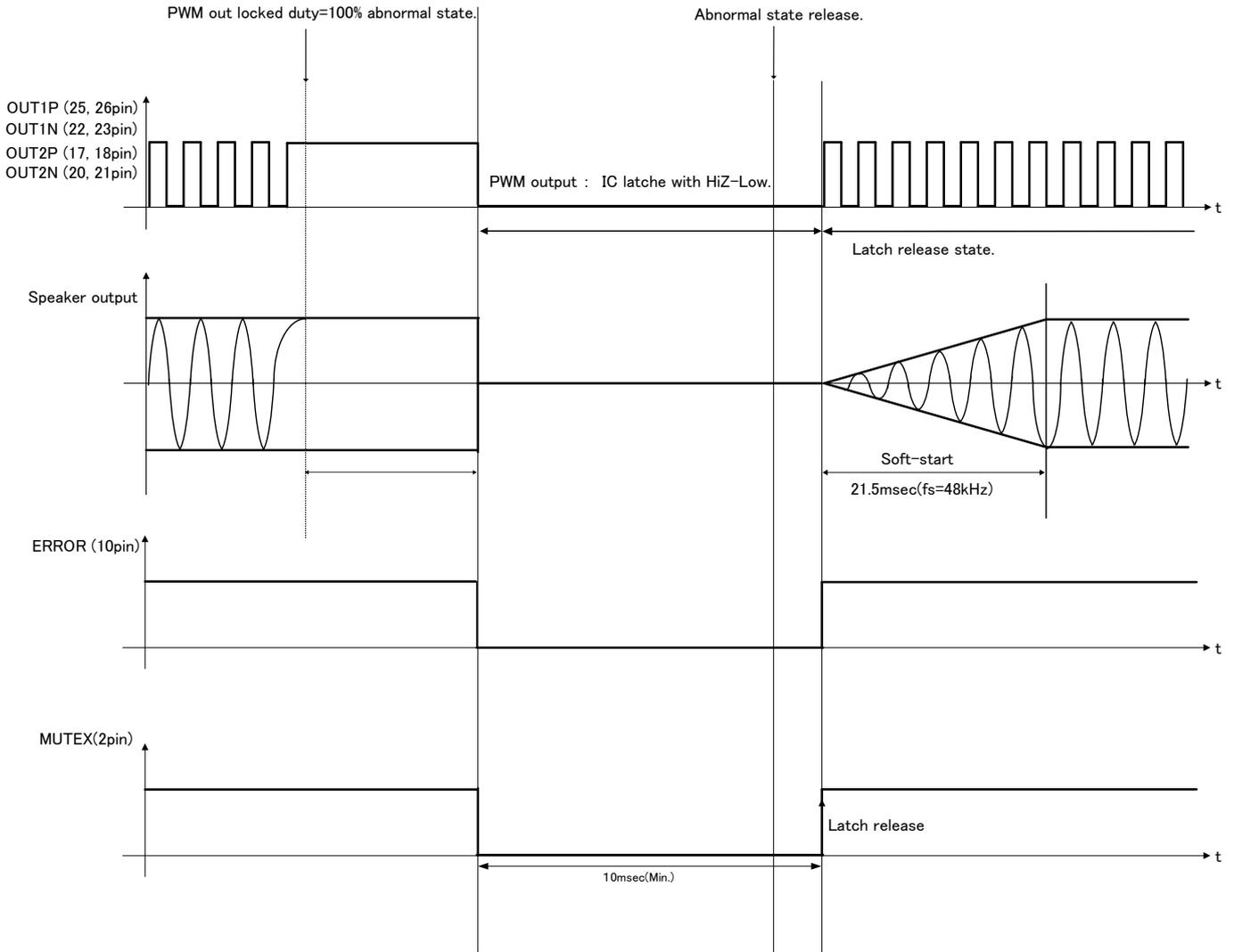
3) DC voltage protection in the speaker

When the DC voltage in the speaker is impressed due to abnormality, this IC has the protection circuit where the speaker is defended from destruction.

Detecting condition - It will detect when MUTE_X pin is set High or Low and PWM output Duty=0% or 100% , 43msec(fs=48kHz) or above. Once detected, The PWM output instantaneously enters the state of HiZ-Low, and IC does the latch.

Releasing method – ①After turning MUTE_X terminal to Low(holding time to Low = 10msec(Min.)) turn back to High again.

②Restore power supply after dropping to power supply voltage V_{cc}<3V(10msec (Min.) holding) which internal power on reset circuit activates.

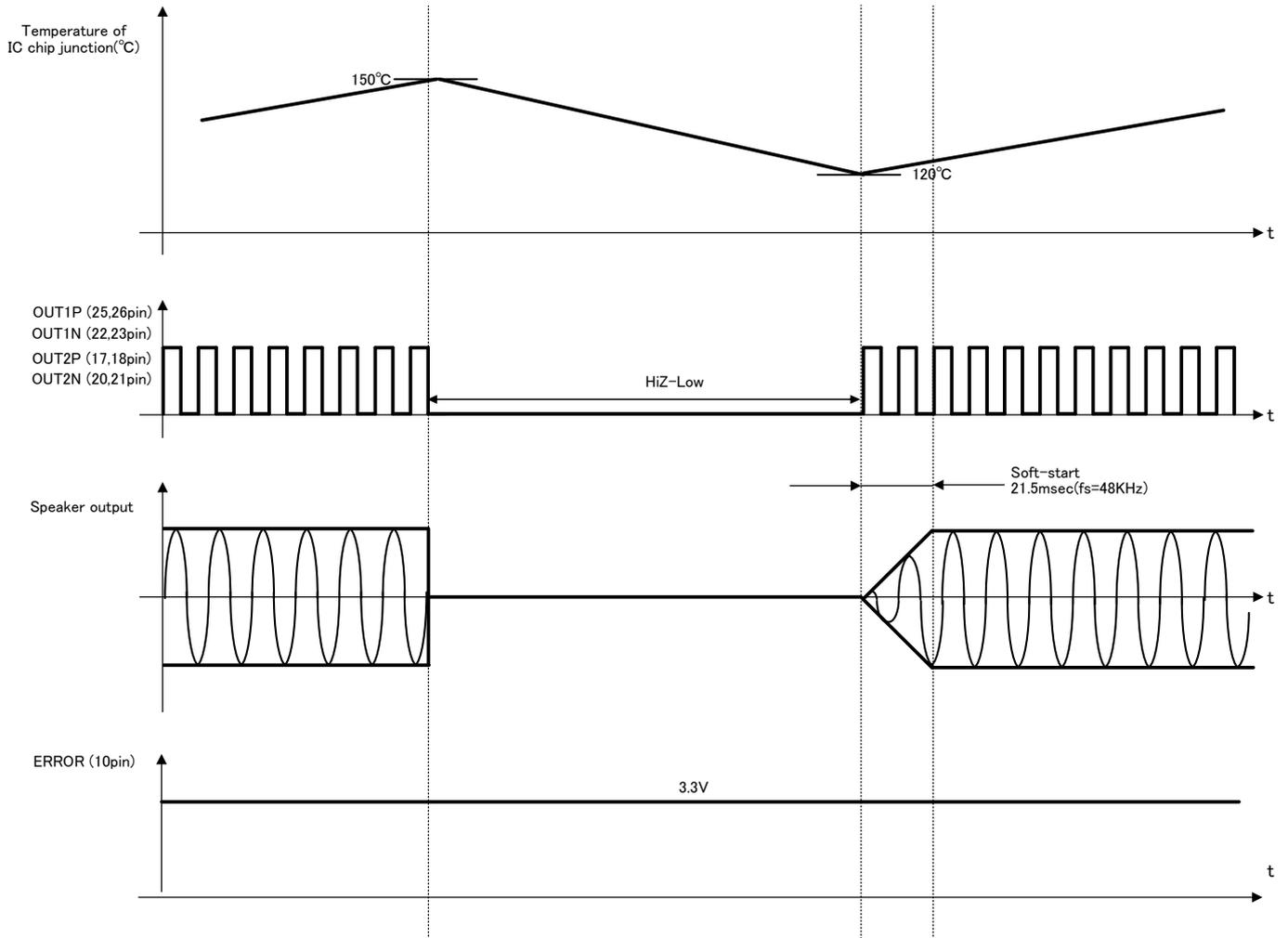


4) High temperature protection

This IC has the high temperature protection circuit that prevents thermal reckless driving under an abnormal state for the temperature of the chip to exceed $T_{jmax}=150^{\circ}\text{C}$.

Detecting condition - It will detect when MUTEX pin is set High and the temperature of the chip becomes 150°C (TYP.) or more. Speaker output turn MUTE immediately, when High temperature protection is detected.

Releasing condition - It will release when MUTEX pin is set High and the temperature of the chip becomes 120°C (TYP.) or less. The speaker output is outputted through a soft-start when released.

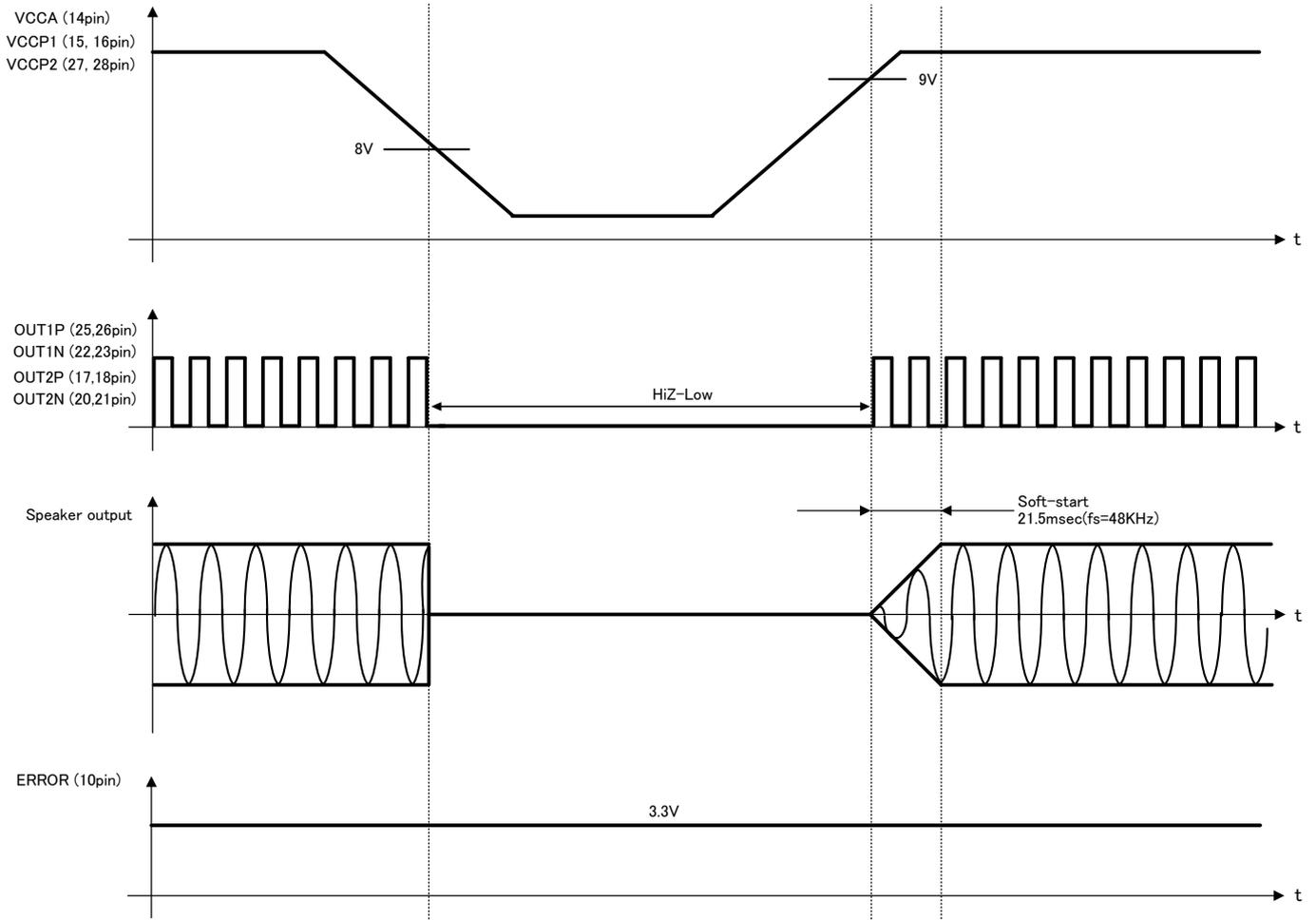


5) Under voltage protection

This IC has the under voltage protection circuit that make speaker output mute once detecting extreme drop of the power supply voltage.

Detecting condition – It will detect when MUTEX pin is set High and the power supply voltage becomes lower than 8V. Speaker output turn MUTE immediately, when Under voltage protection is detected.

Releasing condition – It will release when MUTEX pin is set High and the power supply voltage becomes more than 9V. The speaker output is outputted through a soft-start when released.

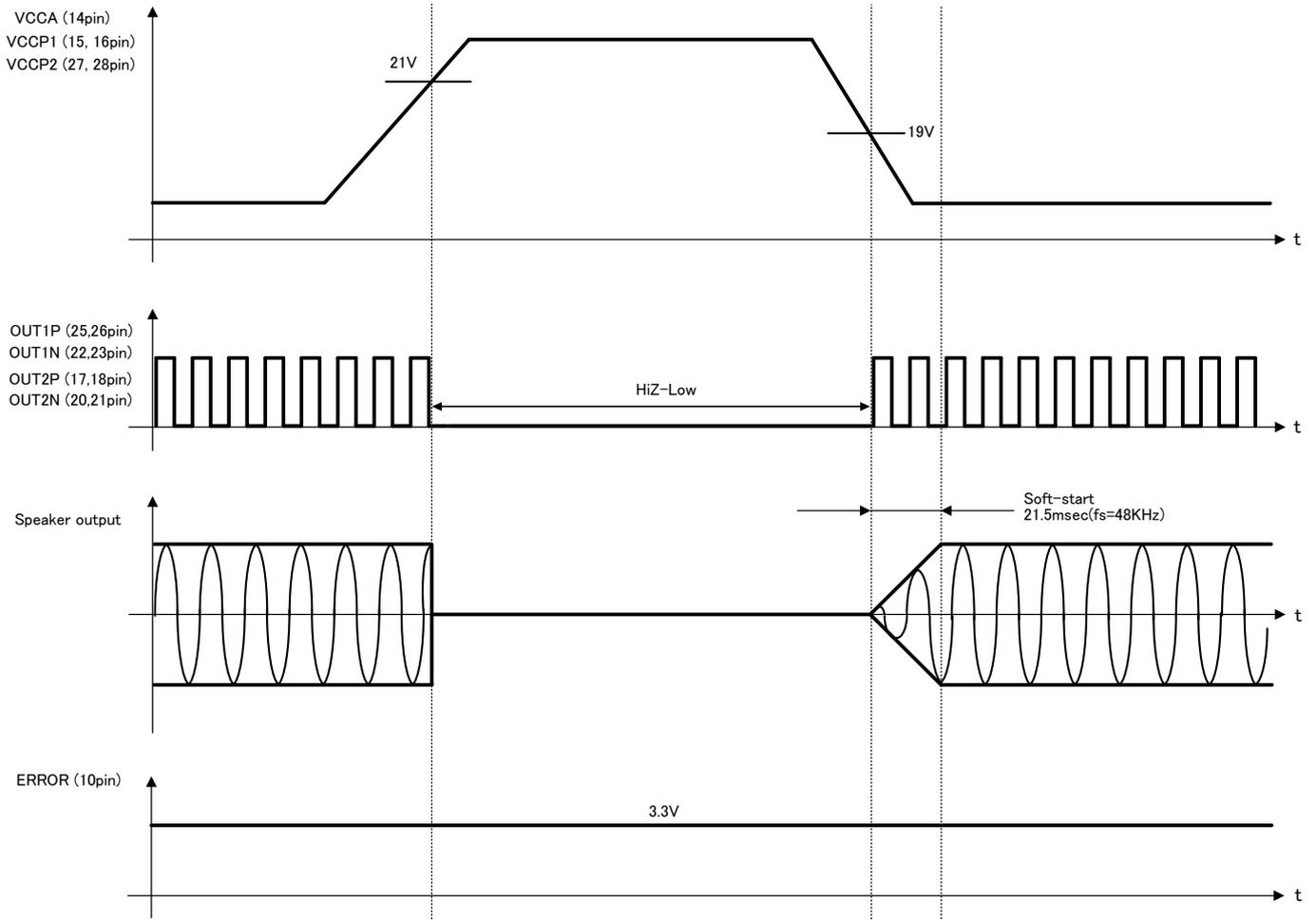


6) Over voltage protection

This IC has the under voltage protection circuit that make speaker output mute once detecting extreme drop of the power supply voltage.

Detecting condition – It will detect when MUTEX pin is set High and the power supply voltage becomes more than 21.5V. Speaker output turn MUTE immediately, when over voltage protection is detected.

Releasing condition – It will release when MUTEX pin is set High and the power supply voltage becomes lower than 20.5V. The speaker output is outputted through a soft-start when released.

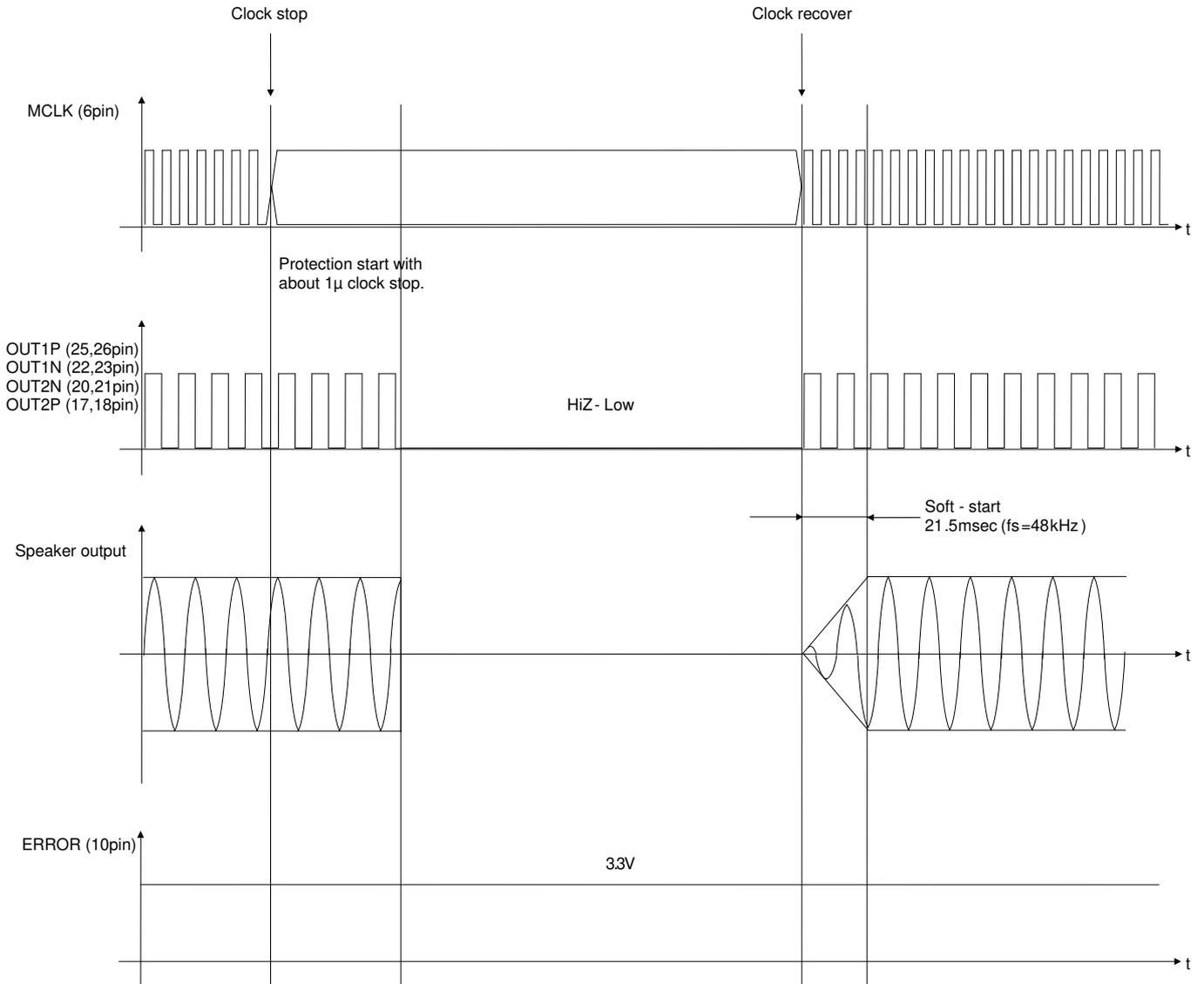


7-1) Clock stop protection(MCLK)

This IC has the clock stop protection circuit that make the speaker output mute when the MCLK signal of the digital audio input stops.

Detecting condition - It will detect when MUTEX pin is set High and the MCLK signal stops for about 1 μ sec or more. 21.5V. Speaker output turn MUTE immediately, clock stop protection is detected.

Releasing condition - It will release when MUTEX pin is set High and the MCLK signal returns to the normal clock operation. The speaker output is outputted through a soft-start when released.



7-2) Clock stop protection(BCLK)

This IC has the clock stop protection circuit that make the speaker output mute when the BCLK signal of the digital audio input stops.

Detecting condition - It will detect when MUTEX pin is set High and the BCLK signal stops for about 1 μ sec or more. 21.5V.Speaker output turn MUTE immediately, when clock stop protection is detected.

Releasing condition - It will release when MUTEX pin is set High and the BCLK signal returns to the normal clock operation. The speaker output is outputted through a soft-start when released.

