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OPEN-LOOP POL EVALUATION BOARD USER'S GUIDE

1. Kit Contents

The Open Loop Point of Load (POL) Evaluation Board contains the following items:

- Open-Loop Evaluation Board featuring:
 - Si8234 ISODriver
 - Si8512 AC Current Sensor
 - Si8540 DC Current Sensor

1.1. Hardware Overview

The Open Loop POL Evaluation Board implements a single-phase POL (an architecture similar to that found in switch-mode power supplies, motor control, inverters, and ballast lighting) whose switching frequency can be varied from 100 to 500 kHz. Its duty cycle can be varied from 20 percent to 80 percent. Figure 1 illustrates a high-level schematic overview. This variability provides a convenient means to fully evaluate the various products featured on the board. The Open Loop POL evaluation board shown in Figure 2 uses Silicon Laboratories' Si8234 ISODriver to drive the high-side and low-side FETs. It uses two Si8512 ac current sensors to monitor the switching currents in the high-side and low-side FETs respectively. The board also uses the Si8540 dc current sensor to monitor the dc current being delivered to the load. Refer to the Si85xx, Si823x, and Si854x family data sheets for more information concerning their operation.

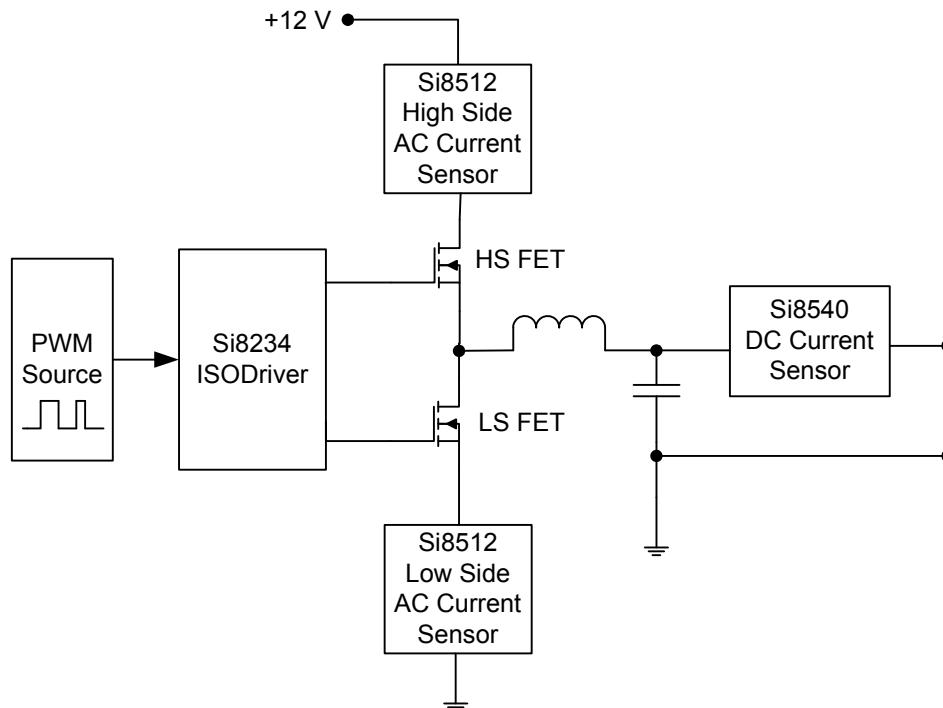


Figure 1. Open Loop POL High-Level Schematic

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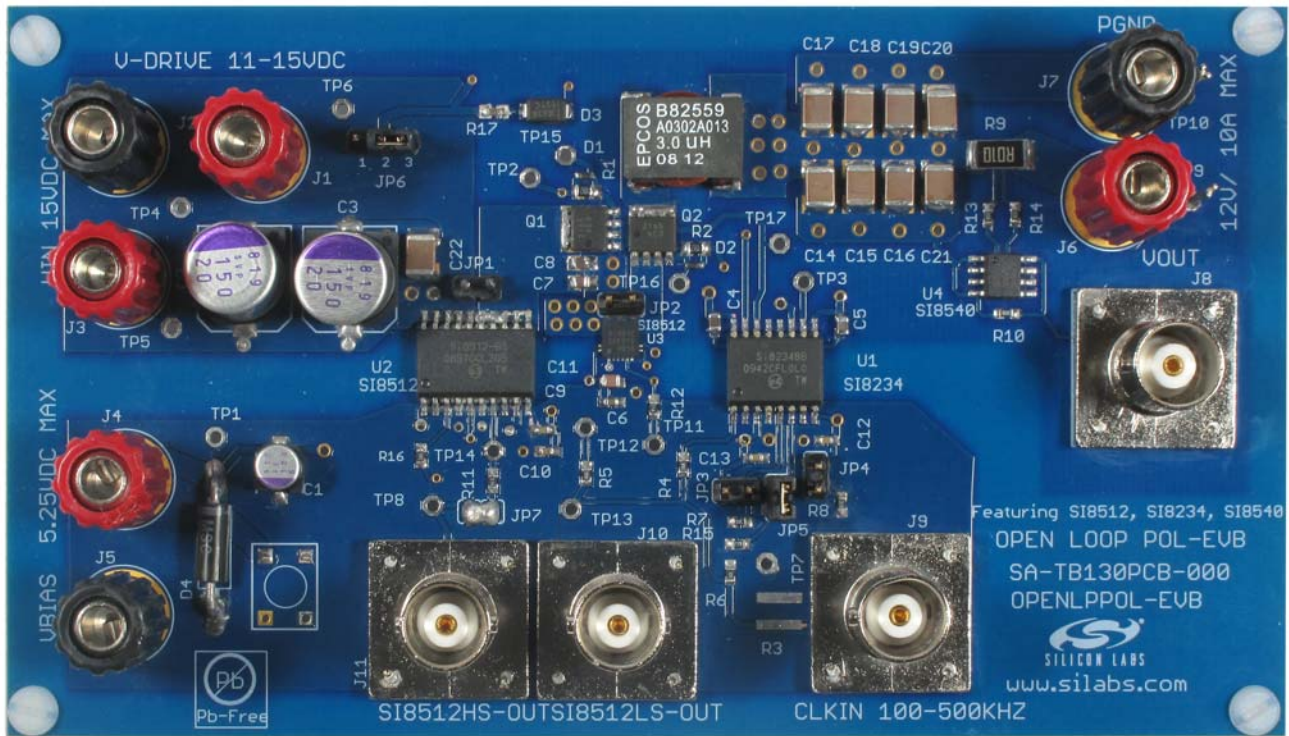


Figure 2. Open Loop POL Evaluation Board

2. Required Equipment

The following equipment is required:

- 1 digital multi-meter
- 2 multi-meter test leads (black and red)
- 1 oscilloscope (Tektronix TDS 2024B or equivalent)
- 1 BNC splitter
- 5 BNC cables
- 1 dc power supply (HP6024A, 15 V dc, 0–5 A or equivalent)
- 2 banana to banana wires (black and red)
- 1 electronic load simulator (Kikusui PLZ164WA or equivalent)
- 1 Agilent 33220A 20 MHz function/arbitrary wave generator or equivalent
- Open-Loop POL Evaluation Board (board under test)
- Open-Loop POL Evaluation Board User's Guide (this document)

3. Hardware Overview and Demo

The POL evaluation board is designed to provide a nominal 6.0 V output with a 250 kHz, 50 percent duty cycle input (this assumes a 12 V input voltage on J3 VIN). It is not recommended that the electronic load exceed 10 A of output current. The safest operating range for the E-Load is up to 5 A.

This test tests the basic function of the Open Loop POL board.

3.1. Board Jumper Settings

1. See Figure 1.
2. Ensure that J2, J5, and J7 are black and that J1, J3, J4, and J6 are red.
3. Ensure that the shunts are installed on JP5 and pins 2 and 3 of JP6.
4. Ensure that no shunt is installed on JP4.

3.2. DC Supply Configuration

1. Turn ON the DC Power supply.
2. Adjust one DC Power Supply to provide 12 V on its output.
3. Adjust a second DC Power Supply to provide 5 V on its output.
4. Connect the Black and Red Banana terminated wires to the outputs of the DC supply.
5. Turn OFF the DC Power Supplies.
6. Connect the 12 V Red and Black terminated wires to the Open Loop POLs J3 (Red wires here) and J2 (Black wire here). The positive terminal is J3.
7. Connect the 5 V Red and Black terminated wires to the Open Loop POLs J4 (Red wires here) and J5 (Black wire here). The positive terminal is J4.

3.3. Wave Form Generator

1. Turn ON the Arbitrary Wave Form Generator.
2. Adjust its output to provide a 250 kHz, 0 to 5 V peak-to-peak square wave output with 50 percent duty cycle.
3. Split the output of the Generator with a BNC splitter
4. Connect a BNC cable from the output of the Arbitrary Wave Form Generator to J9 (CLKIN) on the Open Loop POL board.
5. Connect another BNC cable from the output of the Arbitrary Wave Form Generator to CH1 of the oscilloscope.
6. Engage the output of the Wave Form Generator.

3.4. Oscilloscope Setup

1. Turn on the Oscilloscope.
2. Connect a BNC from J11 (OUT85xxHS) to CH2.
3. Connect a BNC from J10 (OUT85xxLS) to CH3.
4. Connect a BNC from J8 (OUT8540) to CH4.
5. Set the scope to Trigger on CH1 and adjust Trigger Level to 1 V minimum.
6. Set CH1 to 5 V per division; set CH2/3 to 1 V per division, and set CH4 to 200 mV per division.
7. Adjust the Seconds/Division setting to 1 μ s/division.
8. Adjust the level indicator for ALL channels to properly view each channel as shown in Figure 5.

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3.5. Electronic Load

1. Connect output of the Electronic Load to J6 (positive terminal) and J7 (negative terminal).
2. Adjust the output of the electronic load to provide 2.5 A.
3. See Figure 3 for a summary diagram of the test setup.

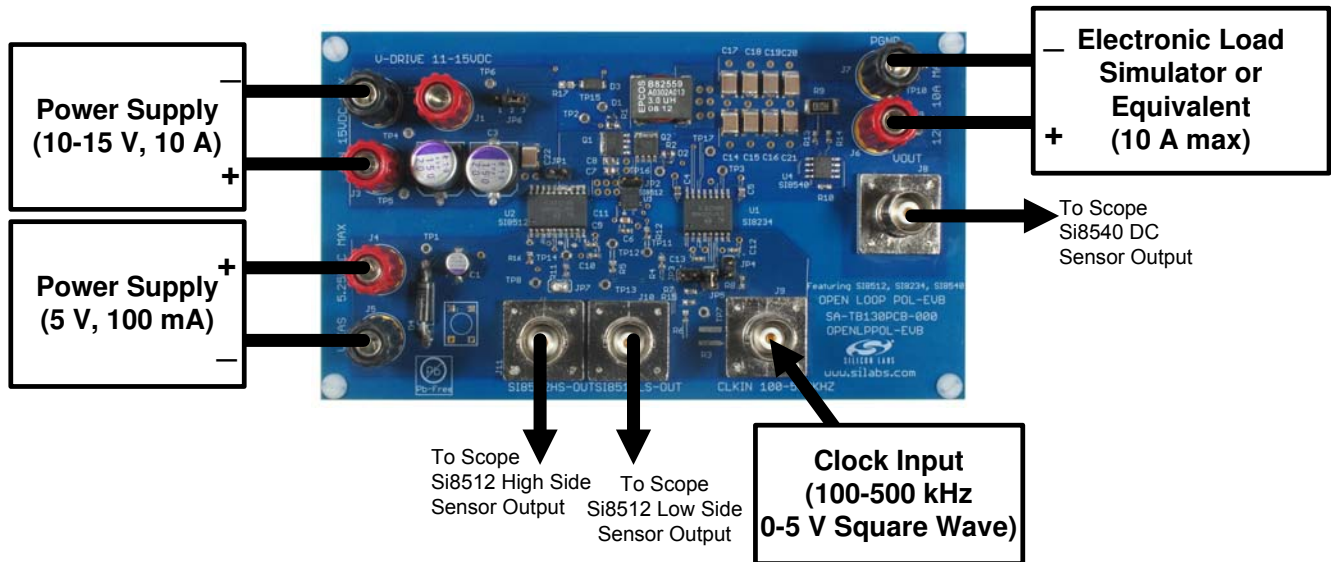


Figure 3. Summary Diagram of Test Setup

4. Turn ON the DC Power Supplies.
5. Use the digital multi-meter to measure the voltage across J6 (positive lead) to J7 (negative lead). The voltage should measure approximately 6 V.
6. Engage the output of the Electronic Load (see Figure 4). If an electronic load is not available, a 15 W, 3 Ω resistor can be used.



Figure 4. Kikusui PLZ164WA Setup

3.6. Test Conditions

The oscilloscope should display waveforms similar to Figure 5.

Channel 1 should output a signal with a peak voltage of 5 V and have similar slope as shown in Figure 5.

Channel 2 should output a signal with a peak voltage of 500 to 800 mV and have similar slope as shown in Figure 5.

Channel 3 should output a signal with a peak voltage of 500 to 800 mV and have similar slope as shown in Figure 5.

Channel 4 should output a signal with a peak voltage of 250 to 350 mV and have similar slope as shown in Figure 5.

The user can now vary the Open Loop POL's input frequency (from 100 to 500 kHz), duty cycle (from 20 to 80 percent), and load (from 0 to 10 amps) to get a feel for how Silicon Labs' Si8512, Si8234, and Si8540 operate in a real world power supply.

3.7. Isolated Supply Connection

The Open Loop POL's Si8234 ISOdriver's outputs can be powered from a separate, quieter supply if desired. To accommodate this:

1. Move shunt on JP6 from position 2–3 to position 1–2.
2. Connect a 10–15 V supply between J1 (Red wire here) and J2 (Black wire here). The positive terminal is J1.

All the above outputs on Ch1-Ch4 of the scope should be the same.

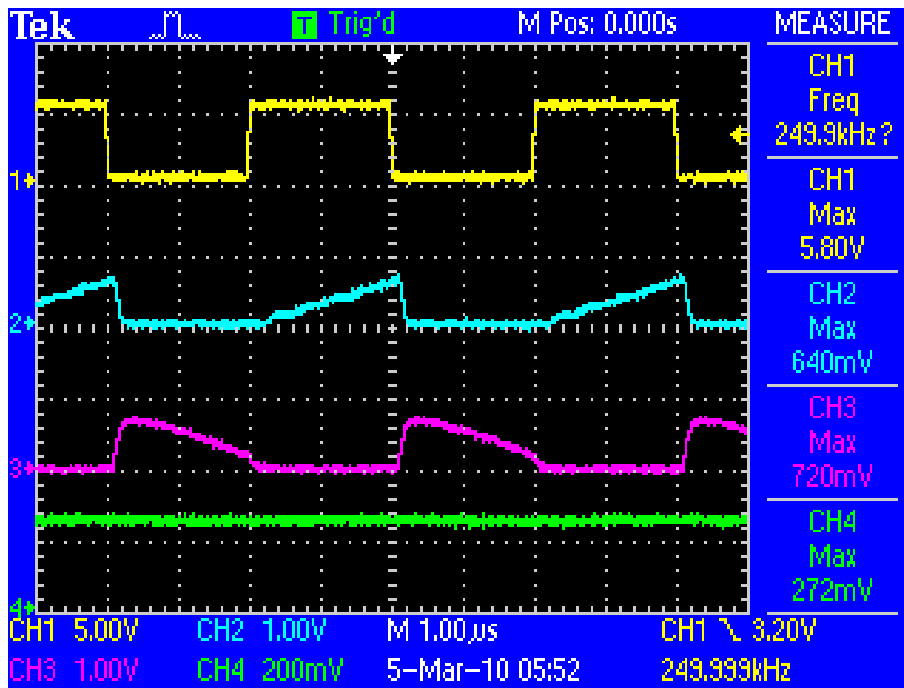


Figure 5. Oscilloscope Display

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4. Open Loop POL Evaluation Board

The Open Loop POL evaluation board has an Si8234, two Si8512s (both the QFN and SOIC packages) and a Si8540 installed. There are two Si8412s (QFN and SOIC packages) installed to allow users to evaluate either package. Refer to Figure 6 for the locations of the various I/O connectors and major components.

- J1, J2, J3, Input Power: Input power connection 10–15 V, 10 A.
- J4, J5 VBIAS: Isolated Input power connection 5 V, 100 mA.
- J6, J7, VOUT: Supply output connection for load simulator.
- J8, OUT8540: BNC provides output of Si8540, dc current to load.
- J9 CLKIN: Input Clock for POL.
- J10, OUTLS8512: BNC provides output of Si8512, ac current through Q2.
- J11, OUTHS8512: BNC provides output of Si8512, ac current through Q1.
- JP3 Disable Control: Disables VOA and VOB of Si8234.
- JP4 Deadtime Control: Provides ~900 ns of deadtime when populated.
- JP5 Deadtime Control: Provides ~70 ns of deadtime when populated.
- JP6 ALTSPLY: Alternate means to power driver outputs.

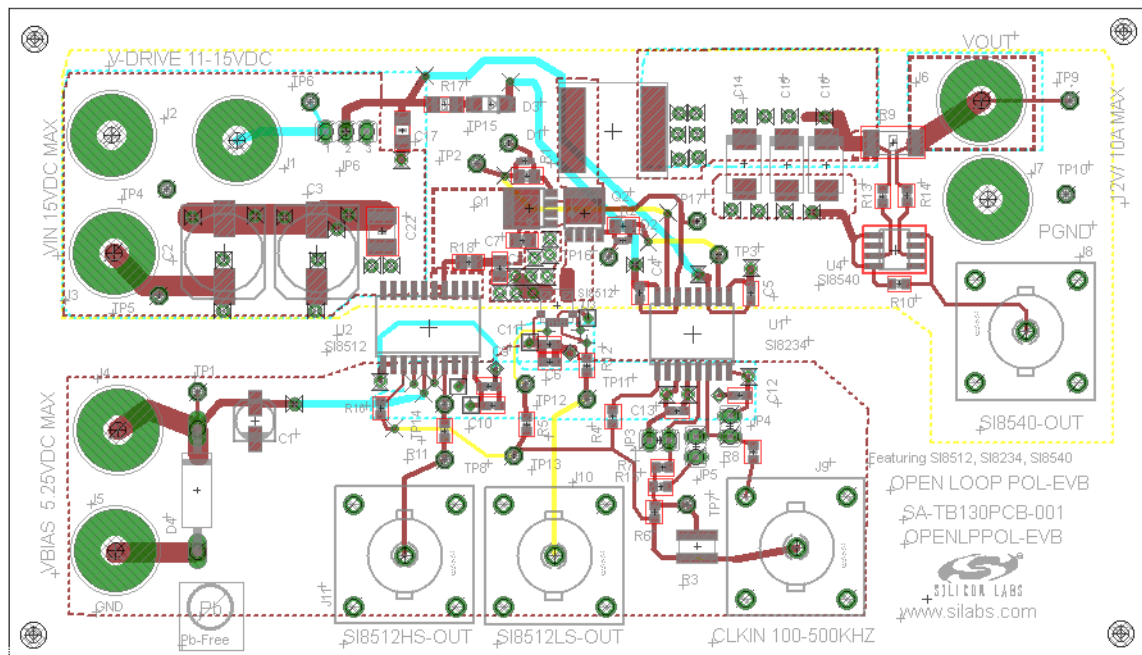


Figure 6. Open Loop POL Evaluation Board Silkscreen

4.1. Voltage and Current Sense Test Points

The Open Loop POL evaluation board has several test points. These test points correspond to the respective pins on the Si8234, Si8512 and Si8540 integrated circuits as well as other useful inspection points. See See “5. Schematic” on page 7. for more details.

5. Schematic

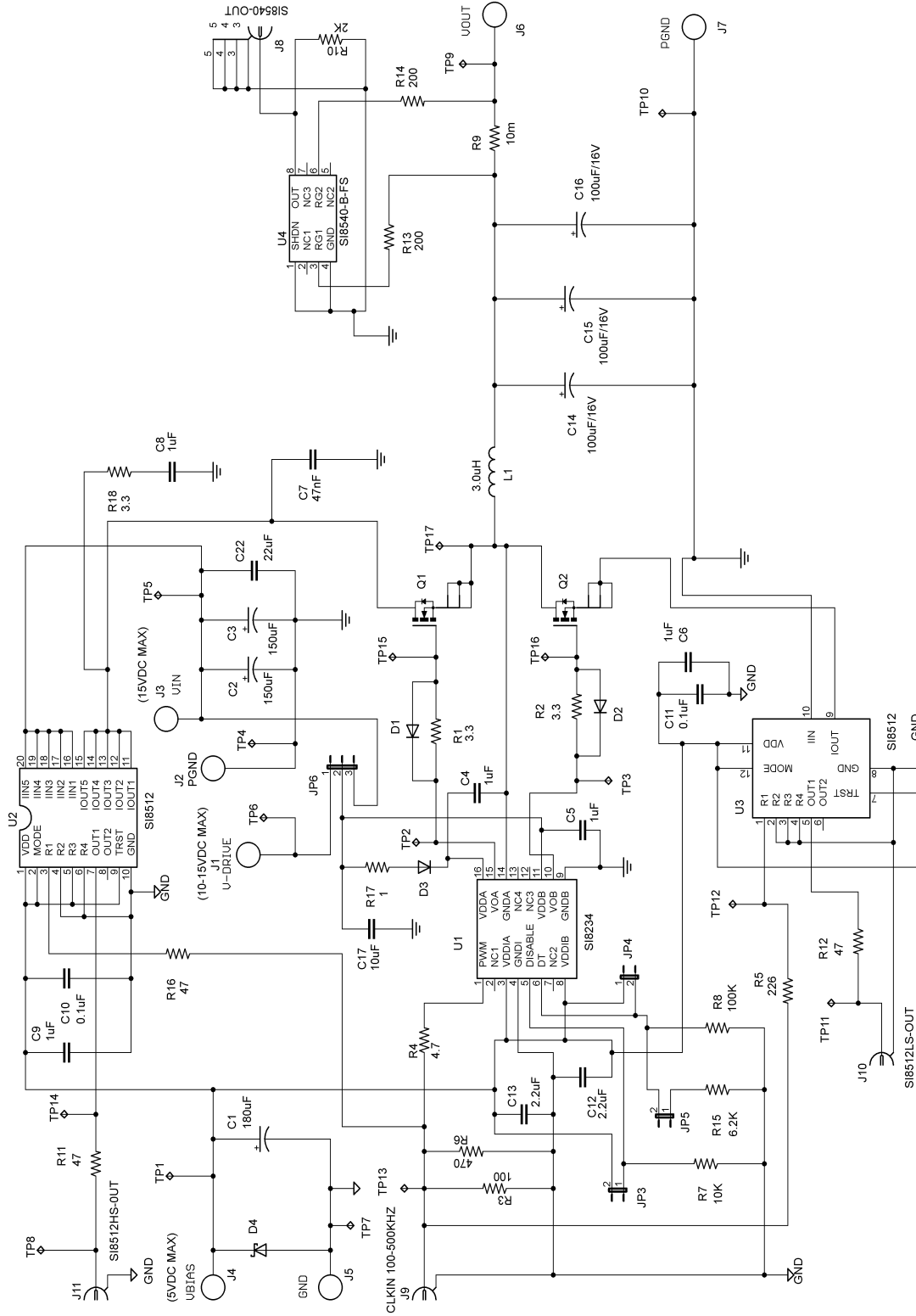


Figure 7. Open Loop POL Evaluation Board Schematic (Power)

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6. Bill of Materials

Table 1. Open Loop POL Evaluation Board Bill of Materials

Qty	Ref	Value	Rating	Tol	Part Number	Mfr
1	C1	180 μ F	6.3 V	20%	6SVPE180M	Sanyo
2	C2, C3	150 μ F	20 V	20%	20SVP150M	Sanyo
5	C4-C6, C8, C9	1 μ F	25 V	10%	C0603X5R250-105K	Venkel
1	C7	47 nF	25 V	20%	C0603X7R250-473MGE	Venkel
2	C10, C11	0.1 μ F	25 V	10%	C0603X5R250-104K	Venkel
2	C12, C13	2.2 μ F	10 V	10%	C0603X5R100-225K	Venkel
3	C14, C15, C16	100 μ F	16 V	20%	16TQC100M	Sanyo
1	C22	22 μ F	16 V	20%	C1812X5R160-226M	Venkel
1	C17	10 μ F	25 V	10%	C1206X5R250-106KNE	Venkel
2	D1, D2	200 mA 75 V - SOD523	200 mA 75 V		BAS16XV2T1G	On Semi
1	D3	1 A 100 V - DO214AC	1 A 100 V		ES1C	Vishay
1	D4	6.8 V	6.8 V 600 mW		P6KE6.8A	Littlefuse Inc.
1	U1	SI8234BB-C-IS SOIC16W	2.5 kVrms 5 kVrms		SI8234BB-C-IS Si8234BD-C-IS	Silicon Labs
1	U2	SI8512-C-ISSO20W			SI8512-C-IS	Silicon Labs
1	U3	SI8512-C-IMQFN12			SI8512-C-IM	Silicon Labs
1	U4	SI8540-B-FSSO8			SI8540-B-FS	Silicon Labs
4	J1, J3, J4, J6	Red Banana-jack			111-703-001	Johnson/Emerson
3	J2, J5, J7	Black Banana-jack			111-702-001	Johnson/Emerson
4	J8-J11	BNC Connector			227699-2	Tyco Electronics Amp
4	JP3-JP6	Jumper			TSW-102-07-T-S	Samtec
1	L1	3.0 μ H	13 A 5.1 m Ω		B82559A	Epcos
2	Q1, Q2	N-CHANNEL MOS-FETLFPK			HAT2165H	Renesas

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Table 1. Open Loop POL Evaluation Board Bill of Materials (Continued)

Qty	Ref	Value	Rating	Tol	Part Number	Mfr
3	R1, R2, R18	3.3 Ω (0805)	1/10 W	5%	CR0805-10W-3R3JT	Venkel
1	R3	100 Ω	1/4 W	5%	cr1210-4W-101JT	Venkel
1	R4	4.7 Ω	1/16 W	5%	CR0603-16W-4R7JT	Venkel
2	R5	226 Ω (0603)	1/16 W	1%	CR0603-16W-2260FT	Venkel
2	R6	470 (0603)	1/16 W	5%	CR0603-16W-471JT	Venkel
1	R7	10 k Ω (0603)	1/16 W	105%	CR0603-16W-103JT-14	Venkel
1	R8	100 k Ω (0603)	1/16 W	5%	CR0603-16W-104T-13	Venkel
1	R9	10 m Ω	2 W	1%	LCR2512R010FT	Venkel
1	R10	2 k Ω (0603)	1/16 W	5%	CR0603-16W-202JT	Venkel
3	R11, R12, R16	47 Ω (0603)	1/16 W	5%	CR0603-16W-470JT	Venkel
2	R13, R14	200 Ω (0603)	1/16 W	1%	CR0603-16W-2000F	Venkel
1	R15	6.2 k Ω (0603)	1/16 W	5%	CR0603-16W-622JT	Venkel
1	R17	1 Ω (1206)	1/4 W	5%	CR1206-8W-1R0JT	Venkel
17	TP1-TP17	Testpad			151-201	Kobiconn
4	MH1-4	Stand off/screw			1902EK-ND/H546	Digikey

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7. Ordering Guide

Table 2. Open Loop POL Evaluation Board Ordering Guide

Ordering Part Number	Description
OPENLPPOL-EVB	Open Loop Point-of-Load evaluation board

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Revised entire document to reflect board revision from using Si8410 to using Si8234.
- Removed Figure 6, "Open Loop POL Evaluation Board Schematic (Sense)".
- Added Ordering Guide.

Revision 0.2 to Revision 0.3

- Updated "3.1. Board Jumper Settings" on page 3.
 - Deleted JP3 in Step 3.
- Updated "3.5. Electronic Load" on page 4.
 - Updated Step 6.
 - Added Figure 4 on page 4.

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