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ORCA® ORT/ORSO42G5 High-Speed SERDES Board

User's Guide

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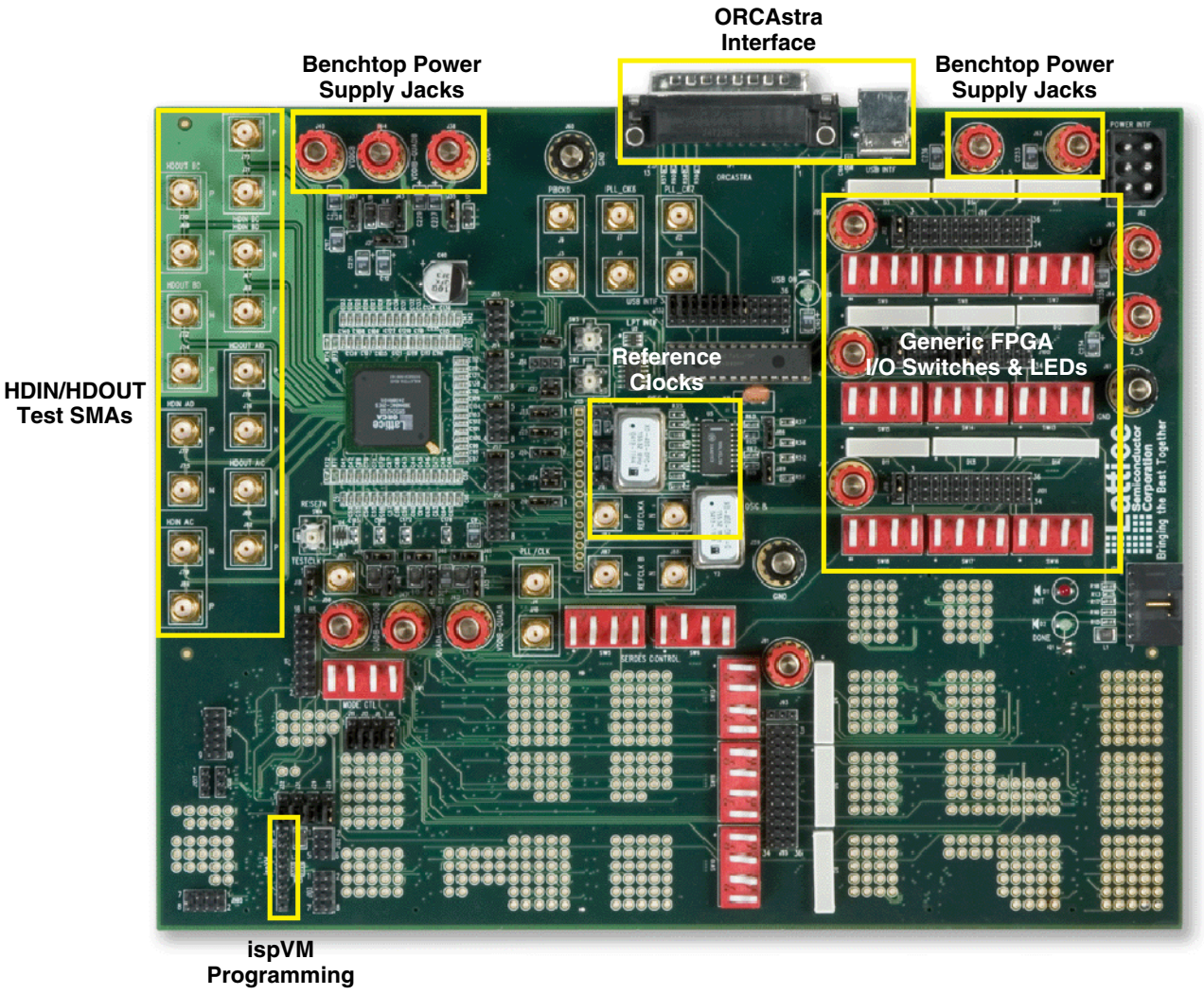
Introduction

This user's guide describes the Lattice High-Speed SERDES Board for the ORCA ORT/ORSO42G5 device, a stand-alone evaluation PCB that provides a functional platform for device feature demonstrations. The board includes the following features:

- Power connections
- ispVM® programming support
- On-board and external reference clock sources
- Discrete high-speed interface SMA test points and clock connections
- ORCAstra Demonstration Software interface
- Varied high-speed layout structures

The contents of this user's guide include top level functional descriptions of the various portions of the evaluation board, descriptions of the on-board connectors, diodes and switches and a complete set of schematics for version 1.1 of the board. Figure 1 shows the functional partitioning of the board.

Figure 1. ORT/ORSO42G5 High-Speed SERDES Board



J30

An 8-pin connector that provides the interface to the ispDOWNLOAD® cable.

Pin Number	Signal
Pin 1	VDD
Pin 2	TDO
Pin 3	TDI
Pin 4	N/C
Pin 5	N/C
Pin 6	TMS
Pin 7	GND
Pin 8	TCK

J21

A 7-pin serial connector used for serial configuration.

Pin Number	Signal
Pin 1	GND
Pin 2	NC
Pin 3	PROGRMN
Pin 4	DONE
Pin 5	D0
Pin 6	CCLK
Pin 7	VDD

Header Connections

Standard 0.100 headers are provided for interconnecting points on the board. This can be accomplished with 0.100 IDC connectors and ribbon cable for bus connections or 0.025 pin socket patch cords (such as Pomona Electronics #5948 (www.pomonelectronics.com). 0.100 jumpers shunts are also used for board selections such as Sullins Electronics P/N SPC02SYAN (www.sullinselectronics.com).

D1, D2

These LEDs indicate the status of configuration to the FPGA DONE/INITN status pins. When D2 is illuminated this indicates the successful completion of configuration. When D1illuminates, this indicates that programming was aborted or reinitialized.

J23, 25

These standard 3x1 headers provide connections of the PROGRAMN and RESETN control pins. For standard evaluation board use, a 2-pin shunt should be placed across pins 2 and 3. This will connect the pins to on-board push-button switches.

Pin Number		Signal
J23	Pin 1	Global
	Pin 2	PROGRMN
	Pin 3	Local
J25	Pin 1	Global
	Pin 2	RESETN
	Pin 3	Local

J24, 27

These standard 2x2 headers provide connection of the DONE and INITN status pins. For standard evaluation board use, a 2-pin shunt should be placed across pins 1 and 2. This will connect the pins to on-board LED indicators.

Pin Number		Signal
J24	Pin 1	Local
	Pin 2	DONE
	Pin 3	Global
	Pin 4	DONE
J27	Pin 1	Local
	Pin 2	INITN
	Pin 3	Global
	Pin 4	INITN

J28, 29, 31, 32

These standard 1x3 headers connect the JTAG pins to the ispVM down connection. For standard evaluation board use, a 2-pin shunt should be placed across pins 2 and 3. This will connect the pins to J30.

Pin Number		Signal
J28	Pin 1	Global
	Pin 2	TDO
	Pin 3	Local
J29	Pin 1	Global
	Pin 2	TDI
	Pin 3	Local
J31	Pin 1	Global
	Pin 2	TMS
	Pin 3	Local
J32	Pin 1	Global
	Pin 2	TCK
	Pin 3	Local

J5, 6, 11, 12

These standard 1x3 headers connect the configuration MODE pins to the on-board DIP switches. For standard evaluation board use, a 2-pin shunt should be placed across pins 2 and 3.

Pin Number		Signal
J5	Pin 1	Global
	Pin 2	Mode1
	Pin 3	Local
J6	Pin 1	Global
	Pin 2	Mode2
	Pin 3	Local
J11	Pin 1	Global
	Pin 2	Mode3
	Pin 3	Local
J12	Pin 1	Global
	Pin 2	Mode0
	Pin 3	Local

J18, 19, 20, 26

These standard 1x3 headers connect the CCLK, DIN, RDCFGN and PTEMP pins.

Pin Number		Signal
J18	Pin 1	PROM
	Pin 2	CCLK
	Pin 3	CABLE
J19	Pin 1	DATA0
	Pin 2	DIN
	Pin 3	CABLE
J20	Pin 1	3.3V
	Pin 2	RDCFGN
	Pin 3	CABLE
J26	Pin 1	3.3V
	Pin 2	PTEMP
	Pin 3	GND

Control Switches

The following switches provide the user control of the various control pins.

Switch	Use	Notes
SW1	Configuration Mode Pins[3:0]	A=M0,B=M1,C=M2,D=M3
SW2		Pushbutton for RESETN
SW3		Pushbutton for PROGMN
SW4		Pushbutton for PASB_RESETN(SERDES RESET)
SW5	Test pins	A=NC, B=NC, C=PDN, D=TRISTN
SW6	Test pins	A=PBIST, B=PLOOP, C-DOBIST,D=PSSIG_ALL

J13, 14, 16

These 2x1 standard headers connect the chip selects to various sources. For standard evaluation board use, place a shunt across J13, J14, J16, pins 1 and 2.

Pin Number		Signal
J13-CS0N	Pin 1	CS0N
	Pin 2	GND
J14-CS1	Pin 1	3.3V
	Pin 2	CS1
J16-CS1	Pin 1	Source
	Pin 2	CS1

J22

These 2x1 standard headers connect the LVDS_R pin to a 100-ohm resistor to GND. For standard evaluation board use, leave header open.

Pin Number	Signal
Pin 1	100-ohm
Pin 2	LDVS_R

General Purpose FPGA I/O Selection

These 12x3 standard headers connect the DIP switch packs or LEDs to general purpose I/O pins.

Pin Number	Signal
J94	GEN_FPGA[0:11]
J95	GEN_FPGA[24:35]
J100	GEN_FPGA[36:47]
J102	GEN_FPGA[12:23]

General Purpose Switch Selection

These 3x1 standard headers connect the DIP switch packs to either an externally supplied voltage or the on-board 2.5V source.

Switch	Selections
J92	GEN_FPGA_SWITCH_SEL[0:11]
J93	GEN_FPGA_SWITCH_SEL[24:35]
J98	GEN_FPGA_SWITCH_SEL[12:23]
J99	GEN_FPGA_SWITCH_SEL[36:47]

General Purpose LED Selection

These 3x1 standard headers connect the LED packs to the designated FPGA pin.

LED Bank	Selections
D3	LED array connected to J94-General IO[0:3]
D4	LED array connected to J95-General IO[24:27]
D5	LED array connected to J94-General IO[4:7]
D6	LED array connected to J95-General IO[28:31]
D7	LED array connected to J94-General IO[8:11]
D8	LED array connected to J95-General IO[32:35]
D9	LED array connected to J100-General IO[12:15]
D10	LED array connected to J100-General IO[16:19]
D11	LED array connected to J101-General IO[36:39]
D12	LED array connected to J100-General IO[20:23]
D13	LED array connected to J101-General IO[40:43]
D14	LED array connected to J101-General IO[44:47]

General Purpose I/O Connections

The 12x3 headers are jumper programmable to connect a particular FPGA pin to either a switch or an LED. The table below provides the connectivity to the device pins.

Net	Pad	BGA	Header	Switch	Device	LED
GEN_FPGA_PIN0	PB4A	AA3	J94	1	2	3
GEN_FPGA_PIN1	PB5C	Y4	J94	4	5	6
GEN_FPGA_PIN2	PB6D	AB4	J94	7	8	9
GEN_FPGA_PIN3	PB7C	W5	J94	10	11	12
GEN_FPGA_PIN4	PB7D	Y5	J94	13	14	15
GEN_FPGA_PIN5	PB8C	AA5	J94	16	17	18
GEN_FPGA_PIN6	PB8D	AB5	J94	19	20	21
GEN_FPGA_PIN7	PB9C	V6	J94	22	23	24
GEN_FPGA_PIN8	PB10C	W6	J94	25	26	27
GEN_FPGA_PIN9	PB10D	Y6	J94	28	29	30
GEN_FPGA_PIN10	PB11C	AA6	J94	31	32	33
GEN_FPGA_PIN11	PB11D	AB6	J94	34	35	36
GEN_FPGA_PIN12	PB12C	W7	J100	1	2	3
GEN_FPGA_PIN13	PB12D	Y7	J100	4	5	6
GEN_FPGA_PIN14	PB14A	V7	J100	7	8	9
GEN_FPGA_PIN15	PB14C	AA7	J100	10	11	12
GEN_FPGA_PIN16	PB20C	AB11	J100	13	14	15
GEN_FPGA_PIN17	PB20D	AA11	J100	16	17	18
GEN_FPGA_PIN18	PB21A	U10	J100	19	20	21
GEN_FPGA_PIN19	PB21C	Y11	J100	22	23	24
GEN_FPGA_PIN20	PB21D	W11	J100	25	26	27
GEN_FPGA_PIN21	PB22A	U11	J100	28	29	30
GEN_FPGA_PIN22	PB22C	AB12	J100	31	32	33
GEN_FPGA_PIN23	PB22D	AA12	J100	34	35	36
GEN_FPGA_PIN24	PB23A	U12	J95	1	2	3
GEN_FPGA_PIN25	PB24A	V11	J95	4	5	6
GEN_FPGA_PIN26	PB24C	AB13	J95	7	8	9
GEN_FPGA_PIN27	PB24D	AA13	J95	10	11	12
GEN_FPGA_PIN28	PB25A	V12	J95	13	14	15
GEN_FPGA_PIN29	PB25C	AB14	J95	16	17	18
GEN_FPGA_PIN30	PB25D	AA14	J95	19	20	21
GEN_FPGA_PIN31	PB36D	W16	J95	22	26	24
GEN_FPGA_PIN32	PB26C	Y13	J95	25	23	27
GEN_FPGA_PIN33	PT9C	A7	J95	28	29	30
GEN_FPGA_PIN34	PT9D	B7	J95	31	32	33
GEN_FPGA_PIN35	PT14C	A10	J95	34	35	36
GEN_FPGA_PIN36	PT15C	C9	J101	1	2	3
GEN_FPGA_PIN37	PT16D	A11	J101	4	5	6
GEN_FPGA_PIN38	PT15D	D9	J101	7	8	9
GEN_FPGA_PIN39	PT19C	B13	J101	10	11	12
GEN_FPGA_PIN40	PT20C	B14	J101	13	14	15

Net	Pad	BGA	Header	Switch	Device	LED
GEN_FPGA_PIN41	PT20D	A14	J101	16	17	18
GEN_FPGA_PIN42	PT22D	E11	J101	19	20	21
GEN_FPGA_PIN43	PT24C	B16	J101	22	23	24
GEN_FPGA_PIN44	PT26C	B17	J101	25	26	27
GEN_FPGA_PIN45	PT27D	D13	J101	28	29	30
GEN_FPGA_PIN46	PT29C	A20	J101	31	32	33
GEN_FPGA_PIN47	PT29D	B20	J101	34	35	36

Non-applicable Headers

These standard headers are used for lab purposes only and are left unused for standard evaluation board use.

Location	Description
J15	HEADER 16X1
J17	HEADER 8X2
J102	HEADER 3x2
J103	HEADER 2x4
J104	HEADER 5X2
J105	HEADER 2x4
J106	HEADER 3x1
J107	HEADER 3x1

SERDES Voltage Supply Selection

These 3x1 standard headers are used for selecting voltage sources for the SERDES power supplies.

Header	Pin 1	Pin 2	Pin 3	Default Shunt
J33	1.8V	VDDIBA	1.5V	2-3
J35	1.5V	VDDA	Banana	1-2
J37	VDDA	VDDGB	Banana	1-2
J39	1.8V	VDDIBB	1.5V	2-3
J41	On-board	VDDIBA	Banana	1-2
J43	On-board	VDDIBB	Banana	1-2
J45	1.8V	VDDOBA	1.5V	2-3
J46	On-board	VDDOBA	Banana	1-2
J48	1.8V	VDDOBB	1.5V	2-3
J49	On-board	VDDOBB	Banana	1-2

VDDIO

These standard 2x4 headers select the input for the VDDIO voltage. Placing shunts connects the specified voltage level to the associated VDDIO bank and are as follows.

Header	VDDIO Bank
J53	VDDIO7
J54	VDDIO6
J55	VDDIO5
J56	VDDIO1
J57	VDDIO0

5	1	3.3V
6	2	2.5V
7	3	1.8V
8	4	1.5V

VDDIO Selection

ORCAstra PC Interface

J133

The standard 12x3 headers select the input for the ORCAstra demo interface. Placing shunts connects the specified source either LPT or USB communications of a PC. Placing shunts across 2-3, 5-6, 8-9, 11-12, 14-15, 17-18, 20-21 and 23-24 will connect the USB to the interface.

The following designators are used to interface with the ORCAstra GUI:

Jack #	Size	Function
D15	LED	Green LED indicates USB connected for ORCAstra
J108	4-pin	Universal Serial Bus (USB) ORCAstra Interface
P1	24-pin	Parallel Port (LPT) ORCAstra Interface

SERDES Reference Clocks

J86, J89

These 1x3 standard headers connect to the reference clock pins of the SERDES to an on-board oscillator or a direct differential reference clock sourced from SMA.

Pin Number		Signal
J86	Pin 1	External
	Pin 2	REFCLKA
	Pin 3	OSC
J89	Pin 1	External
	Pin 2	REFCLKB
	Pin 3	OSC

External REFCLK

These SMA connectors connect to the reference clock pins of the SERDES. These pins receive a direct differential reference clock.

SMA Connector	SERDES Clock
J84	REFCLKA_P
J85	REFCLKA_N
J87	REFCLKB_P
J88	REFCLKB_N

On-board REFCLK

These DIP sockets connect an oscillator for the SERDES reference clocks.

Socket	SERDES Clock	Type	Description
Y1	REFCLKA	4-pin DIP	Oscillator for REFCLKA
Y2	REFCLKB	4-pin DIP	Oscillator for REFCLKB

SERDES Channels

These SMA connectors connect to the SERDES Tx and Rx channels of the SERDES.

SMA Connector	SERDES Channel
J67	HDIN_BD_N
J68	HDOUT_BC_N
J69	HDIN_BD_P
J70	HDOUT_BC_P
J71	HDIN_BC_P
J72	HDOUT_BD_N
J73	HDIN_BC_N
J74	HDOUT_BD_P
J75	HDIN_AD_N
J76	HDOUT_AD_N
J77	HDIN_AD_P
J78	HDOUT_AD_P
J79	HDIN_AC_N
J80	HDOUT_AC_N
J81	HDIN_AC_P
J82	HDOUT_AC_P

Additional SMA Connections

SMA connectors are available to connect to several FPGA clock pins.

SMA Connector	Signal	BGA Pin
J1	PLL_CK6T	AA2
J2	PLL_CK7T	Y2
J3	PBCK0T	W10
J4	PTCK0T	B12
J7	PLL_CK6C	AB2
J8	PLL_CK7C	Y1
J9	PBCK0C	Y10
J10	PTCK0C	A12

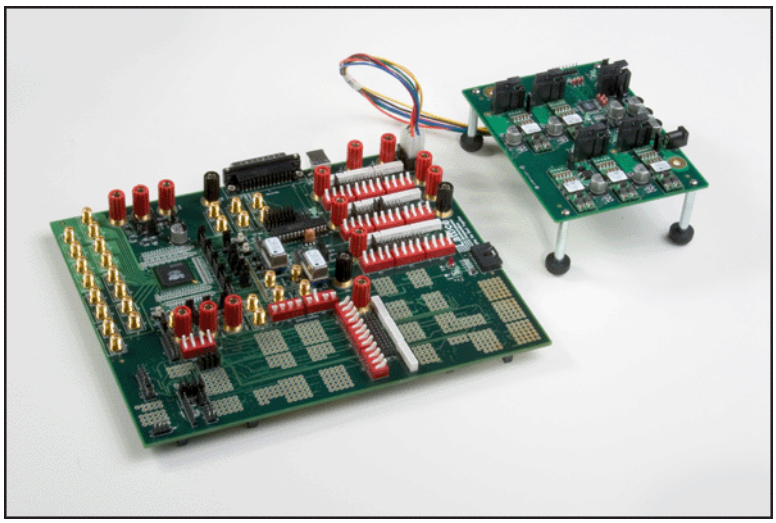
External Power Supply Connections

The following banana jack connectors are available for supplying power to the evaluation board from an external source:

Connector	Type	External	Typical Voltage
J38	Red Binding Post	VDDA	1.5V
J40	Red Binding Post	VDDGB	1.5V
J42	Red Binding Post	VDDIBA	1.5V/1.8V
J44	Red Binding Post	VDDIBB	1.5V/1.8V
J47	Red Binding Post	VDDOBA	1.5V/1.8V
J50	Red Binding Post	VDDOBB	1.5V/1.8V
J59	Black Binding Post	GND	Negative supply
J60	Black Binding Post	GND	Negative supply
J61	Black Binding Post	GND	Negative supply
J63	Red Binding Post	VDD33	3.3V
J64	Red Binding Post	VDD25	2.5V
J65	Red Binding Post	VDD18	1.8V
J66	Red Binding Post	VDD15	1.5V
J90	White Binding Post	GEN_FPGA[0:11]	Input Pad Dependent
J91	White Binding Post	GEN_FPGA[24:35]	Input Pad Dependent
J96	White Binding Post	GEN_FPGA[23:12]	Input Pad Dependent
J97	White Binding Post	GEN_FPGA[36:47]	Input Pad Dependent

A Molex 6-pin power connector (J62) is provided for interconnection of a power module.This module integrates the ispPAC®-PWR1208 device and specified power regulator devices to provide adequate 1.5V, 1.8V, 2.5V and 3.3V rails to supply this board via a standard wall transformer module. Figure 2 highlights the connection between the evaluation and the ispPAC-PWR1208 power module board.

Figure 2. ORT/ORSO42G5 High-Speed SERDES Board with Power Module (ICM) Board



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