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ORSO/ORT82G5-B1 Evaluation Board User Manual

JP4

Schematic page 3

A 7-pin serial connector used for configuration.

Serial Connector	
Pin 1	GND
Pin 2	NC
Pin 3	PROGRMN
Pin 4	DONE
Pin 5	D0
Pin 6	CCLK
Pin 7	VDD

JP6

Schematic page 3

JP6 is an 8-pin JTAG connector. It is physically similar to **JP4**; an arrow indicates pin 1.

JTAG Connector	
Pin 1	GND
Pin 2	INIT_N
Pin 3	RD_CFG_N
Pin 4	TDO
Pin 5	TCK
Pin 6	TMS
Pin 7	TDI
Pin 8	VDD

Header Connections

Standard 0.100 headers are provided for interconnecting points on the board. This can be accomplished with 0.100 IDC connectors and ribbon cable for bus connections or 0.025 pin socket patch cords(such as Pomona Electronics #5948 www.pomonelectronics.com).

D17 & D18

Schematic page 3

These LEDs indicate the status of configuration to the FPGA. When D17 is illuminated this indicates the successful completion of configuration. When D18 illuminates this indicates that the programming was aborted or reinitialized.

JP1 & JP2

Schematic page 2

This is a *standard* header. Pin one is at the bottom left. Pin numbers increment from left to right. The even pins on this header correspond to general I/O pins. The odd pins are connected to ground .

JP3

Schematic page 2

This is a standard header (utilizing the even pins only) as described above. This header connects to 16-LEDs. When a jumper cable is used, output from the ORSO/ORT82G5 can drive these LEDs to display a pattern from JP1 and JP2.

JP35

Schematic pages 4

This is a 3 by 1 header that provids differential input/output from the ORSO/ORT82G5 primary clock spines. The first pin connects to the true side of the pair. Ground is connected to the middle column. The third pin is connected to the complement side of the pair.

J39, 40, 41

Schematic page 6

These 96-pin headers fit with the 860 bus to communicate to a Windriver (www.windriver.com) MPC860 development board.

JP32

Schematic page 5

This jumper selects the data 0 bit between the 860 bus communications and the 7-pin serial connector (**J1**). Jumping pins 2 and 3 selects the serial communication. Jumping pins 1 and 2 selects the 860 bus.

J52 and J53

Schematic page 4

These SMA connectors provide differential input to the PLL clocks.

PLL clocks	
J52	PLL_CLK0C
J53	PLL_CLK0T

JP36

Schematic page 4

This 2x2 header allows connection of ac coupling for J52 and J53. Adding a jumper between pins 1 and 2 or pins 3 and 4 removes the ac coupling capacitor.

PB1, PB2, PB3

Schematic page 3

These push button switches assert/de-assert the logic levels on the FPGA PRGMN, PRESET, and the SERDES reset. Depressing the button drives a logic level "0" to the device.

JP7

Schematic page 3

The 1x2 header enables the de-bounce IC for push-buttons PB1, 2, & 3. Connecting a jumper enables the circuitry.

JP9

Schematic page 3

This 1x3 header is connects PB3 to the SERDES reset or can connect the reset pin to GND.

JP12, JP13, JP14, JP15, JP16

Schematic page 5

These are 2X10 reference voltage headers are used to connect the specified voltage reference pins used by the FPGA IO pins.

JP19, 20, 21, 22,23

Schematic page 8

These jumpers select the input for the VddI/O voltage. Jumper connections are as follows.

1	2	1.5V
3	4	2.5V
5	6	3.3V

JP8

Schematic page 3

This 2x4 header is used to drive the correct levels to the device Mode pins. When left without jumpers to the even (2,4,6,8) pins the device is driven to "1". No jumpers is "1111" for slave serial programming mode.

J51

Schematic page 9

This banana jack is connected to the ground plane of the board.

JP25, 30, 28, 26, 31

Schematic page 9

These 3-pin headers select the source of the SERDES power supplies. When a jumper is placed between Pin 1 and 2 the source of the supply comes from the on-board power supply. When the jumper is between P2 and 3 this selects the source from the adjacent banana jacks to be connected to an external supply.

JP24, 27, 29

Schematic page 9

These 3-pin headers select the source of the device (3.3V, 2.5V, and 1.5V) power supplies. When no jumpers are used the source of the supply comes from the on-board power supply. When the jumper is between P1 and 2 this selects the source from the adjacent banana jacks to be connected to an external supply.

J50

Schematic page 9

This banana jack connects to 5VDC supply.

JP5

Schematic page 3

JP5 is a ten-pin header for additional dedicated signals from the ORSO/ORT82G5. One column of the header (pins 2,4,6, etc) is connected to ground.

J82			
Pin 1	LVDS_R	Pin 2	GND
Pin 3	RCLK	Pin 4	GND
Pin 5	DOUT	Pin 6	GND
Pin 7	LDC	Pin 8	GND
Pin 9	HDC	Pin 10	GND

JP17, 18

Schematic page 5

These headers are the chip select controls. The default is selected when no jumpers are present.

JP10

Schematic page 4

This connector interconnects test points for the SERDES for characterization only. It is not populated for general use. This connector type is an Amp Z-Pack 2mm header. A cable similar to one from W. L. Gore (http://www.wlgore.com/) P/N 2MMA3193-01 adapts the 2mm Z-Pack to individual SMA connectors and is useful to observe signals or connect to other test devices.

JP10									
Pin A1	GND	Pin B1	RBC0	Pin C1	GND	Pin D1	RBC1	Pin E1	GND
Pin A2	WD_SYNC	Pin B2	GND	Pin C2	GND	Pin D2	GND	Pin E2	BYTE_SYNC
Pin A3	GND	Pin B3	GND	Pin C3	GND	Pin D3	GND	Pin E3	GND
Pin A4	GND	Pin B4	GND	Pin C4	GND	Pin D4	GND	Pin E4	XCK

JP11

Schematic page 4

This connector interconnects test points for the SERDES for characterization only. It is not populated for general use. This connector type is an Amp Z-Pack 2mm header. A cable similar to one from W. L. Gore (http://www.wlgore.com/) P/N 2MMA3192-01 adapts the 2mm Z-Pack to individual SMA connectors and is useful to observe signals or connect to other test devices.

JP11									
Pin A1	GND	Pin B1	LDIO0	Pin C1	GND	Pin D1	LDIO1	Pin E1	GND
Pin A2	LDIO2	Pin B2	GND	Pin C2	GND	Pin D2	GND	Pin E2	LDIO3
Pin A3	GND	Pin B3	LDIO4	Pin C3	GND	Pin D3	LDIO5	Pin E3	GND
Pin A4	LDIO6	Pin B4	GND	Pin C4	GND	Pin D4	GND	Pin E4	LDIO7
Pin A5	GND	Pin B5	LDIO8	Pin C5	GND	Pin D5	LDIO9	Pin E5	GND

J26

Schematic page 4

This test point is used to observe the CV (code violation) signal from the SERDES.

SERDES Reference Clocks

Schematic page 4

These SMA connectors connect to the reference clock pins of the SERDES. These pins receive a direct differential reference clock

J13	REFCLKA_N	J14	REFCLKA_P
J22	REFCLKB_N	J23	REFCLKB_P

SERDES Channels

Schematic page 4

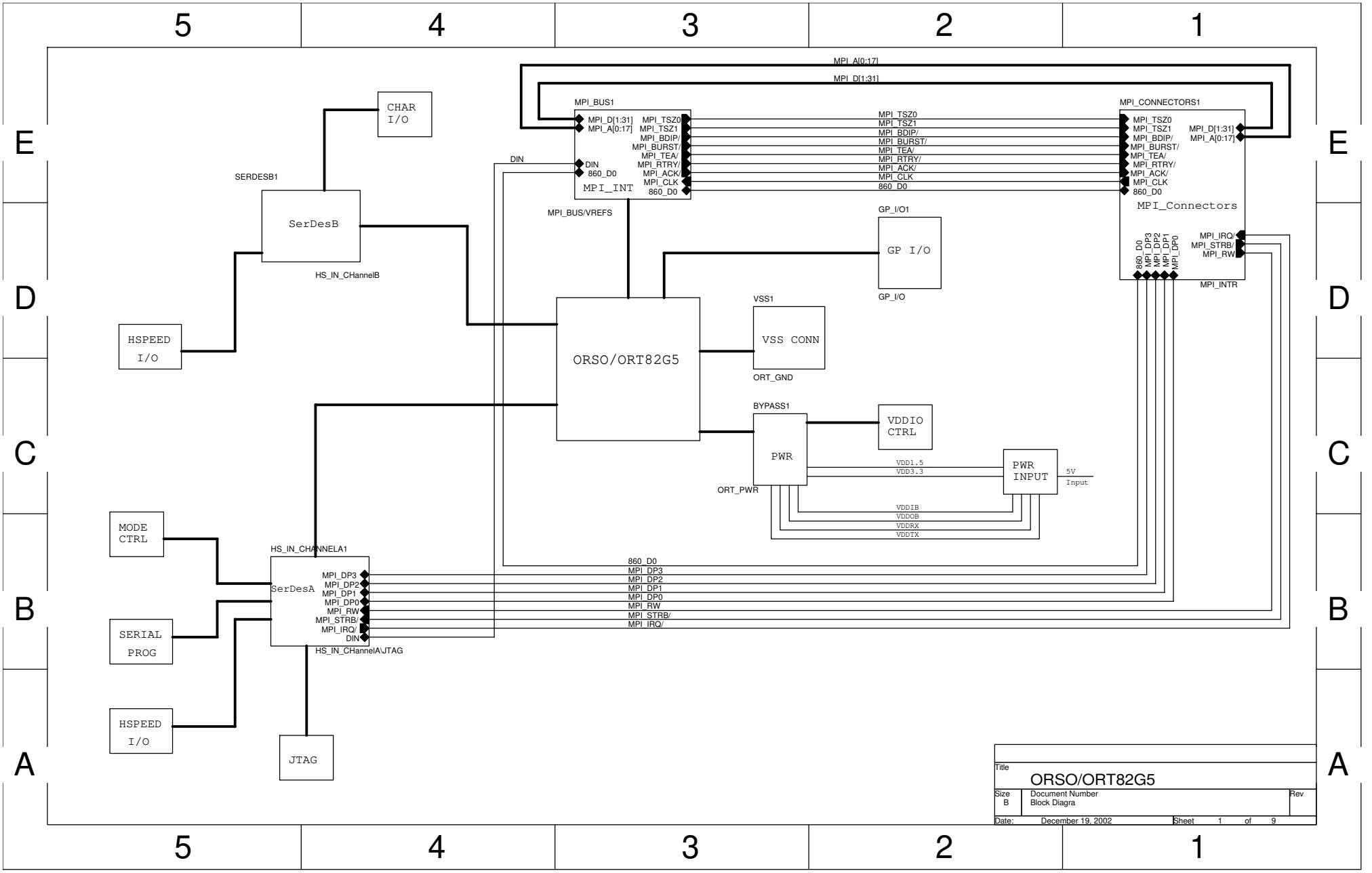
These SMA connectors connect to the SERDES Tx and Rx channels of Quad B of the SERDES. These pins receive a direct differential data.

J19	INN_BA	J24	OUTN_BA
J20	INP_BA	J25	OUTP_BA
J27	INN_BB	J29	OUTN_BB
J28	INP_BB	J30	OUTP_BB
J31	INN_BC	J33	OUTN_BC
J32	INP_BC	J34	OUTP_BC
J35	INN_BD	J37	OUTN_BD
J36	INP_BD	J38	OUTP_BD

JP33 & JP34

Schematic page 3

JP33 and JP34 are unpopulated connections for the SERDES channel A.


MPI_A[0:17]
MPI_D[1:31]
MPI_BUS1
MPI_D[1:31]
MPI_A[0:17]
MPI_TSZ0
MPI_TSZ1
MPI_BDIP/
MPI_BURST/
MPI_TEA/
MPI_RTRY/
MPI_ACK/
MPI_CLK
860_D0
DIN
MPI_INT
MPI_BUS/VREFS
MPI_CONNECTORS1
MPI_Connectors
MPI_INTR
CHAR I/O
SERDESB1
SerDesB
HS_IN_CHannelB
HSPEED I/O
ORSO/ORT82G5
GP_I/O1
GP I/O
GP_I/O
VSS1
VSS CONN
ORT_GND
BYPASS1
PWR
ORT_PWR
VDDIO CTRL
VDD1.5
VDD3.3
PWR INPUT
5V
Input
VDDIB
VDDOB
VDDRX
VDDTX
MODE CTRL
SERIAL PROG
HSPEED I/O
JTAG
HS_IN_CHANNELA1
SerDesA
MPI_DP3
MPI_DP2
MPI_DP1
MPI_DP0
MPI_RW
MPI_STRB/
MPI_IRQ/
HS_IN_CHannelA\JTAG
Title
ORSO/ORT82G5
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B
Document Number
Block Diagra
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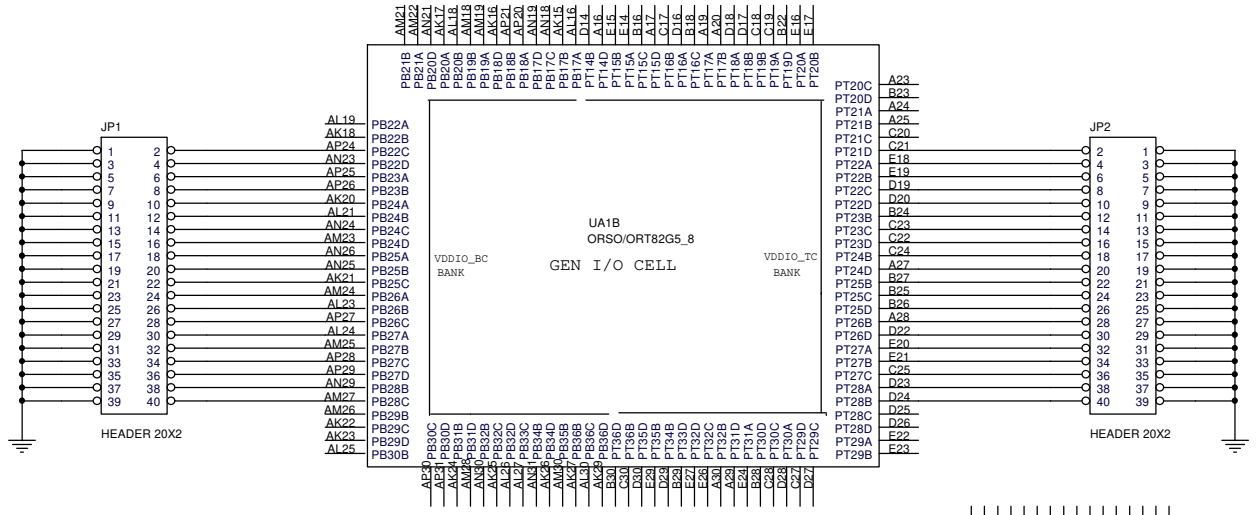
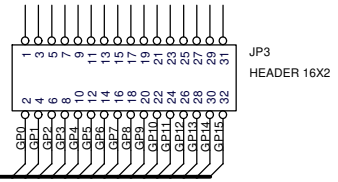
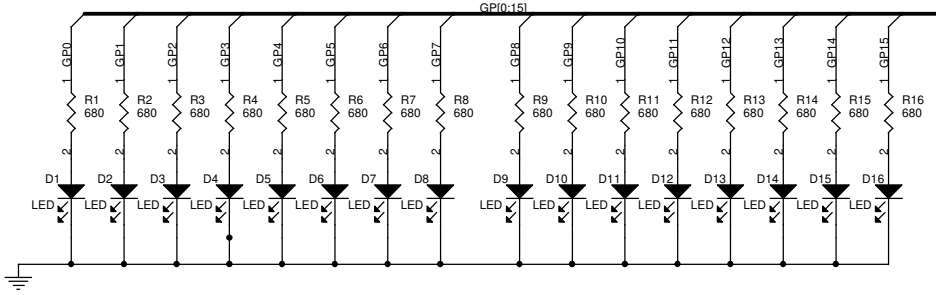
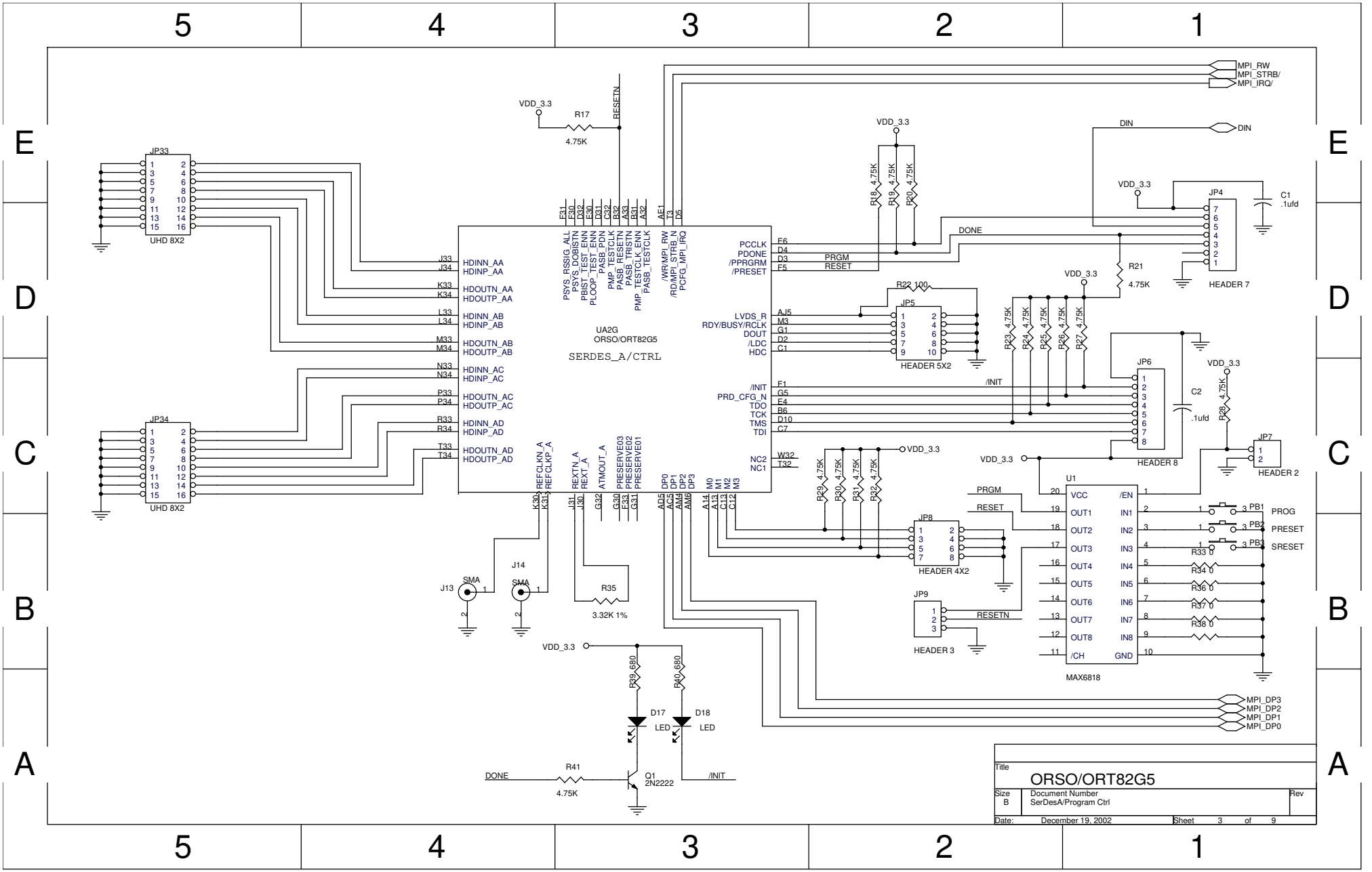






Title	ORSO/ORT82G5	
Size B	Document Number GP_I/O Headers & LEDS	Rev
Date: December 19, 2002	Sheet 2 of 9	


JP33
UHD 8X2
JP34
UHD 8X2
UA2G
ORSO/ORT82G5
SERDES_A/CTRL
HDINN_AA
HDINP_AA
HDOUTN_AA
HDOUTP_AA
HDINN_AB
HDINP_AB
HDOUTN_AB
HDOUTP_AB
HDINN_AC
HDINP_AC
HDOUTN_AC
HDOUTP_AC
HDINN_AD
HDINP_AD
HDOUTN_AD
HDOUTP_AD
RESETN
R17
4.75K
VDD_3.3
MPI_RW
MPI_STRB/
MPI_IRQ/
DIN
PCCLK
PDONE
/PPRGRM
/PRESET
PRGM
RESET
DONE
R18 4.75K
R19 4.75K
R20 4.75K
R21
4.75K
JP4
HEADER 7
C1
.1ufd
R22 100
JP5
HEADER 5X2
LVDS_R
RDY/BUSY/RCLK
DOUT
/LDC
HDC
R23 4.75K
R24 4.75K
R25 4.75K
R26 4.75K
R27 4.75K
JP6
HEADER 8
C2
.1ufd
R28 4.75K
JP7
HEADER 2
/INIT
PRD_CFG_N
TDO
TCK
TMS
TDI
NC2
NC1
R29 4.75K
R30 4.75K
R31 4.75K
R32 4.75K
JP8
HEADER 4X2
JP9
HEADER 3
RESETN
U1
MAX6818
VCC
/EN
OUT1
IN1
OUT2
IN2
OUT3
IN3
OUT4
IN4
OUT5
IN5
OUT6
IN6
OUT7
IN7
OUT8
IN8
/CH
GND
PB1
PB2
PB3
PROG
PRESET
SRESET
R33 0
R34 0
R36 0
R37 0
R38 0
REFCLKN_A
REFCLKP_A
REXTN_A
REXT_A
ATMOUT_A
PRESERVED03
PRESERVED02
PRESERVED01
DP0
DP1
DP2
DP3
M0
M1
M2
M3
J13
SMA
J14
SMA
R35
3.32K 1%
R39 680
R40 680
D17
D18
LED
LED
R41
4.75K
Q1
2N2222
MPI_DP3
MPI_DP2
MPI_DP1
MPI_DP0
Title
ORSO/ORT82G5
Size
B
Document Number
SerDesA/Program Ctrl
Rev
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3
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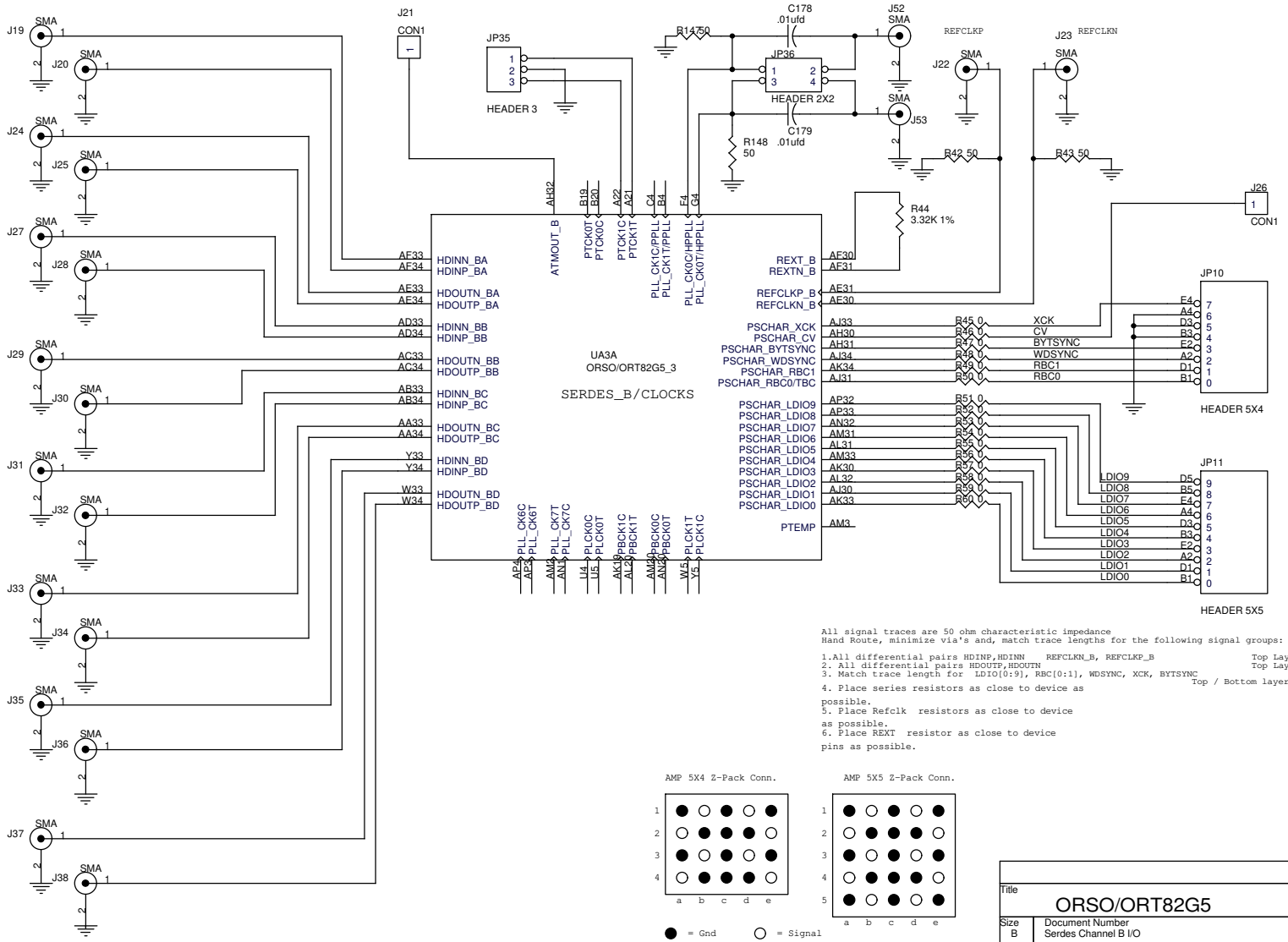
9


SMA J19
SMA J20
SMA J24
SMA J25
SMA J27
SMA J28
SMA J29
SMA J30
SMA J31
SMA J32
SMA J33
SMA J34
SMA J35
SMA J36
SMA J37
SMA J38
J21 CON1
JP35
HEADER 3
C178 .01ufd
C179 .01ufd
JP36
HEADER 2X2
R147 50
R148 50
J52 SMA
J53 SMA
REFCLKP
REFCLKN
J22 SMA
J23 SMA
R42 50
R43 50
R44 3.32K 1%
J26 CON1
UA3A
ORSO/ORT82G5_3
SERDES_B/CLOCKS
HDINN_BA
HDINP_BA
HDOUTN_BA
HDOUTP_BA
HDINN_BB
HDINP_BB
HDOUTN_BB
HDOUTP_BB
HDINN_BC
HDINP_BC
HDOUTN_BC
HDOUTP_BC
HDINN_BD
HDINP_BD
HDOUTN_BD
HDOUTP_BD
REXT_B
REXTN_B
REFCLKP_B
REFCLKN_B
PSCHAR_XCK
PSCHAR_CV
PSCHAR_BYTSYNC
PSCHAR_WDSYNC
PSCHAR_RBC1
PSCHAR_RBC0/TBC
PSCHAR_LDIO9
PSCHAR_LDIO8
PSCHAR_LDIO7
PSCHAR_LDIO6
PSCHAR_LDIO5
PSCHAR_LDIO4
PSCHAR_LDIO3
PSCHAR_LDIO2
PSCHAR_LDIO1
PSCHAR_LDIO0
PTEMP
ATMOUT_B
PTCK0T
PTCK0C
PTCK1C
PTCK1T
PLL_CK1C/PPLL
PLL_CK1T/PPLL
PLL_CK0C/HPPLL
PLL_CK0T/HPPLL
PLL_CK6C
PLL_CK6T
PLL_CK7T
PLL_CK7C
PLCK0C
PLCK0T
PBCK1C
PBCK1T
PBCK0C
PBCK0T
PLCK1T
PLCK1C
R45 0 XCK
R46 0 CV
R47 0 BYTSYNC
R48 0 WDSYNC
R49 0 RBC1
R50 0 RBC0
R51 0
R52 0
R53 0
R54 0
R55 0
R56 0
R57 0
R58 0
R59 0
R60 0
JP10
HEADER 5X4
JP11
HEADER 5X5
LDIO9
LDIO8
LDIO7
LDIO6
LDIO5
LDIO4
LDIO3
LDIO2
LDIO1
LDIO0
All signal traces are 50 ohm characteristic impedance
Hand Route, minimize via's and, match trace lengths for the following signal groups:
1.All differential pairs HDINP,HDINN REFCLKN_B, REFCLKP_B Top Layer
2. All differential pairs HDOUTP,HDOUTN Top Layer
3. Match trace length for LDIO[0:9], RBC[0:1], WDSYNC, XCK, BYTSYNC Top / Bottom layer
4. Place series resistors as close to device as possible.
5. Place Refclk resistors as close to device as possible.
6. Place REXT resistor as close to device pins as possible.
AMP 5X4 Z-Pack Conn.
AMP 5X5 Z-Pack Conn.
= Gnd
= Signal
Title
ORSO/ORT82G5
Size B
Document Number
Serdes Channel B I/O
Rev
Date: December 19, 2002
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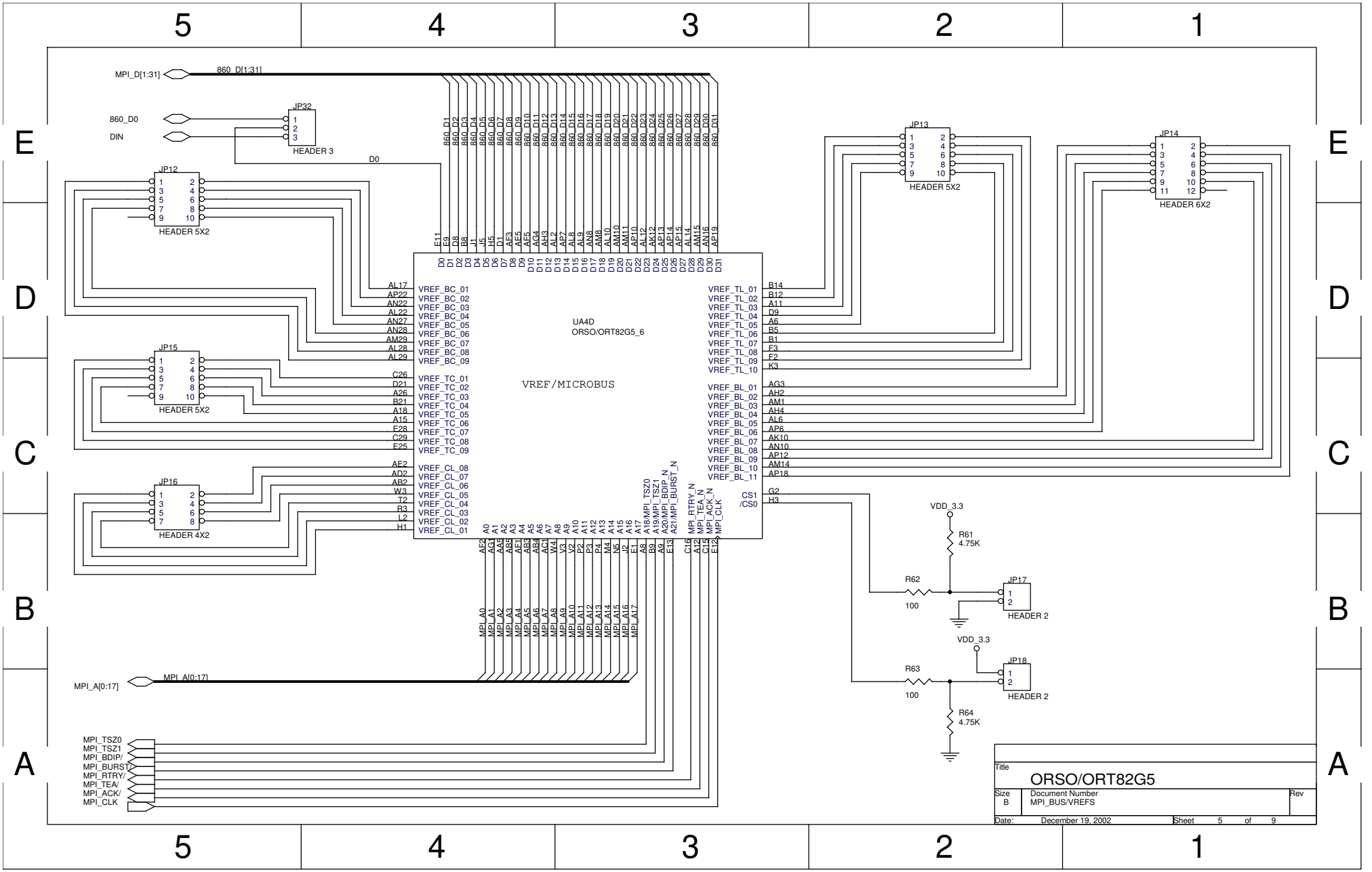
MPI_D[1:31]
860_D[1:31]
860_D0
DIN
JP32
HEADER 3
D0
JP12
HEADER 5X2
JP15
HEADER 5X2
JP16
HEADER 4X2
JP13
HEADER 5X2
JP14
HEADER 6X2
UA4D
ORSO/ORT82G5_6
VREF/MICROBUS
VREF_BC_01
VREF_BC_02
VREF_BC_03
VREF_BC_04
VREF_BC_05
VREF_BC_06
VREF_BC_07
VREF_BC_08
VREF_BC_09
VREF_TC_01
VREF_TC_02
VREF_TC_03
VREF_TC_04
VREF_TC_05
VREF_TC_06
VREF_TC_07
VREF_TC_08
VREF_TC_09
VREF_CL_08
VREF_CL_07
VREF_CL_06
VREF_CL_05
VREF_CL_04
VREF_CL_03
VREF_CL_02
VREF_CL_01
VREF_TL_01
VREF_TL_02
VREF_TL_03
VREF_TL_04
VREF_TL_05
VREF_TL_06
VREF_TL_07
VREF_TL_08
VREF_TL_09
VREF_TL_10
VREF_BL_01
VREF_BL_02
VREF_BL_03
VREF_BL_04
VREF_BL_05
VREF_BL_06
VREF_BL_07
VREF_BL_08
VREF_BL_09
VREF_BL_10
VREF_BL_11
CS1
/CS0
MPI_A[0:17]
MPI_TSZ0
MPI_TSZ1
MPI_BDIP/
MPI_BURST/
MPI_RTRY/
MPI_TEA/
MPI_ACK/
MPI_CLK
VDD_3.3
R61
4.75K
R62
100
JP17
HEADER 2
VDD_3.3
R63
100
JP18
HEADER 2
R64
4.75K
Title
ORSO/ORT82G5
Size
B
Document Number
MPI_BUS/VREFS
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5
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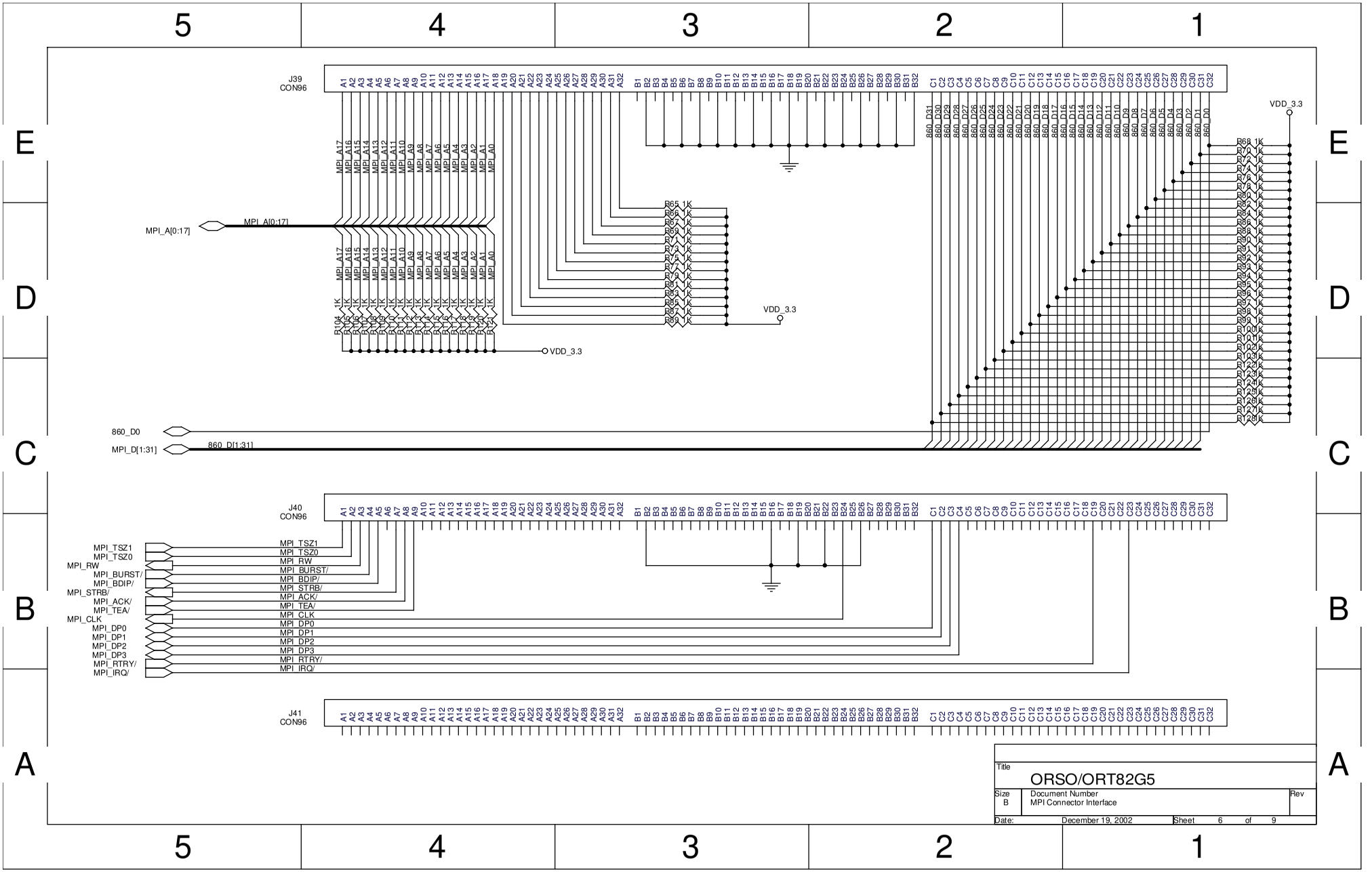
J39
CON96
MPI_A[0:17]
MPI_A17
MPI_A16
MPI_A15
MPI_A14
MPI_A13
MPI_A12
MPI_A11
MPI_A10
MPI_A9
MPI_A8
MPI_A7
MPI_A6
MPI_A5
MPI_A4
MPI_A3
MPI_A2
MPI_A1
MPI_A0
R65 1K
R66 1K
R67 1K
R69 1K
R71 1K
R73 1K
R75 1K
R77 1K
R79 1K
R81 1K
R83 1K
R85 1K
R87 1K
R89 1K
R104 1K
R105 1K
R106 1K
R107 1K
R108 1K
R109 1K
R110 1K
R111 1K
R112 1K
R113 1K
R114 1K
R115 1K
R116 1K
R117 1K
R118 1K
R119 1K
VDD_3.3
VDD_3.3
VDD_3.3
860_D31
860_D30
860_D29
860_D28
860_D27
860_D26
860_D25
860_D24
860_D23
860_D22
860_D21
860_D20
860_D19
860_D18
860_D17
860_D16
860_D15
860_D14
860_D13
860_D12
860_D11
860_D10
860_D9
860_D8
860_D7
860_D6
860_D5
860_D4
860_D3
860_D2
860_D1
860_D0
R68 1K
R70 1K
R72 1K
R74 1K
R76 1K
R78 1K
R80 1K
R82 1K
R84 1K
R86 1K
R88 1K
R90 1K
R91 1K
R92 1K
R93 1K
R94 1K
R95 1K
R96 1K
R97 1K
R98 1K
R99 1K
R100 1K
R101 1K
R102 1K
R103 1K
R120 1K
R121 1K
R122 1K
R123 1K
R124 1K
R125 1K
R126 1K
R127 1K
R128 1K
860_D0
MPI_D[1:31]
860_D[1:31]
J40
CON96
MPI_TSZ1
MPI_TSZ0
MPI_RW
MPI_BURST/
MPI_BDIP/
MPI_STRB/
MPI_ACK/
MPI_TEA/
MPI_CLK
MPI_DP0
MPI_DP1
MPI_DP2
MPI_DP3
MPI_RTRY/
MPI_IRQ/
J41
CON96
Title
ORSO/ORT82G5
Size
B
Document Number
MPI Connector Interface
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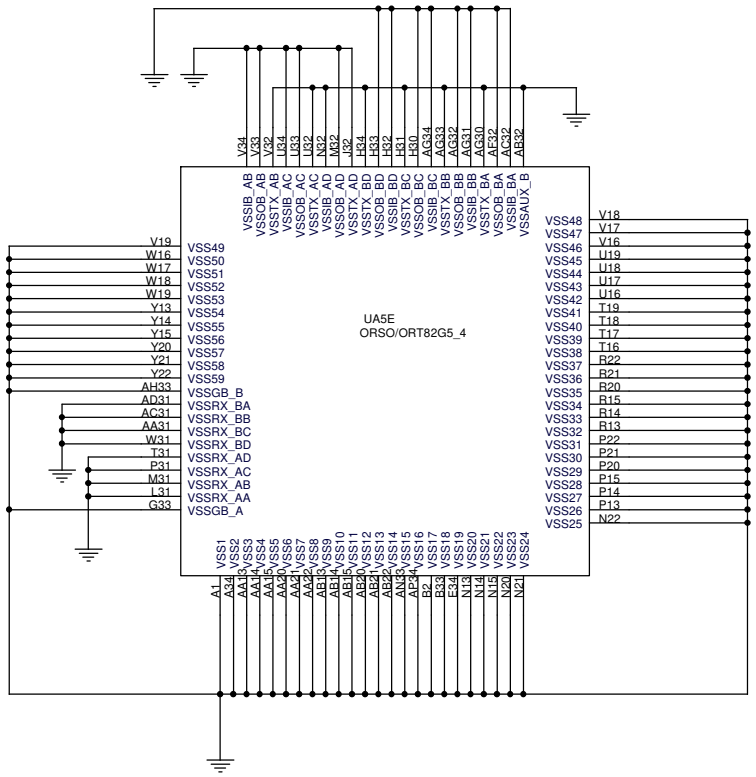
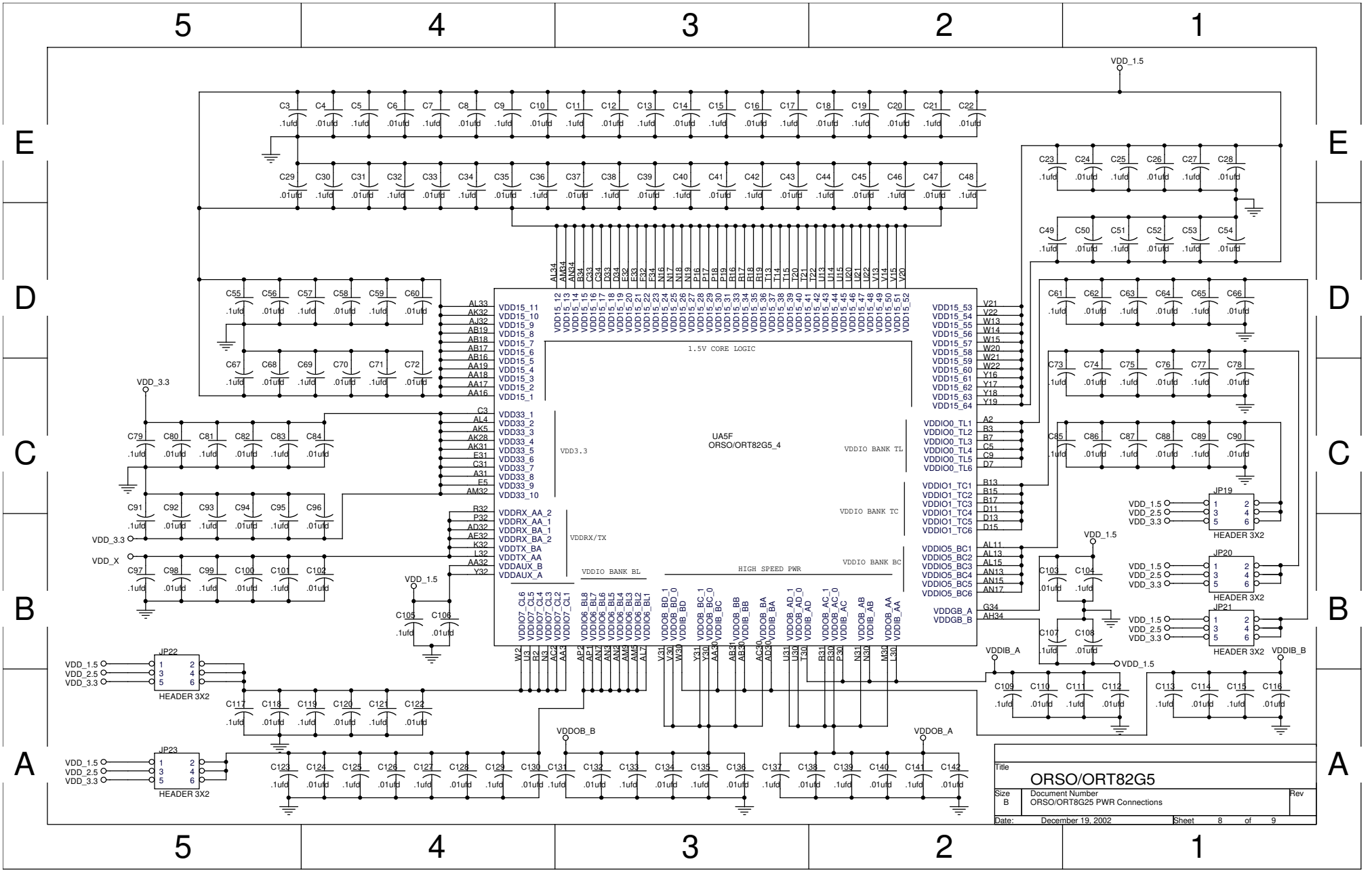


Title	ORSO/ORT82G5	
Size B	Document Number VSS/GND Connections	Rev
Date: December 19, 2002	Sheet 7 of 9	


VDD_1.5
VDD_3.3
VDD_X
1.5V CORE LOGIC
UA5F
ORSO/ORT82G5_4
VDD3.3
VDDRX/TX
VDDIO BANK TL
VDDIO BANK TC
VDDIO BANK BC
VDDIO BANK BL
HIGH SPEED PWR
VDDIB_A
VDDIB_B
VDDOB_A
VDDOB_B
HEADER 3X2
JP19
JP20
JP21
JP22
JP23
Title
ORSO/ORT82G5
Size
B
Document Number
ORSO/ORT8G25 PWR Connections
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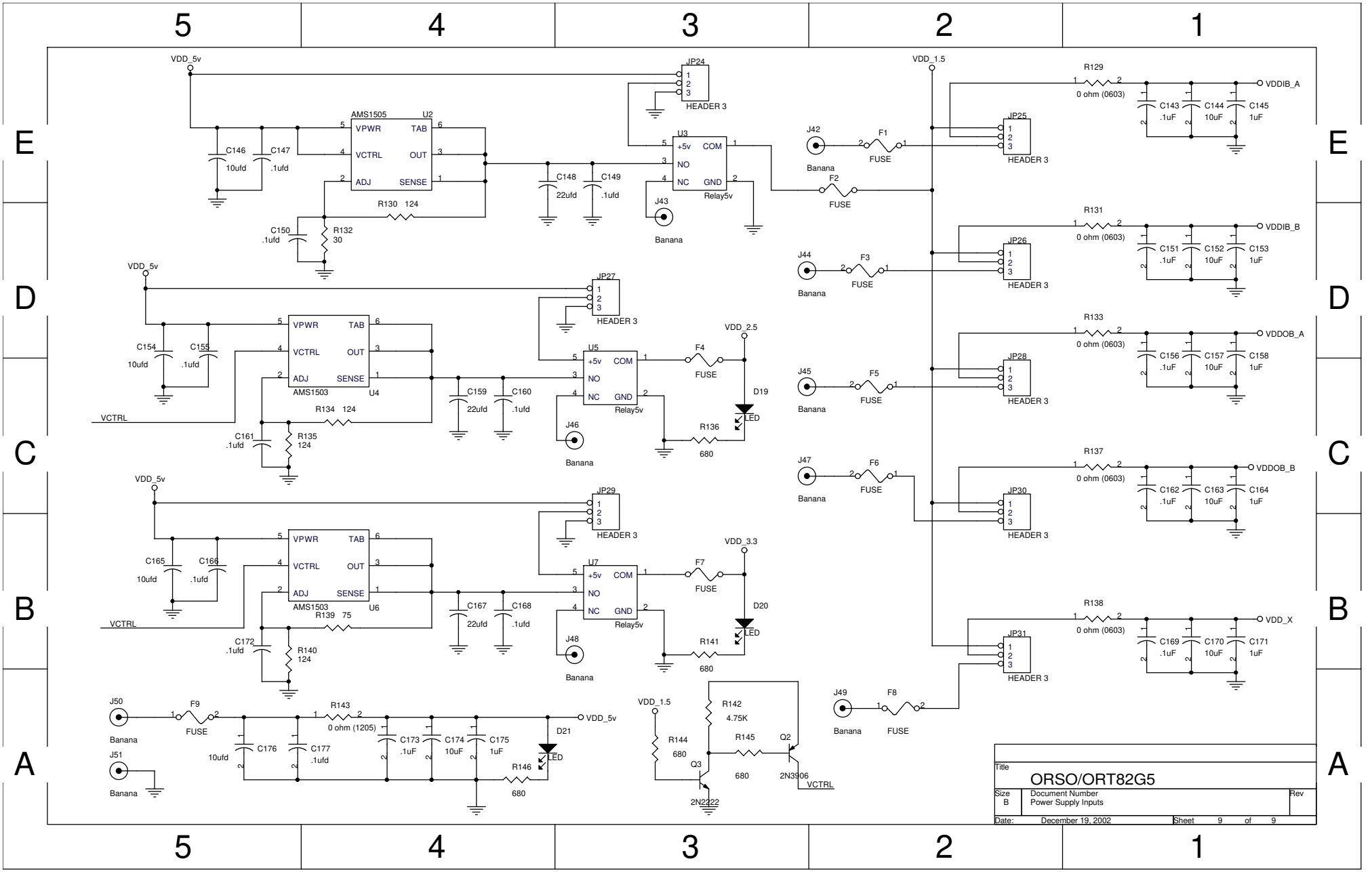
VDD_5v
JP24
HEADER 3
AMS1505
U2
VPWR
TAB
VCTRL
OUT
ADJ
SENSE
C146
10ufd
C147
.1ufd
R130 124
C150
.1ufd
R132
30
U3
+5v
COM
NO
NC
GND
Relay5v
C148
22ufd
C149
.1ufd
J43
Banana
VDD_1.5
J42
F1
FUSE
Banana
F2
FUSE
JP25
HEADER 3
R129
0 ohm (0603)
C143
.1uF
C144
10uF
C145
1uF
VDDIB_A
VDD_5v
JP27
HEADER 3
AMS1503
U4
C154
10ufd
C155
.1ufd
VCTRL
R134 124
C161
.1ufd
R135
124
C159
22ufd
C160
.1ufd
U5
VDD_2.5
F4
FUSE
D19
LED
R136
680
J46
Banana
J44
F3
FUSE
Banana
JP26
HEADER 3
R131
0 ohm (0603)
C151
.1uF
C152
10uF
C153
1uF
VDDIB_B
VDD_5v
JP29
HEADER 3
AMS1503
U6
C165
10ufd
C166
.1ufd
VCTRL
R139 75
C172
.1ufd
R140
124
C167
22ufd
C168
.1ufd
U7
VDD_3.3
F7
FUSE
D20
LED
R141
680
J48
Banana
J45
F5
FUSE
Banana
JP28
HEADER 3
R133
0 ohm (0603)
C156
.1uF
C157
10uF
C158
1uF
VDDOB_A
J47
F6
FUSE
Banana
JP30
HEADER 3
R137
0 ohm (0603)
C162
.1uF
C163
10uF
C164
1uF
VDDOB_B
J50
F9
FUSE
Banana
J51
Banana
R143
0 ohm (1205)
C176
10ufd
C177
.1ufd
C173
.1uF
C174
10uF
C175
1uF
D21
LED
R146
680
VDD_5v
VDD_1.5
R142
4.75K
R144
680
R145
680
Q2
2N3906
Q3
2N2222
VCTRL
J49
F8
FUSE
Banana
JP31
HEADER 3
R138
0 ohm (0603)
C169
.1uF
C170
10uF
C171
1uF
VDD_X
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Power Supply Inputs
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